Sr. No.....

Dec 2018

B.Tech. III SEMESTER

Digital Electronics and Computer Organization (CE-207/[redacted])

Time: 3 Hours | Max. Marks:60

Instructions:
1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

		PART –A	
Q1	(a)	A 4 bit binary counter starts count from 0000. What will be its count after 45 pulses?	(2
	(b)	Determine the single error-correcting code for the message code 01101. Assume the parity code is even.	(2)
	(c)	List various binary codes? Represent the given number $(9238)_{10}$ in (i) BCD code (ii) Excess-3 code (iii) Gray code	(2)
	(d)	Construct a 16X1 multiplexer using multiple 4X1 multiplexers. Write truth-table for the same.	(2)
	(e)	What is race around condition? In which flip-flop it occurs? How it can be eliminated?	(2)
	(f)	The Q output of D and J-K flip-flops is 1. It changes to 0 when a clock pulse is applied. What are the possible values of D, J and K?	(2)
	(g)	How many references to memory are needed for each direct and an indirect address instruction to bring an operand into a processor register.	(2)
	(h)	Discuss the basis of Flynn's classification of computers. List all categories with brief description.	(2)
	(i)	Differentiate between hardwired and micro programmed control unit.	(2)
	(j)	Determine values of x and y, which satisfies the following expressions $(46)_x = (55)_y$ and $(49)_y = 45$.	(2)
		PART –B	
Q2	(a)	Draw the logic circuit of J-K flip-flop using D flip-flop. Explain complete conversion process.	(5)
	(b)	What is an instruction? Classify instructions on the basis of addressing modes, operation performed and number of address fields.	(5)

	(b)	What is store program concept? Explain multilevel viewpoint of digital machine.	(5)
Q4		Design MOD-10 Synchronous and Asynchronous counter using any flip-flop. Explain complete design process.	(10)
Q5	(a)	Define Fetch-Decode-execute cycle? Draw and discuss complete instruction cycle?	(5)
	(b)	Implement the following using 3 :8 line decoder and 4:1 multiplexer: (i) $Y(A,B,C)= \sum m(2,3,4,6)$ (ii) Half-subtractor	(5)
Q6	(a)	Simplify the following equation using K-map and Boolean Algebra. Implement it in NAND logic. $F(A,B,C,D)= \sum m(0,2,4,7,8,9)+d(3,10,14,15)$	(5)
	(b)	An instruction is stored at location 206 with its address field at location 207. The address field has the value 800. A processor register R1 contains the number 475. Evaluate the effective address if the addressing mode of the instruction is: (i) Direct (ii) Immediate (iii) Relative (iv) Register indirect (v) Index with R1 as the index register	(5)
Q7		Briefly differentiate between: 1. Shift and storage register 2. Combinational and sequential circuit 3. Decoder and demultiplexer 4. Primary and secondary memory 5. RISC and CISC processor	(10)