MODELING, ESTIMATION AND REDUCTION OF TOTAL LEAKAGE IN SCALED CMOS LOGIC CIRCUITS

THESIS

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DECLARATION

I hereby declare that this thesis entitled "**MODELING, ESTIMATION AND REDUCTION OF TOTAL LEAKAGE IN SCALED CMOS LOGIC CIRCUITS**" by **NITIN SACHDEVA**, being submitted in fulfilment of the requirements for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under Faculty of Engineering & Technology, J.C. Bose University of Science & Technology, YMCA Faridabad, during the academic year 2020-2021 is a bona fide record of my original work carried out under guidance and supervision of **Dr. Munish Vashishath, Professor,** Electronics Engineering Department, J.C. Bose University of Science & Technology, YMCA, Faridabad and **Dr. P.K Bansal, Professor, Former Principal,** Malout Institute of Management and Information Technology**,** Malout, Punjab and has not been presented elsewhere.

I further declare that the thesis does not contain any part of any work which has been submitted for the award of any degree either in this university or in any other university.

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ABSTRACT

Metal oxide semiconductor (MOSFET) is the most important promising building block of Very-Large-Scale Integrated (VLSI) circuits due to its incomparable properties. Both the International Technology Roadmap for Semiconductor Technology (ITRS) and Moore's Law played a most important role in progressing CMOS technology. In specific, the road map was a significant guiding document that provides the direction for next-generation devices in research and development. The requirement for greater packing density, low power consumption, high speed, and low price needs aggressive MOSFET scaling. MOSFET with 16 nm will be accessible in 2010, 10 nm in 2015, 6 nm in 2020, according to the latest edition of the ITRS. Continuous scaling-down the dimensions of MOSFET needs an investigation of the impact of scaling on performance of MOSFET. The most critical performance parameters of MOSFET are cut-off frequency, threshold voltage, mobility, gate leakage and time delay. As the size of the device decreases, the sharing of charges from source to drain raises leading to reduced gate control over the depletion region of the channel. Hence, decreasing the device channel length leads to short channel effects such as drain-induced barrier lowering (DIBL), threshold voltage lowering (V_{th}), Punch-through, channel length modulation and hot carrier effects.

Minimization of channel width also results in a decrease in the current drivability and deterioration caused by the hot carriers owing to the high electric field at the bottom of the field barrier. Currently the VLSI sector's growth focuses primarily on the way semiconductor devices are effective which in turn is highly dependent on the advancement of CMOS technology. Leakages and short-channel effects (SCE) pose big challenges in the design of CMOS devices as the size of the device enters the nano-scale regime. CMOS has become the most widely used technology to be implemented in high-scale integration chips (VLSI) due to high noise immunity, low static power consumption, and high packaging density.

The main goal of the integrated circuit design and production is to use low power, small area, and low price to achieve high-speed performance. From small scale integration to Giga scale integration, integrated innovations are rising. In the literature review,

conventional MOSFETs are discussed to outline current MOSFET structure, existing methodologies and challenges take place due to scaling.

There are different methods of reducing the leakage current of the device by adjusting the work-function of the Gate, Poly doping, Halo doping and Threshold Implant concentration to limit the leakage current of the device. To enhance the performance of the device further, the silicon channel is replaced with two-dimensional materials to achieve higher I_{ON}/I_{OFF} ratio to be used in RF and wireless communication applications and reduced off-state leakage current to be used in low power applications.

In this research work, the two-dimensional model for surface potential is obtained by solving Poisson's Equation and estimation of threshold voltage for novel silicon MOSFET is presented. Leakage current is the main aspect of the high-power dissipation contribution. It should be less for low-power applications. The improvement of the sub-threshold current has now become the primary issue. Different methods are discussed and implemented in this research to reduce it. In scaled devices, the impact of sub-threshold current is directly proportional to the supply voltages and leakage current results due to scaling down of supply voltage. Sub-threshold current has been reduced by controlling the device process parameters i.e. channel length, width, thickness of gate oxide, doping profile etc.

Enhanced chip density, enhanced driving current, enhanced transistor trans-conductance and cutoff frequency are the main merits of downscaling of the transistors. Different parameters are derived analytically and simulated to match with each other such as threshold voltage, sub-threshold leakage current, sub-threshold slope and DIBL. The parameters i.e. gate oxide thickness, poly doping concentration, substrate doping, source/drain doping, threshold implant concentration, halo doping, work-function and doping distributions are adjusted to obtain the enhanced output parameters of the device. The extracted parameters are Drain current characteristics, threshold voltage, sub-threshold current, ON/OFF ratio, DIBL, sub-threshold slope, trans-conductance and Capacitance-Voltage characteristics. The entire design, virtual fabrication, simulation and extraction of parameters have been performed in the numerical-based tool-SILVACO.

The primary objective of this research work is to design and evaluate different methods for producing the device with decreased leakage current and greater ON/OFF current ratio. The lightly doped substrates are preferred here to enhance the ON current, lower substrate current and for better noise immunity rather than heavily doped substrates preferred in existing devices.

The work-function variation of gate electrode demonstrates that the lightly doped substrate devices have reduced OFF-state leakage and DIBL which is best suitable for low-power applications. The device is designed having different effective channel lengths 40nm and 18nm as per ITRS guidelines. The doping profiles Gaussian and Pearson have been used during virtual fabrication to investigate the device characteristics. The device with Pearson Doping Profile is giving less OFF-state leakage current. PMOS device is also designed using Gaussian Doping Profile. The effect of variation of the halo implant, gate oxide thickness and threshold implant that impacts the threshold voltage, drain current, leakage current and substrate current of the device has been explored.

Dual material SOI has been designed and simulated to enhance the performance of the device. The device is designed with a dual material gate i.e having two different work-functions with single and dual halo doping in the lightly doped channel and high k material Hafnium oxide (HfO2) is used as a gate dielectric material. Decreased OFF-state leakage current is achieved by incorporating the dual halo in the channel region.

Graphene is a comparatively latest material that holds promise for electronic applications with its unique characteristics. Graphene-Silicon on Insulator (G-SOI) is designed and simulated with graphene as a channel material. It is a wonderful device that the semiconductor industry has greatly valued in most recent years due to its high mobility and high ON current. G-SOI is presented with two-dimensional graphene material as a channel material, hexagonal Boron Nitride as a substrate and with new high-k gate oxide material Lanthanum Gadolinium Oxide (La_2GdO_3) to obtain a higher I_{ON}/I_{OFF} ratio and lower device sub-threshold current. It is concluded from the simulation results that the G-SOI with chosen device structure parameters gives greater ON current, reduced sub-threshold swing, lower off-current (I_{OFF}) and greater ON/OFF current ratio. The device is designed and compared with various substrates and different oxide materials. The primary motivation of

this design is to obtain maximum ON/OFF current ratio, reduced sub-threshold current and DIBL for best performance device. The ON/OFF ratio is extracted and also compared with previous research work. This research work provides the highest value of the I_{ON}/I_{OFF} ratio which is good enough to switch from the UTB-SOI devices to G-SOIs.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

Abbreviation	Description
2D	Two dimensional
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
DIBL	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
ITRS	International Technology Roadmap for Semiconductors
I_{ON}	ON-current
I_{OFF}	Leakage current
L_G	Gate Length
L_{eff}	Effective gate length
N	Doping Concentration
Si	Silicon
SiO_2	Silicon dioxide
t_{ox}	Gate oxide thickness
Si_3N_4	Silicon Nitride
V_{DD}	Supply voltage
V_{DS}	Drain to Source voltage
V_{GS}	Gate to Source voltage
V_{T0}	Threshold voltage at zero substrate bias
w_f	Work-function
TCAD	Technology Computer Aided Design
S/D	Source/Drain
SCE	Short Channel Effects
ρ	Charge density
ε	Permittivity
n	electrons
k	Boltzmann's constant

q	Electron charge
μ_n	Electron mobility
HfO_2	Hafnium Oxide
$LaGdO_3$	Lanthanum Gadolinium Oxide
HD	Heavily Doped
LD	Lightly Doped
SiC	Silicon Carbide
h-BN	Hexagonal Boron Nitride
G-SOI	Graphene-Silicon on Insulator
I_D	Drain Current

CHAPTER 1
INTRODUCTION

1.1 PREAMBLE

Over the last few years, semiconductor manufacturing has done notable progress and primarily leading to fast advancement in integration techniques as well as the design of large-scale devices. As the integration level of chip improves, there is more complication in manufacturing. The transistor size is switched from micrometer to nanometer. In 1947, the first transistor was invented at Bell Labs; the electronics sector is switched from electron tubes to solid-state electronic devices [1]. The development in solid-state electronics research in particular and semiconductor-based electronics trade began with the growth of bipolar transistors which is found to be one of the most significant innovations in 20th century. This innovation of bipolar devices had an extraordinary effect on the growth of the science and technology of semiconductors at that time. The bipolar junction transistors (BJTs) are replaced by MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) in Digital Electronic Circuits [2]. MOSFET is a semiconductor device widely used for switching and amplifying electronic signals in electronic systems. MOSFET is a core of an integrated circuit that can be designed and produced in one chip due to its very tiny size. CMOS (Complementary Metal Oxide Field Effect Transistor) is a major component of digital and analog integration. CMOS technology is the chosen technology for the construction of various integrated circuits i.e. microprocessors, microcontrollers, memory chips, sensors, data converters and several communication applications. The size of the system must be reduced to accommodate more transistors on a single chip. The scaling down of transistor sizes results in different unexpected issues that degrade the efficiency of the device. The various short channel effects, leakage current issues and threshold voltage variation etc. occur due to the scaling issues [3].

This study aims to investigate the issues caused by scaling the dimensions of MOSFET and applying alternative methods to manage them. Various architectures, channel materials and modified structures are suggested to solve the issues in existing devices. Different techniques are explored to reduce the leakage current. Additional changes in the existing MOS structures such as Halo doping, threshold voltage implant and work-function engineering [4] are illustrated to control the sub-threshold leakage and DIBL.

Various channel materials such as Graphene is utilized during virtual fabrication of the device to get a higher I_{ON}/I_{OFF} ratio.

1.2 INTEGRATED CIRCUIT TECHNOLOGY TRENDS

Increasing the number of transistors assembled on a single chip result in various levels of integration. The problem was the size of the transistor at that time. Large size components and their interconnections in the computer slowed down the system speed. This problem motivates the Engineers to develop a system to incorporate all the components on a single chip. The integrated circuit was invented by Jack Kilby and Robert Noyce. An integrated circuit is a circuit that combines the active and passive components on a single chip. As the number of transistors is increased by reducing the transistor's dimensions, the level of integration is increased from Small-Scale Integration to Giga-Scale Integration as shown in Figure1.1

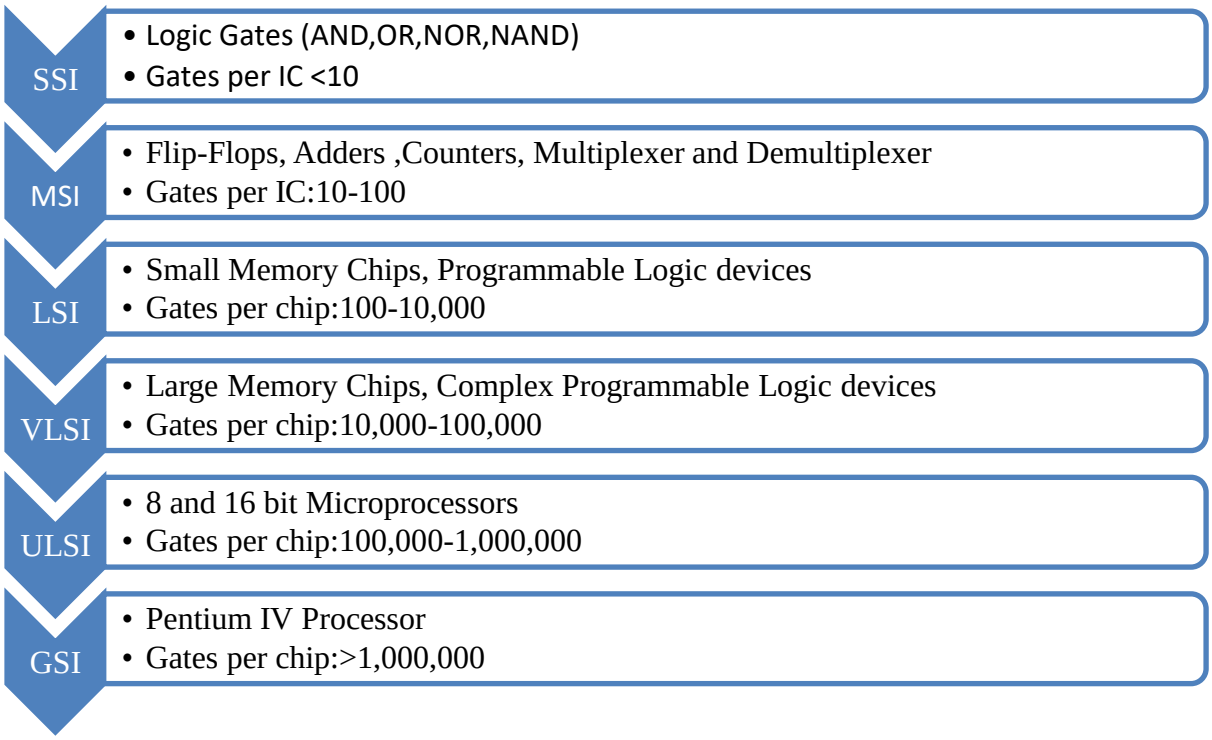


Figure 1.1 Levels of Integration

Miniaturization with Very Large-Scale Integration (VLSI) in the areas of multimedia communication, image processing and many broadband applications has been increasing at a very fast speed. It is a system of integration on a single silicon chip with millions of MOS transistors. When complexity increases exponentially, this contributes to ultra-large-scale (ULSI) implementation [5]. Miniaturization further enabled

intelligence to be integrated into almost any human-use gadget whether it is a mobile phone or a car or a washing machine.

1.3 MOORE'S LAW

In 1965, Intel's co-founder, Gordon Moore reported that several transistors on a chip were doubled after every two years. [6]. He expected this trend of an increasing number of transistors to continue in the future also. This law describes the huge change in productivity, economic growth, and technology. Moore explained why and how, over time, our technology is becoming thinner, lighter and quicker. Each silicon chip generation gains more transistors that are added every two years-in reality and becomes double. As the chips are miniaturized, it will cut the cost in long run. This law results in further advancements in Digital and Analog applications. Figure 1.2 shows the density of chips is increasing year by year.

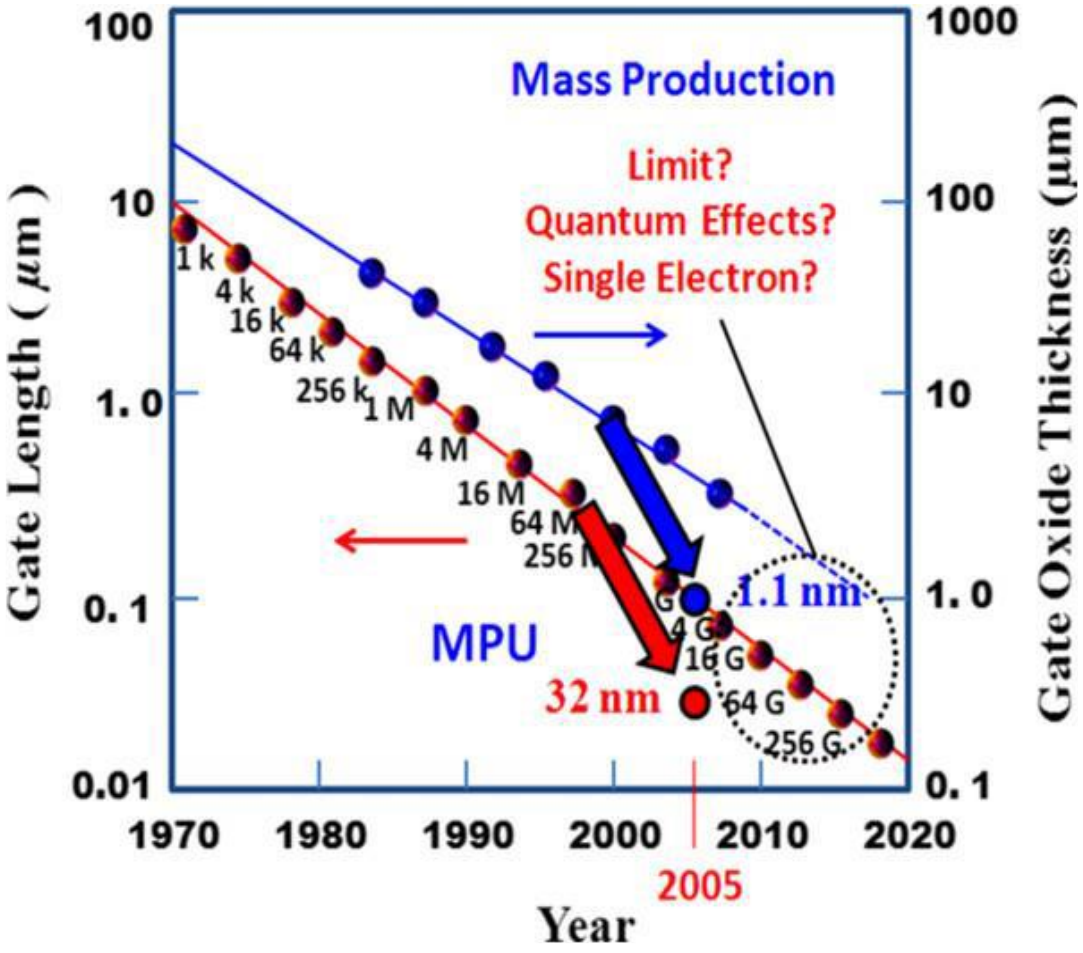


Figure 1.2 Technology Progress

1.4 AN OVERVIEW OF MOSFET

Microelectronics production, automation, data sharing and signals processing over the past thirty years has been heavily dependent on the very large-scale integrated circuit (VLSI) market. High-speed, ultra-small, low-power semiconductor chips, sensors and all innovative materials are all attributed to VLSI development. In 1960, Kahng and Atilla conducted the first practical exhibition on MOSFETs based on Silicon. Jack Kilby and Robert Noyce of the Fairchild Corporation invented the Integrated Circuits (IC) concept at Texas Instruments in 1958. MOSFET is a semiconductor device broadly used in electronic systems for switching and amplifying electronic signals. It is a component of an integrated system that can be built and assembled in one chip due to its short dimensions. The MOSFET is a four-terminal device comprising terminals Source(S), Gate(G), Drain(D) and Substrate (B) as shown in Figure 1.3. The MOSFET's substrate is connected to the source making it like the field-effect transistor a three-terminal device.

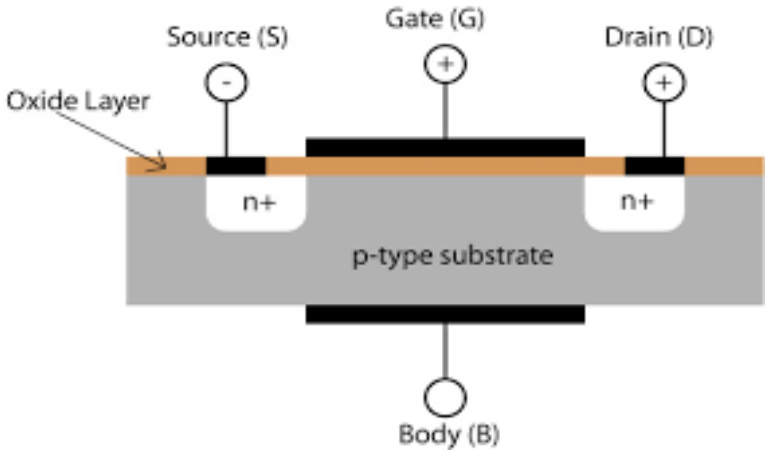


Figure 1.3 MOSFET Structure

A voltage drop across the oxide causes a conducting channel between the source and drain as a result of the voltage applied in the MOSFET in enhancement mode. The enhancement-mode refers to increased conductivity of the oxide field attracting channel carriers and forms the inversion layer. The channel can contain electrons (for n-type MOSFET) or holes (for p-type MOSFET) reversing the substrate in nature so that n-type MOSFET is ready with a p-type substrate and p-type MOSFET with an n-type substrate. In depletion mode of MOSFET, the channel is already pre-fabricated at the time of production and contains carriers to the substrate in a reverse-type surface layer. It degrades conductivity by adding a field that eliminates carriers from that surface layer. The MOSFET gate can be made of poly-silicon or metal gates. Different

dielectric materials can be used as gate oxides depending upon the compatibility of the device. MOSFET has three specific regions: Cutoff Region, Linear Region and Saturation Region depending on the voltage connected to the gate. When the PMOS transistor is connected as a load transistor and the NMOS transistor is connected as a driver, then it forms CMOS. With the advent of CMOS technology that uses the minimum power and scaling technology has progressed from Small Scale Integration (SSI) to Very Large-Scale Integration (VLSI). CMOS (Complementary Metal-Oxide Semiconductor) becomes a predominant integrated circuit production technology. This dominance of CMOS technology will remain for centuries to come in the manufacture of Integrated Circuits or ICs. CMOS technology is associated with VLSI (Very Large-Scale Integration) technology with a few million or even billions of transistors integrated into a single chip. Reliability, low power consumption, significantly low price and most importantly scalability are the reasons for the dominant use of CMOS technology in the manufacture of VLSI chips.

1.5 MOSFET SCALING

Scaling is defined as a managed change in physical and electrical properties resulting in a decreased chip area while maintaining the device's output. It is often referred to as reducing the size i.e. MOSFET dimensions. MOS transistor scaling requires the systematic decrease of the overall dimensions of the device as allowed by the existing technology while maintaining the geometric ratios found in the larger devices. The scaling results in varying device parameters such as threshold voltage, gate oxide thickness, channel size and width.

1.5.1 Need for Scaling

Scaling has improved device performance, cost, circuit speed, packing density, Gate delay and Power dissipation. Higher package density can be achieved through scaling, reduced supply voltage and increased substrate concentration. As a result of scaling, good electrostatic gate control has been achieved which reduces the overall cost of the chip. The circuit speed has been increased due to the fast switching of smaller transistors. Reduction in dimensions of transistors i.e scaling also has its advantages and disadvantages for VLSI chips. Scaling also gives rise to an increase in device density, reduction in depletion region width to obstruct the contact of source and drain depletion regions, increased built-in potential and most importantly undesired sub-

threshold current increases. The net consideration is that by increase and decrease in various parameters leads to second-order effects. The need for feature size of MOSFET arises to improve the two major factors such as threshold voltage and channel length. The reduction of these two parameters results in short channel effects [7]. To keep the short channel effects under check, the advanced lithographic methods and ion implantation methods are important to optimize any unit. The deep submicron varies from 90 nm to 65 nm and the ultra-deep submicron ranges from 45 nm to 32 nm. Due to these scaling dimensions of the transistor, the electrical performance of the device degrades to the breakdown of the drain junction, punch through, short channel effects, hot electron generation, leakage current, MOS transistor threshold voltage fluctuation, contact resistance, parasitic resistance, parasitic capacitance, and MOSFET threshold voltage mismatch as well as other device parameters

1.5.2 Types of Scaling

There are two types of scaling:

(a) Constant Field Scaling: The motive of this type of scaling is to scale system voltages and device dimensions at the constant electric field (both horizontal and vertical). When the size of the device and the voltage of the supply are decreased, the circuit delay is also reduced by factor k [8]. The scaling down of circuit delay increases the circuit speed. The circuit density is increased due to more incorporated transistors due to scaling but the active power per chip area remains unchanged. As a result of this type of scaling, the power delay product has a significant improvement.

(b) Constant Voltage Scaling: This method of scaling relates to the scaling of the intensity of the electric field and doping. Under constant voltage scaling, the parameters i.e the inversion region charge per unit area, mobile load size, inversion layer thickness and Debye length are scaled.

CMOS Technology has been followed by mixed steps of Constant Field and Constant Voltage Scaling to increase system performance. Constant Field Scaling is used to achieve higher circuit density and speed without loss of reliability and power. But there are some non-scalable factors such as KT/q thermal voltage, built-in junction, layer width depletion, bandgap, and threshold voltage. Other parameters like the non-scalability of threshold voltage results in the non-scaling of sub-threshold current.

When the physical dimensions of the transistors are scaled-down the sub-threshold current increases by factor k at constant threshold voltage. It is due to the exponential relationship between sub-threshold current and threshold voltage.

1.6 SCALING LIMITATIONS

Fabricating MOSFETs with much shorter channel lengths are a major issue nowadays and the problems of manufacturing semiconductor devices are always a notification sign in developing integrated circuit production. Over the past few years, the small dimension of the MOSFET has developed operational disorders under a few tens of nanometers. Due to the possibility of using optical lithography to pattern any tiny feature on silicon, the incorporation of billions of transistors on a chip can be possible. As optical lithography joins the regime of sub-wavelength, light diffraction and interference from the structure of sub-wavelength create image dysfunction. Hence, patterning becomes hard without implementing methods for improving resolution. The gate oxide thickness must be decreased to preserve the supply voltage and threshold voltage resulting in gate leakage current.

1.6.1 Drain Induced Barrier Lowering (DIBL)

This is a short channel effect resulting from the threshold voltage decrease at greater drain voltages [9] [10]. For long channel devices, the threshold voltage is independent due to the sufficient distance between the channel and the drain. Nevertheless, in short channel devices the drain voltage is increased due to the shortening of the channel. The depletion of the source comes closer to the drain's depletion region and the drain/source becomes closer to the channel results in turn-on the transistor prematurely. As a result, the source potential is reduced due to the penetration of electrical fields resulting in higher source penetration of electrons over the decreased channel barrier [11] [12] resulting in threshold voltage changes. Figure 1.4 shows the DIBL effect.

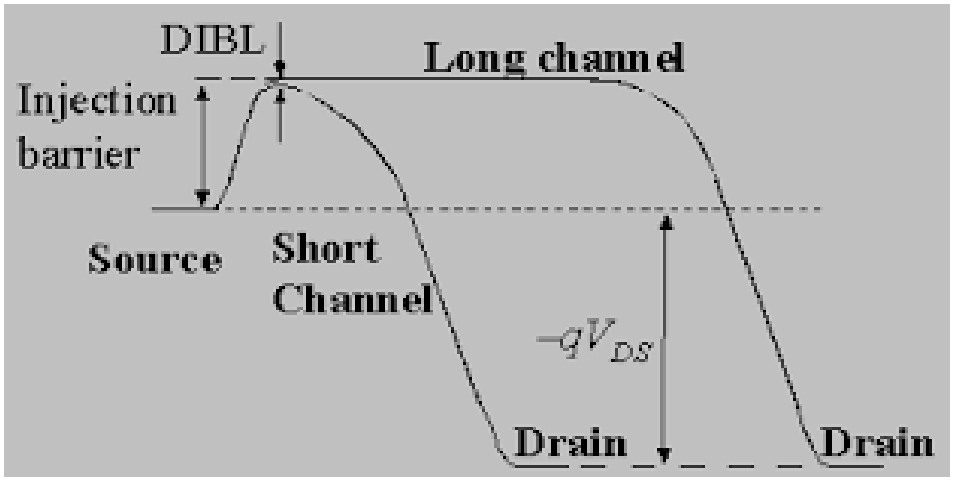


Figure 1.4 DIBL Effect

Therefore, the threshold voltage gets reduced by increasing the drain voltage for short-channel transistors. This shortening of threshold voltage at higher drain voltages is known as threshold voltage lowering or DIBL. The DIBL effect can be estimated by calculating the threshold voltage as a function of two different drain voltages.

$$DIBL = -\frac{{V_{TH}}^{DD} - {V_{TH}}^{LOW}}{V_{DD} - {V_D}^{LOW}} \tag{1.1}$$

${V_{TH}}^{DD}$ is the threshold voltage at a higher drain voltage and ${V_{TH}}^{LOW}$ is the threshold voltage at low drain voltage. V_{DD} is the high drain voltage and ${V_D}^{LOW}$ is the low drain voltage.

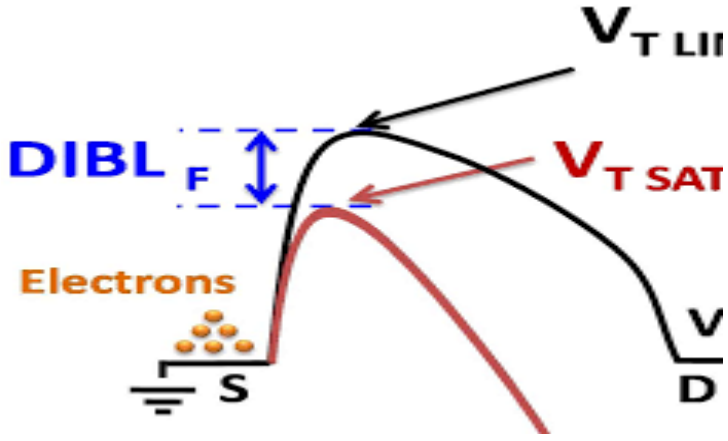


Figure 1.5 Threshold voltage and DIBL calculation

Figure 1.5 shows the calculation of threshold voltages at different drain voltages. By computing the threshold voltages at low and high drain voltages, DIBL can be calculated to check the effect of variation of threshold voltages on the performance of

the device. DIBL is measured in mV/V. The threshold voltage is reduced due to barrier lowering results in the increased leakage current of the device.

1.6.2 Sub-threshold Leakage

When the gate voltage of MOS is less than the threshold voltage, the MOS transistor is in cutoff mode and $V_{GS}<V_t$, the minority carriers (hole in the case of the p-type substrate) flow from source to drain in a weak inversion region. This leakage current occurs because of the reduced potential barrier between source and drain. As the supply voltage is reduced to decrease the dynamic power dissipation as well as to possess the low electrical field in the device, sub-threshold leakage increases [13]. Due to the accumulation of holes under the gate, the channel is partially created between the source and drain. A small current flow is called sub-threshold conduction in a weak inversion region due to minority carriers. MOSFET is in the area of weak inversion i.e. the channel is not inverted [14]. The drain current is almost zero in this region below the threshold voltage. There is a sub-threshold current that is exponentially dependent upon threshold voltage. Sub-threshold current is undesirable in digital circuits generally causes leakage in an off state. Sub-threshold leakage is one of the main causes of static leakage that contribute to the dissipation of static power [15]. The sub-threshold current arises whenever the gate-to-source voltage is less than the threshold voltage in the cut-off region, i.e. when the transistor operates in the weak inversion region.

1.6.3 Punch-Through

When the depletion layers formed around the drain and source regions join with each other causes punch through effect in MOSFETs. The drain current starts increasing due to the high electric field below the gate with the rise of a drain to source voltage. This increased drain current will increase the output conductance and confines the maximum operation of the device. The usual operation of MOSFET has not occurred and a sharp increase in drain current causes a device to permanent damage.

1.6.4 Hot Electron Effect

Electrons and holes with high kinetic energy (called hot carriers) are introduced into the gate oxide due to the increased electric field in the pinch-off region and lead to permanent shifts in the oxide interface and degrades the device's current-voltage characteristics. The hot electron effect is shown in Figure 1.6

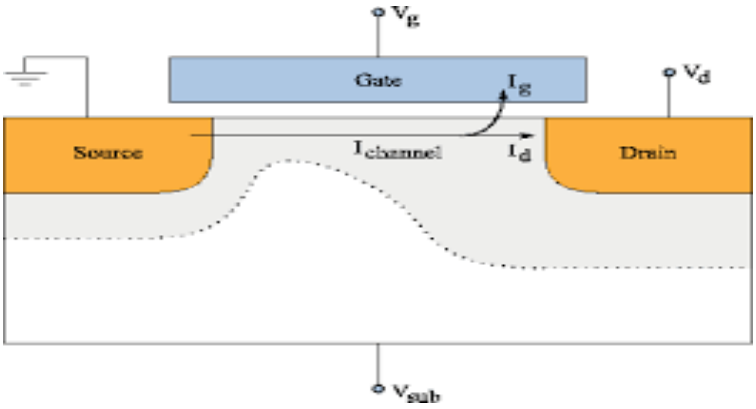


Figure 1.6 Hot Electron Effect

1.6.5 Dielectric Breakdown

When the gate oxide thickness is scaled-down and a thin oxide function at the high electric field then it will degrade the performance of the gate oxide after a while. It may breakdown and leads to permanent damage to the device.

1.7 REMEDIES TO SCALING PROBLEMS

1.7.1 Alternate Dielectric Materials

The scaling of gate oxide thickness along with channel length of MOS transistors gives rise to an increase in undesired gate leakage current. To avoid this type of leakage high-k materials are recommended to replace low k materials as a Gate oxide material. High k materials with their high permittivity can provide lower equal oxide thickness required to reduce tunneling current at higher physical thickness. The use of High k dielectrics is the solution to reduce the dielectric breakdown of the gate oxide [16]. To overcome the physical limits of transistor scaling, high-k dielectric oxides were used to replace the widely used silicon dioxide (SiO_2) gate dielectrics. High-k dielectric gate thickness affects threshold voltage (V_{th}) and off-state leakage current (I_{OFF}). A device with a high drive current (I_{ON}) and low I_{OFF} results in a high on-off current ratio (I_{ON}/I_{OFF}) resulting in faster switching speeds for the N-type Metal Oxide Semiconductor Field Effect Transistor (NMOS). The equivalent oxide thickness (EOT) of a material is defined as the SiO_2 layer thickness required to achieve the same capacitance density as the high-k material. EOT is given by:

$$EOT = \left(\frac{3.9}{k}\right) * t_{ox} \quad (1.2)$$

where t_{ox} is the gate oxide thickness, k is a dielectric constant of the oxide. High k materials are formed by the deposition technique of fabrication. The choice of high k

material for a particular device is a big challenge. There are various high k materials listed below in Table 1.1

Table 1.1 High k materials and their properties

Material	Eg(eV)	K-value	ΔEc(eV)	ΔEv(eV)	Stability with Si	Crystal structure
SiO_2	9	3.9	3.5	4.4	Yes	Amorphous
Si_3N_4	5	7.5	2.4	1.8	Yes	Amorphous
Al_2O_3	8.7	8.5-10.5	2.8	4.9	Yes	Amorphous
TiO_2	3-3.5	30-100	1.2	1.2	Yes	Tetragonal
La_2O_3[73]	4.3	27	2.3	0.9	Yes	Hexagonal, Cubic
HfO_2	5.7	30	1.5	3.4	Yes	Tetragonal
ZrO_2	5.8	25	1.4	3.3	Yes	Tetragonal
Gd_2O_5	5.4	12-23	3.2	3.9	Yes	Amorphous
$LaGdO_3$	5.6	22	2.57	1.91	Yes	Amorphous

A high k material can be chosen based on the requirement of the device performance [17]. Similarly, Poly gates are replaced by metal gates. The device with a high k gate oxide and metal gate can give an improved performance as compared to low k gate oxide and polysilicon gates. It gives improved sub-threshold swing due to which ON-OFF switching will be fast. It also gives a higher ON/OFF ratio.

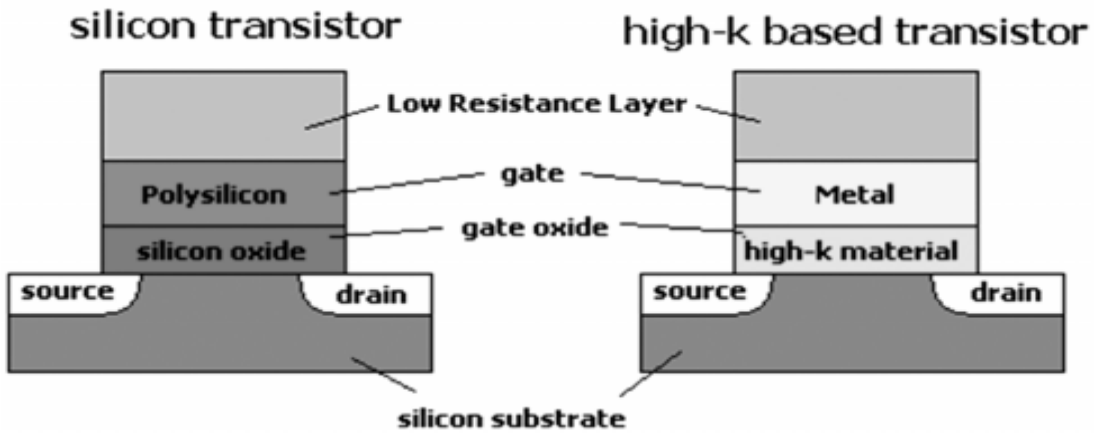


Figure 1.7 Replacement of SiO_2/Polysilicon gates with High-k/metal gates

Figure 1.7 shows two different devices having SiO_2 with Poly-silicon gates and the second device shows with High-k with metal gates.

1.7.2 Alternate Gate Materials

SiO_2 has been used as an effective dielectric gate since the advent of MOS devices over 40 years ago. The need for the enhanced velocity at stable power density has resulted in a reduction in MOSFET sizes and the oxide thickness is also lowered in step according to the scaling rules. Gate electrode is also one of the primary problems associated with the scaling process. It is not possible to use poly-silicon commonly used for gate electrodes for devices below 70 nm. This is because doped poly-silicon demonstrates load depletion impacts at greater voltages which decreases the gate capacitance of devices produced particularly with thicker dielectric systems. For devices in the nanometer scale, the metal gate electrodes are chosen over poly-silicon. The benefits of metal gate electrode over poly-silicon gates are reduced gate resistance and desirable function setting. For compatibility with standard high-temperature CMOS processing, thermally stable metal electrodes are needed.

1.7.3 Alternate Implants

Integrated circuit chips have different fabrication steps from crystal growth to metallization of the device. Different patterns are created and different layers are placed upon each other having insulating layers between them. Every layer is deposited or diffused on the surface of the wafer having defined temperature, time and doping concentration [18]. There are various parameters at different steps that can be altered during fabrication to enhance the performance of the device [19]. Various implants can be incorporated into the device to reduce short channel effects. The various types of implants are given below:

(a) Halo implant

There is a chance in the short channel MOSFET for the space charging areas (SCR) connected with the source and drain to come near to each other. This creates the so-called punch-through effect. This effect can be suppressed by Halo doping as shown in Figure 1.8. Halo dopings i.e two heavily doped (p^+ in NMOS and n^+ in PMOS) are deposited nearby the drain and source in the substrate so that the halo doping of drain overlaps with the halo doping of the source and increasing the substrate concentration in the channel as well the threshold voltage. The use of halo doping also results in reduced Punch through. If the concentration of the substrate is increased, it also results in an increased sub-threshold swing. Halo implants are used to adjust the threshold voltage to get a high I_{ON}/I_{OFF} ratio so that a good signal to noise ratio can be achieved.

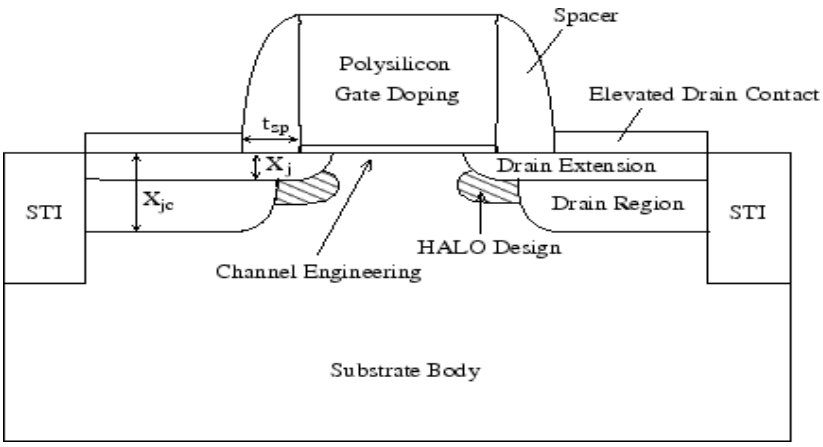


Figure 1.8 Halo Implant

(b) Source/Drain Implant

Source/drain doping concentration can be adjusted to diminish the leakage current of the device. Deep source/drain implants are usually used to decrease series resistance and provide an excellent contact interface. It is also used to regulate the threshold voltage of the device.

(c) Substrate Doping

By increasing the total doping concentration of the bulk, Punch through effect can be minimized. Due to increased doping concentration, the drain/source depletion regions will grow into smaller regions and will not form a parasitic current path. Earlier the devices are fabricated on heavily doped substrates. MOSFETs fabricated on lightly doped substrates give improved drain current and improved substrate current which initiates a new concept in the integrated circuit design area.

(d) Threshold Voltage Implant

Threshold voltage deviation is one of a CMOS technology's major analog performance indices as it controls the precision-speed-power trade-off of the fundamental analog construction blocks. The essentially reduced voltage threshold deviation is mainly due to modifications in the doping of the substrate. Complications result in obtaining the accurate transistor threshold voltage (V_{th}) value and also controlling the gate leakage current to an appropriate level. The DIBL scaling effect can be reduced by proper scaling of drain and source depths, improving sub-threshold swing, increasing the substrate doping concentration and reduction of gate oxide thickness [20]. There are various ways to increase the threshold voltage at reduced channel length. The increase

in threshold voltage can reduce the DIBL effect in MOSFETs. By adjusting the threshold voltage implant concentration, the threshold voltage of the device can be adjusted depending upon the requirement of the device [21]. The channel implant can be used to increase the threshold voltage of the device.

1.7.4 Alternate Channel Materials

The scaling has continued unchallenged for about five decades brought new difficulties to device and process engineers. Changes in processing techniques and the introduction of new materials and device architectures have resolved many of the difficulties in the device concentrations [22][23]. Silicon on Insulator (SOI) is one of those architectures that IBM launched. It is predicted that by decreasing power consumption and enhancing the device's transient response, the substrate current can be reduced [24]. Highly susceptible to ionizing radiations and cosmic rays are conventional semiconductor devices. These radiations can cause the generation of electron-hole pairs in the silicon substrate and thus cause a large leakage current. This not only causes an increase in static power dissipation but can also alter the information stored in memories of semiconductors popularly known as single event upset. The presence of the BOX layer in SOI prevents the radiation effects of devices and circuits. SOI is therefore considered the best candidate for space apps rather than the conventional candidate. Silicon on Insulator (SOI) MOSFET is a semiconductor device in which a silicon layer is fabricated on a buried oxide layer (BOX) formed on a silicon substrate instead of conventional silicon substrate devices [25]. A buried oxide is sandwiched between the silicon substrate and silicon junction. SOI device is preferred due to reduced substrate current, lower parasitic capacitance, reduced power consumption and better transient response of the device, better yield, reduced antenna issues, Latch-up reduction, and low leakage currents. There are two types of SOI MOSFETs: PDSOI (Partially depleted SOI) and FDSOI (Fully depleted SOI). In PDSOI MOSFETs, the buried oxide layer is very large and almost behaves like a bulk MOSFET [26]. In FDSOI MOSFETs, the buried oxide is very thin so that the depletion region covers the whole film.

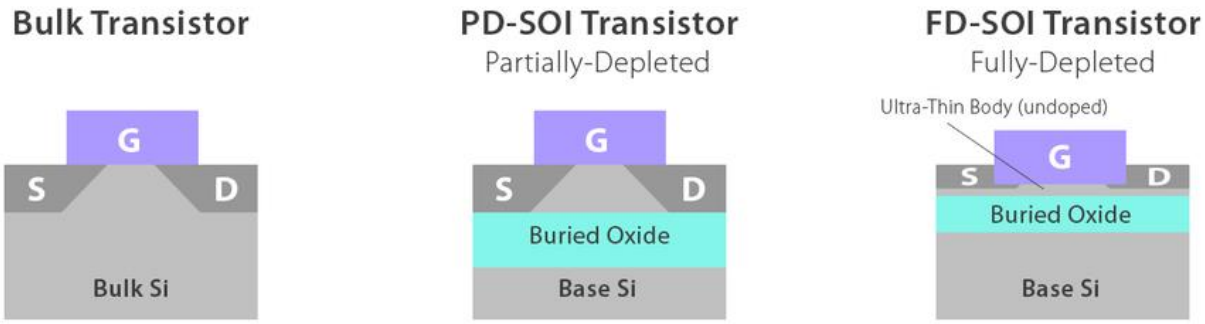


Figure 1.9 Bulk transistor and SOI types

Figure 1.9 shows the structures of the bulk transistor, PD-SOI, and FD-SOI transistor.

SOI is further used as a base device for Multi-gate Transistors and Graphene-based transistors to reduce the short channel effects. Scaling of conventional bulk MOSFETs has been done continuously until 2018 to endure Moore's Law. Due to the scaling of conventional transistors, several short channel effects arise resulting in degradation of the device's performance. It is very necessary to find out an alternative to reduce short channel effects for enhancement of the device. According to ITRS, 2004 first consideration is transport enhanced FETs which improves the carrier mobility and current drive. The second consideration is to have ultra-thin body SOI (UTB SOI) FETs. The third consideration is source/drain engineering FETs and the last consideration is multiple gate FETs. The research of ultra-thin body (UTB) SOI MOSFETs [27] has increased the chance of replacing the conventional MOSFETs at 45 nm technology node and beyond. UTB SOI is the extension of FDSOI. The major difference between SOI and UTB-SOI is the silicon layer thickness. In UTB-SOI MOSFETs, the silicon layer thickness, $t_{si} \leq$ 10nm. Scaling can be further performed at lower technologies i.e at 32nm, 22nm, 15nm, 10nm and 5nm with UTB-SOI devices. The threshold voltage of the device can be adjusted to obtain a low leakage current with appropriate work-functions for the gate materials [28]. The channel doping concentration ($10^{15}/cm^3$) in UTB-SOI devices is very small compared to conventional MOSFETs ($10^{18}/cm^3$), resulting in enhanced mobility and carrier speed in the devices. Hence, the use of low channel doping in these type of devices gives high-performance devices.

Graphene- Silicon on Insulator (G-SOI) is a field-effect transistor that has a lightly doped graphene channel between source and drain. The structure of G-SOI is shown in Figure 1.10 below.

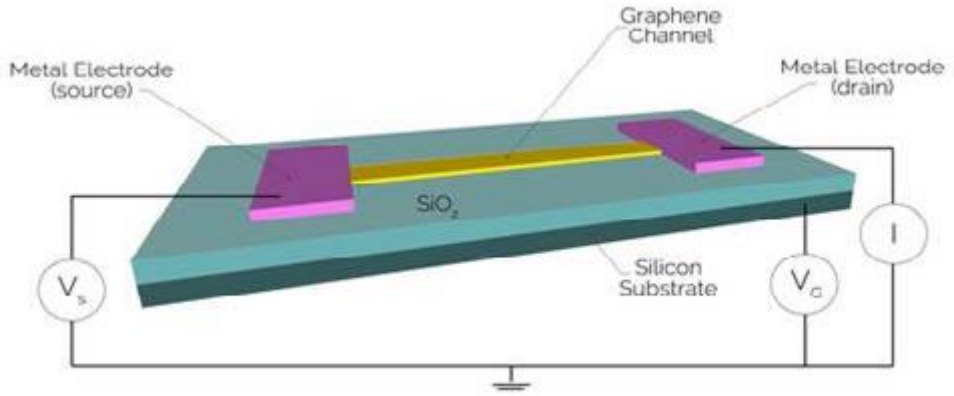
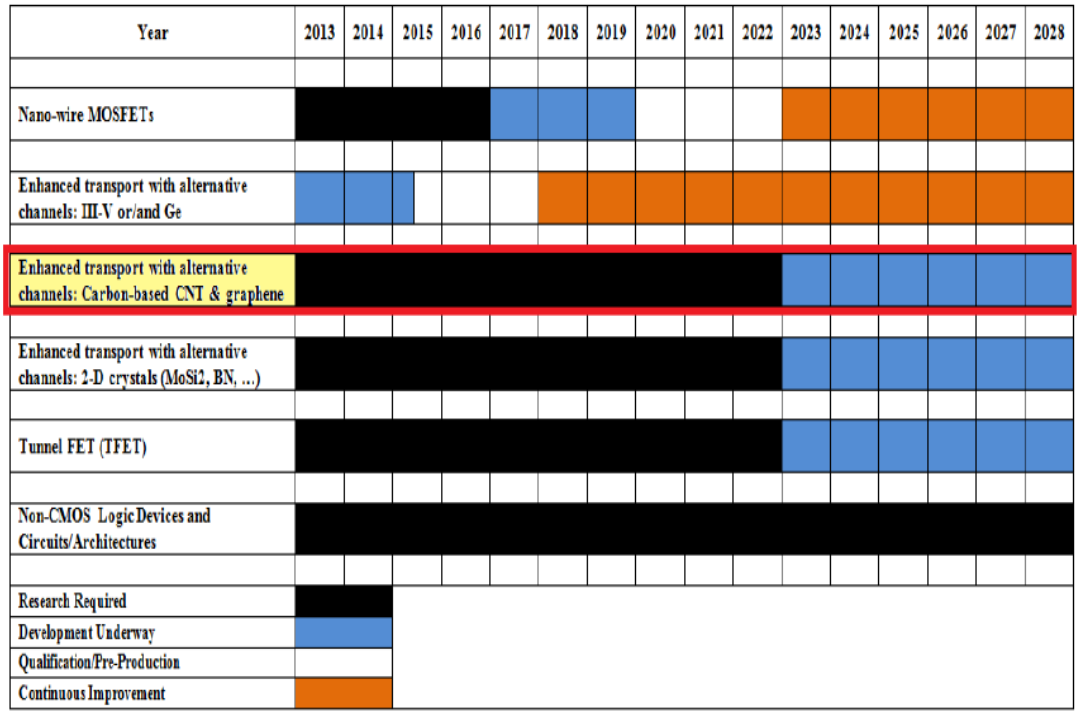


Figure 1.10 G-SOI Structure

G-SOIs are used in photo-sensing, magnetic sensing, bio-sensing, and environmental sensors. Graphene, a two-dimensional, zero-gap material is replacing bulk semiconductors nowadays. In three-dimensional MOS devices, the change in electric charges on the surface of the channel does not penetrate deeper into the device whereas, In G-SOI, graphene is one carbon atom thick, the entire channel surface can be exposed to any molecules in the channel [29]. When the silicon thickness is decreased due to scaling, several surface defects will occur which limits the overall sensitivity of the device whereas graphene can be produced in a single layer with more accuracy [30]. Hence, graphene is more efficient than silicon. Graphene has greater mobility than standard MOSFETs equal to 1000,000 $cm^2V^{-1}s^{-1}$. G-SOIs are manufactured with metal contacts on Si/SiO_2 substrates. The graphene material is deposited on the surface of the wafer by chemical vapor deposition (CVD). It is easy to fabricate on a wafer rather than silicon material. It is free from metallic contaminants, cracks, holes or residues. According to the ITRS report, 2013 Carbon-based CNR and graphene-based devices [31] have a great scope in research in coming years in continuation with Nano-wire MOSFETs as shown in Table 1.2 below.

Table 1.2 ITRS report 2013



1.8 MODELING APPROACHES

Modeling is important before manufacturing to check the functionality of an integrated circuit (IC). To achieve these goals, a novel generation of the Predictive Technology Model is presented for conventional CMOS technology. The predictive technology model of bulk CMOS is effectively created down to the 12 nm node based on a set of necessary device models and early-stage silicon statistics. With reported silicon data, the precision of PTM predictions is thoroughly checked: I_{ON}'s error is less than 10 percent for both NMOS and PMOS devices. PTM can be readily tailored to produce a broad variety of process unreliability by regulation of some main model parameters. Besides, PTM captures the vulnerability to process variations properly [32]. Analyzing a huge number of accessible Metal-Oxide-Silicon Field-Effect-Transistor (MOSFET) models, understanding them and comparing them for their pros and cons has become crucial [33][34]. When the complexity of these models becomes very big the job becomes similarly hard. Various MOSFET modeling approaches are:

(a) Charge Based MOSFET Models

One of the fundamental and primitive modeling methods is the charging-based modeling method. It is based on the calculation of the MOSFET channel inversion charge density in the context of supply voltages i.e. gate and drain voltage [35]. These

models are applicable in the SPICE circuit simulator's original version. These are also referred to as models based on threshold voltage as they are based on identifying all threshold voltage based parameters such as drain current, drain voltage, etc. The main benefit of this strategy is its simplicity and flexibility in introducing characteristics arising from advances in technology. These models are divided primarily into the first generation, second generation and third-generation models depending on their complexity level. The SPICE Level 1, Level 2, Level 3 models are called SPICE Models of the first generation.

(b) Potential Based MOSFET Models

The potential-based model method is based on the defined physics of the MOSFET device and is more precise than the designs depending upon the charges. Additionally, as the scaling [36] remains to the Nano-scale region, the charge-based models grow to even more inaccurate in lower geometries because these models are dependent on threshold voltage that cannot be scaled down beyond a certain limit. The I-V and C-V characteristics are explored by calculating the potential in a MOSFET channel.

(c) Conductance Based MOSFET Models

These types of models are appropriate for analog design applications with low power and short channel. It is well-known as the EKV (Enz-Krummenacher-Vittoz) model created by the Federal Technology, Institute of Switzerland. This model maintains the substrate as the reference in the place of the source as stated in the models based on potential and the charge models. It is very less used due to its higher complexity.

(d) Quantum Based MOSFET Models

Due to the destructive scaling of MOSFETs, the gate oxides are also scaled down to a particular value to meet the device requirements in the nanometer scale. The substrate doping is also required to be increased to avoid short channel effects. This results in an increase in the electric field in the silicon/silicon dioxide interfaces and gives a very steep potential curve. The energy of electrons is quantized and occupies discrete energy levels. The precise modeling of energy quantization in MOSFETs needs some other accurate models which provide the solution of Schrodinger and Poisson Equations. Quantum models are preferred to study this type of behavior of the MOSFETs. One-

dimensional and two-dimensional quantum models are used to get voltage-current and capacitance-voltage curves.

1.9 VLSI DESIGN FLOW

To manage the quickly growing complexity of the design, various computer-aided design (CAD) tools are generated. A VLSI Design flow is shown in Figure 1.11 below.

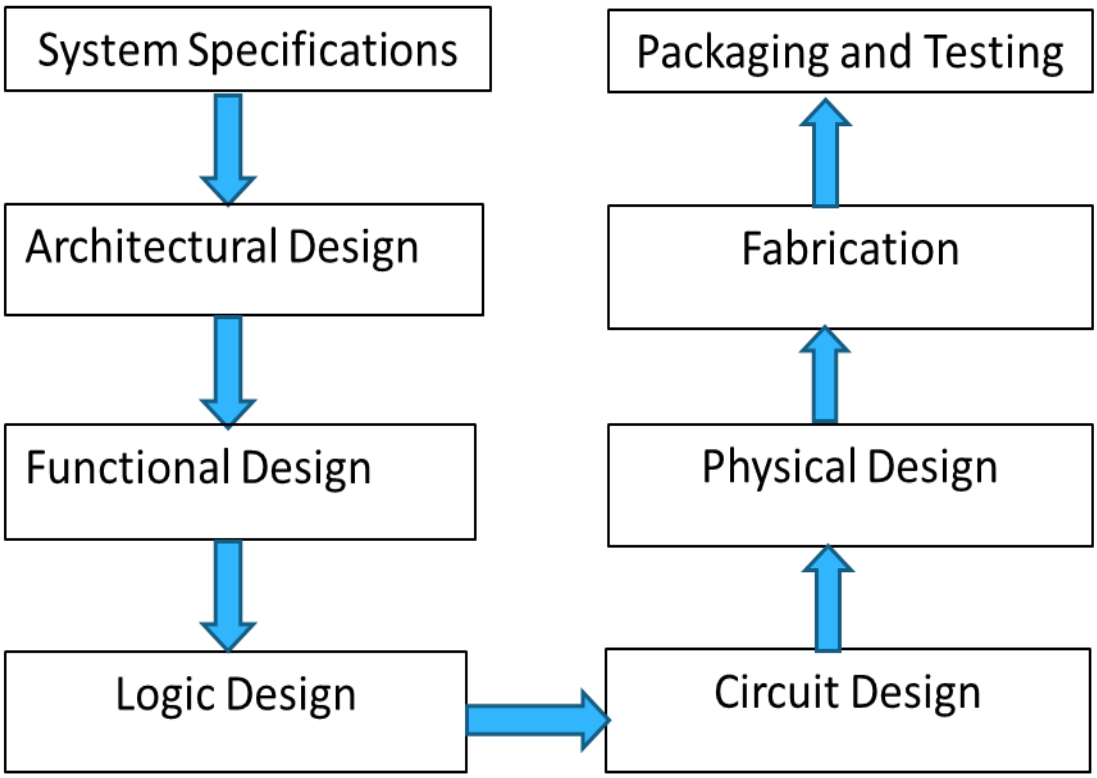


Figure 1.11 VLSI Design Flow

The chip design involves various processing steps to accomplish the entire flow. A specialized EDA tool is needed for every step of the design process. The first step is to bring up the system's design specifications. In this process, different design parameters i.e. chip size, speed, power and functionality are to be considered. It is the interface between market requirements, technology and economic sustainability. After the specifications of the design are specified, the architecture of the proposed system is designed. The simulation and verification of the logic design based on architecture have been performed to check the correctness of the design. The circuit is designed based on logic to verify the correctness and the timing analysis of the design. The netlist is generated after the simulation of the circuit which specifies the gates, macros,

transistors and their interconnections. After the schematic entry, simulation and netlist generation, the layout is created to convert the netlist to a geometric representation. A design rule check can be done to check the design rules of the design. The design is ready for the manufacturing process after the layout and verification. Layout data is converted into photo-lithographic glass masks so that the masks can be transferred to a silicon wafer. The fabrication process consists of crystal growth, oxidation, photolithography, doping, and metallization. Finally, the wafer is fabricated and diced into several individual chips by a diamond saw or other method. Each chip is packaged and tested to check the design specifications and proper functionality

1.10 VARIOUS CAD TOOLS

There can be millions of transistors on a tiny piece of silicon in a modern-day IC. Of course, without computer aids, the manufacture and design of these ICs cannot be performed. Electronic Design Automation (EDA) tools involve both the manufacture and design of these ICs. Highly accurate software tools are needed to analyze and simulate embedded circuit design and manufacturing. Lots of research have been performed on these problems and are still going on.

The whole work is done to accomplish this research work is performed in SILVACO TCAD Tool. ATHENA offers a platform for the simulation of ion implantation, diffusion, etching, deposition, lithography and oxidation of semiconductor materials. ATLAS simulates semiconductor electrical, optical and thermal behavior [37]. ATLAS is a two and three-dimensional device simulator based on physics that analyzes the electrical behavior of semiconductor devices under defined bias conditions. ATLAS uses the physical structures that are simulated with ATHENA as input [38]. The combination of ATHENA and ATLAS enables the effect of process parameters on device features to be determined. Many simulations of the ATLAS tool are using two input files. The first input file is a text file containing ATLAS executable instructions. The second input file is a configuration file describing the simulated structure. ATLAS generates three kinds of output data. The first component of the output file is the runtime data which gives you feedback and alerts and error alerts as the simulation continues. The output file's second form is the log file which contains all supply voltages and currents for system analysis. The third type of output file is the suggestion file which holds the values of solution parameters in the system at a given

bias point 2D and 3D. The ATLAS inputs and Outputs flow is shown in Figure 1.12 below.

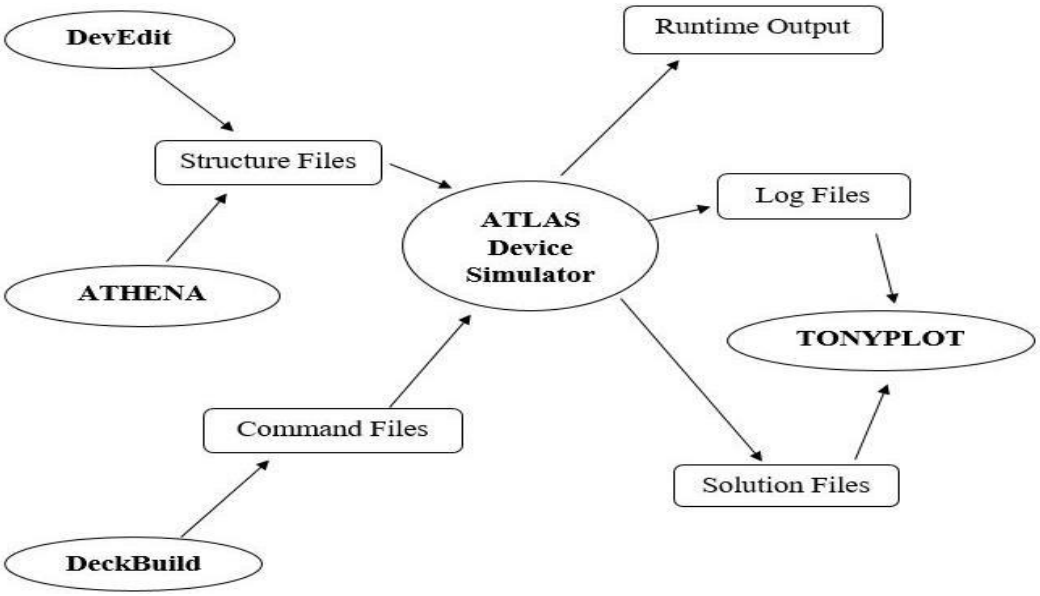


Figure 1.12 ATLAS Inputs and Outputs

ATLAS device simulator can have inputs from DECK BUILD; structure files from DEVEDIT and gives output in the waveform viewer TONYPLOT and log files. The ATLAS design flow is given below in Figure 1.13

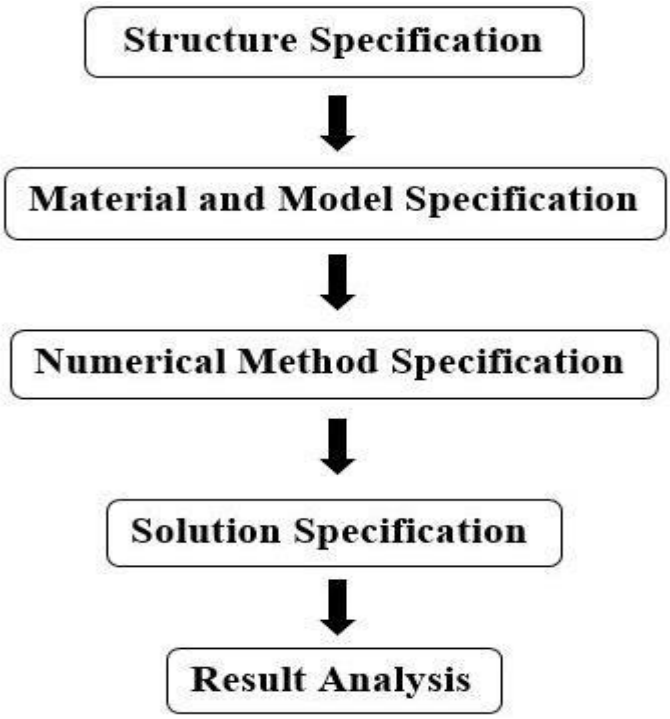


Figure 1.13 ATLAS Design Flow

There are mainly three types of materials viz semiconductors, insulators and conductors. Each category needs to specify distinct parameters. These characteristics include electron affinity, band-gap, and electron density and saturation velocity for semiconductors. Standard material specifications are utilized for many components in device simulation.

The sequence in which statements are inserted in an input file of ATLAS is significant. There are five classes of statements that need to be carried out in the correct order. Unable to do so generally results in an error message that may result in an incorrect or terminated function of the program. For example, if the parameters or models of the material are placed in the wrong manner, then the calculations may not use them. The order of statements is also important while doing mesh creation, structural definition, and solution sets. Failure to put these statements in order may also result in the program being operated incorrectly or terminated. A device structure can be described for use in ATLAS in three distinct respects. Reading a current framework from a file is the first way. Previously generated ATLAS program or any other program designed in ATHENA or DEVEDIT creates the framework [38]. A MESH declaration loads the mesh, geometry, position of the electrode and structure doping. The specification of the framework involves the definition of mesh for the structure and doping of electrodes. Then modeling of any device intended in SILVACO is indicated for models. It describes the material characteristics of a contact interface etc. A specific technique has to be specified after the mathematical model has been established to operate the design by selecting the numerical method. A log file is produced with simulated outcomes after simulation. TONYPLOT displays the final waveform. The parameters are extracted in result analysis e.g threshold voltage, drain current, sub-threshold swing, etc.

1.11 MOTIVATION OF RESEARCH

Integrated circuits (IC) technology has undergone immense technical and economic progress. The main engine powering the electronics journey is "miniaturization." It is becoming a massive challenge in increasing speed and density in the semiconductors industry since the invention of the first calculation devices. Optimizing MOSFETs is a challenging job for digital and analog circuits due to contradictory device performance needs [39] [40]. In logic applications where the trade-off is governed by the I_{ON}/I_{OFF} ratio, the task is to minimize off-current while reducing intrinsic delay and maintaining high ON current. Cutting speed, intrinsic gain, linearity, noise and device mismatches

are the performance metric for RF and analog circuits. The gate length was one of the most critical parameters directly related to CMOS scaling. When MOSFET devices are miniaturized, several complications results. As the length of the channel decreases, several effects alter the quality of MOSFET devices. Reduction of threshold voltage, DIBL, Hot carrier effect, mobility degradation, velocity saturation, channel length modulation, and Punch-through are the various effects that occur due to scaling. The presence of these effects in existing devices due to scaling in MOSFETs is the motivating factor to do research work to reduce these types of effects so that performance due to miniaturization is not degraded. The motive of this research work is to develop various techniques to enhance the performance of the device.

1.12 OBJECTIVES

The following are the objectives of the research work:

- To study and perform the virtual fabrication of Nano-Scale devices.
- To analyse the impact of various design parameters such as gate oxide thickness, halo doping, threshold implant concentration, substrate doping, source/drain doping on the performance of the device.
- To analyse the extraction of various parameters such as Sub-threshold leakage current, drain current, Substrate current, ON current, ON/OFF ratio, device capacitance, etc. of MOSFET using various doping profiles.
- To investigate the effect of the work-function of gate material on device performance.
- To design and simulate an SOI device with high k oxide material and metal gate.
- To design & simulate Graphene-based Transistor

The whole proposed work related to modeling, analysis & simulation has been done using SILVACO TCAD & various other tools

1.13 RESEARCH METHODOLOGY

The purposed work is done by using ATHENA and ATLAS SILVACO software as shown in the flow diagram given in Figure 1.14 below. The Design, fabrication and comparative analysis of various devices have been done to improve the performance metrics of the device.

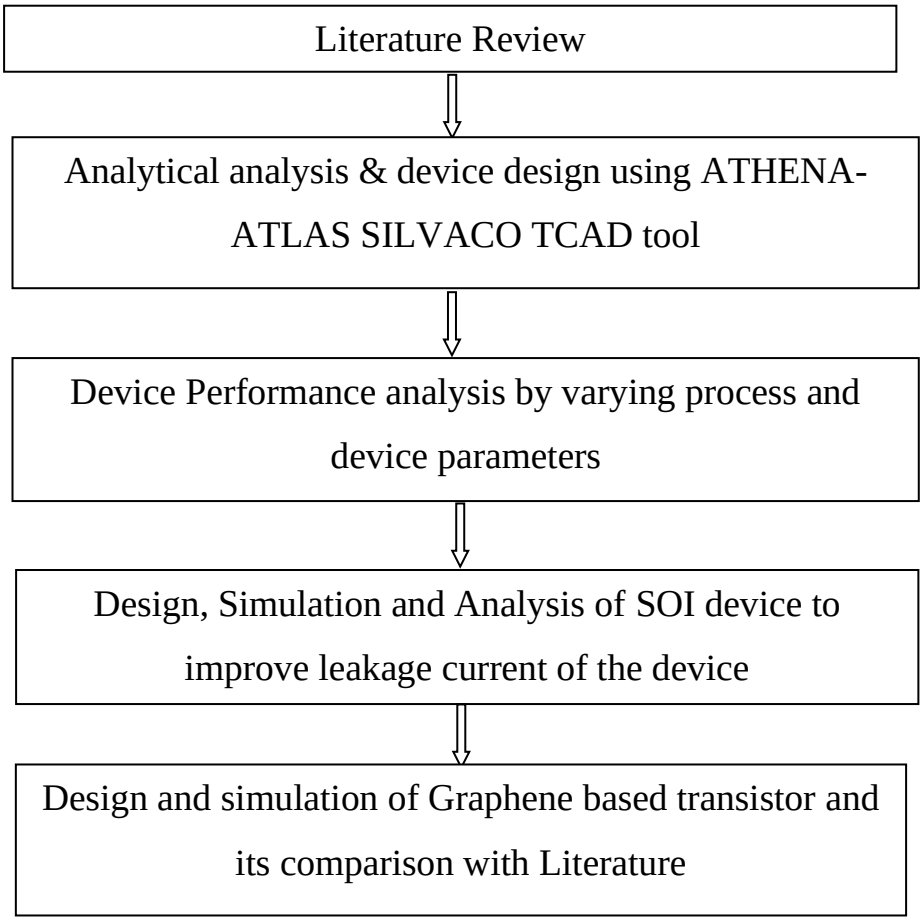


Figure 1.14 Flow diagram for Research Methodology adopted

1.14 THESIS ORGANIZATION

This thesis is organized into seven chapters. A detailed view of all the chapters is given below:

Chapter 1 Introduction

A detailed review of existing devices on various technologies and their related parameters is presented. The solutions to various problems beyond the 50nm channel lengths are explored. The main motive is to formulate the problem in existing devices concentrating on drain current, off-state leakage current, sub-threshold slope and

substrate current of the device. In this chapter, the objectives of the thesis are also discussed.

Chapter 2 Literature Review

This Chapter provides a survey of existing MOSFET scaling and short-channel effects research and present problems. This chapter along with the scaling theory also describes the physics behind the issue. The main sources of variation will then be discussed outlining their impacts on device and circuit efficiency. It presents the conventional existing MOSFET structures, enhancement techniques and recent trends to enhance the performance of the device.

Chapter 3 Modeling and Simulation Methodology

Running real experiments in semiconductor fabrication Labs is both time-consuming and expensive. The use of TCAD tools reduce the development cost and shorten the development time. It is often more cost-effective and time-efficient to substitute simulated experiments for some of the real-world experiments. The device is initially designed and virtually fabricated using SILVACO ATHENA and ATLAS tools. The mathematical expression of surface potential and the threshold voltage is also being derived.

Chapter 4 Electrical Characteristics of Novel Silicon MOSFET

This chapter describes the design, simulation and analysis of NMOS and PMOS devices based on various extracted or simulated parameters. Initially, NMOS and PMOS devices have been designed, virtually fabricated and simulated. Various device design parameters (threshold voltage, drain current, sub-threshold current, substrate current, linear threshold voltage, and DIBL) have been extracted and reported in this chapter. Further, the device with the variation in substrate doping is designed. Two devices have been designed with lightly doped and heavily doped substrates and the comparison of both the devices has been done. The analysis of the device with Gaussian and Pearson Doping Profiles has been reported in this chapter.

Chapter 5 Performance Analysis of the SOI MOSFET

The persistent scaling of MOSFET dimensions worsens the performance of the device and allows the innovation of new devices such as Silicon-on-Insulator (SOI) with modified structures. In this chapter, the surface potential of dual material SOI MOSFET is analytical estimated and compared with the simulated results. Also, the dual-material single halo and dual-material dual halo structures are being designed & simulated to reduce the device's leakage current.

Chapter 6 Characterization of G-SOI MOSFET

An NMOS device with a channel length equals to 10nm has been designed. Initially, 10nm G-SOI was designed using the silicon channel. Then the Silicon material in the channel is replaced with Graphene which gives a high ON current. Further, the SiO_2 substrate is replaced with h-BN material which gives high ON current as well as low leakage current as compared with other devices. Finally, a new high k material $LaGdO_3$ is introduced here to enhance the performance of the device.

Chapter 7 Conclusion and Future Scope

This chapter gives the conclusion and future scope of the work done.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

Due to its exceptional scalability, over the past centuries, CMOS technology on silicon substrates has been the prevailing technology for the design of integrated circuits. This form of system is required to proceed to the 10 nm process. The scaling patterns of design metrics such as threshold voltage and oxide thickness need to be examined in order to effectively determine the attributes of prospective bulk CMOS; their interaction with the determination of significant product attributes should be well integrated for precise design prediction. The continuous scaling of CMOS technology has increased in latest years and is likely to continue in the direction of the 10nm process [30]. Physical variables that had a very small effect on the performance of the digital or analog circuits in the Nano-meter age are now becoming more and more important. Specific examples involve process deviations, mobility degradation, and power consumption. To predict future technology features, an adaptive strategy would necessarily scale down the physical dimensions and supply voltages of today's technology.

This chapter provides a detailed study of current MOSFETs, scaling needs, scaling problems and managing short channel effects. Identifying and analyzing various leakage sources is therefore very significant for the estimation and reduction of leakage power, especially for low-power applications. Different device efficiency methods are discussed by changing process variations, modifying materials and modifying device architecture. Recent trends to limit sub-threshold conduction and DIBL to obtain higher drain current and ON/OFF current ratio is discussed to improve MOSFET's efficiency.

This literature review's technical content is categorized into four parts. The general introduction to this research is given in Section 2.1. Section 2.2 gives its benefits and constraints to the implementation of standard MOSFETs. Section 2.3 introduces the methods for improving devices using high k materials and highlights metal gates. In the last, the current developments include various channel materials.

2.2 CONVENTIONAL MOSFETS AND SCALING LIMITS

The reduction of threshold voltage, channel length and oxide thickness results in high leakage current in micro-meter devices which are the major contributor to the CMOS circuit power dissipation. Numerous intrinsic leakage mechanisms for transistors are discussed including weak inversion, drain-induced barrier lowering (DIBL), gate-induced drain leakage (GIDL) and gate oxide tunneling. Channel Engineering techniques like retrograde well and halo doping were described as a way of controlling short-channel effects for continuous CMOS scaling. Various circuit techniques are discussed to diminish power consumption. Subthreshold and gate leakage in existing deep-sub micro-meter devices with small threshold voltages have become important sources of leakage and are anticipated to grow with technology scaling. In addition, additional leakage currents in advanced CMOS devices i.e. GIDL and BTBT can also become an issue. To control the leakage in micro-meter technology circuits, process technology and circuit-level solutions for leakage reduction need to be pursued. At the process technology stage, retrograde and halo doping well-engineering techniques are used to minimize leakage and boost short-channel features. In high-performance logic and memory designs, transistor stacking, multiple, linear, multiple, and dynamic techniques can effectively reduce the leakage current at circuit level [41]. Moore's Law and the International Technology Roadmap for Semiconductor Technology are discussed here. Both ITRS and Moore's Law played an important role in the progress of CMOS technology. In general, the road map was an important guidance document that provided guidelines for research and development for next-generation devices. In addition to their role as a driving force behind the development of semiconductor technology as a whole, the focus is on their influence on the scaling of MOSFETs. Application-dependent power constraints (including leakage currents), fundamental parameter variations, and the problem of ultra-thin gate dielectric material quality are among the main scaling limiting factors that will in the near future threaten Moore's Law. The simulation approach and overall technique to investigate scaling and fluctuation of intrinsic parameters in Nano CMOS devices are presented here [42][36]. The scaling of traditional MOSFETs and the limits and challenges faced by the semiconductor industry to maintain and expand the rule of Moore until 2018 (end of the present roadmap). It was noted that traditional transistors with gate lengths of 18nm, 13nm and 9nm are becoming increasingly difficult to design due to severe short channel

effects, gate oxide tunneling, power dissipation, intrinsic parameter fluctuations and the causing loss of performance. It is therefore very important to consider alternative device architectures that do not have some of the drawbacks of traditional MOSFETs and which can be realized with limited process technology changes. The last two editions of the ITRS, therefore, cover in great detail new testing tools and technologies. At the same time, it focuses on scientific communities and the microelectronics industry to accelerate non-classical FET research and innovation. The Closed-form 2D Modeling of MOSFETs deep-submicron and sub-100 nm is explored using a conformal mapping method where the 2D Poisson Equation is partitioned into a 1D long-channel situation and 2D Laplace Equation in the depletion regions [15]. One of the issues with the scaling of classical MOSFETs to the sub-100 nm range is that the density of the substrate doping must be increased to 10^{18} cm^{-3} in order to include the source and drain depletion layers. However, high doping has several negative effects on the MOSFET properties such as channel mobility degradation and excessive threshold voltages. One alternative is to use a much lower doping substrate and instead ion implants a higher doping concentration under the surface. A thin layer of lower concentration of doping persists on the surface after annealing usually at a depth of less than 100 nm. The much higher doping required avoiding extreme short-channel effects and punch-through extends into the substrate for another 100 nm or so. This approach applies to both Classical and Non-Classical MOSFETs. The electrical features of the submicron system were investigated. The following parameters have been applied for constant field scaling: active channel size, ion implantation threshold voltage (V_{th}) and gate oxide thickness (t_{ox}). Other approaches used in submicron systems to avoid short channel effects included shallow trench isolation (STI), deposition of sidewall spacers, implantation of lightly doped drain (LDD), and well-implantation retrograde. The findings indicate that well retrograde implantation permitted the highest density of the dopant to drop below the surface of the substrate [43]. A lightly doped region was formed with the implementation of sidewall spacer and LDD implantation beyond the n^+ drain/source junction. Drain Current (I_D) has also risen as the metallization layers rise. The effects of variable channel size, gate insulator thickness (SiO_2), gate insulator content and temperature were analysed using computational simulations. Clearly, these simulation findings show that the carbon nano-tube MOSFETs are the best candidate for use in high-speed switching applications for optimum system parameters than the MOSFET [44].

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was the cornerstone of the development of Nano-electronics technology [45]. The scaling down of planar bulk MOSFET implied by Moore's Law was saturated due to short channel effects and DIBL. Due to this alternative approach, problem-solving was considered with reduced node technology. SOI technology has contributed to a revolution in the scaling of transistors and more volumes of packaging in the same space. [14] The invariability of early voltage and intrinsic gain from drain-bulk connected NMOS and PMOS transistors was controlled in weak inversion. It has been shown in a wide range of geometry and bias conditions for both measured and TCAD simulated systems. Early voltage and undeniable increase are given in weak-moderate inversion, which shows that these quantities are dominated by the impact of the substrate and are insensitive to bias and geometry. [16] By considering the mechanical quantity effects of the deep submicron and the nano-meter scale, a study of all MOSFET modeling approaches such as BSIM, SP and EKV. Several issues and approaches have also addressed the issue of quantum mechanical effects in MOSFET modeling. Therefore, it can be found that in all areas of its operation there is a powerful need for an analytical model that correctly describes the nanometer-sized MOSFET behavior. The electrical properties studied were the threshold voltage (V_{th}) and the current level (I_{max}). The investigation approach was performed by measuring the concentration of boron doping in polysilicon doping, adjusting impurities in polysilicon doping and also increasing the concentration of arsenic doping in source/drain annealing [18]. The doping concentration was correctly varied to obtain the ideal property of the transistor. SILVACO TCAD tools were used to obtain electrical characteristics of the NMOS device. A 90 nm NMOS has been designed and manufactured to test its electrical performance. SILVACO's ATHENA and ATLAS modules were the tools used to visualize the NMOS transistor electrical characteristics. The primary parameter analyzed was the value of threshold voltage (V_{th}) which defines whether or not a transistor is operating[46]. The thickness of the gate oxide, the features of I_D-V_{GS} and I_D-V_{DS} are also examined. The simulation result showed that gate oxide thickness, channel doping, V_{th} modification of implant and halo implantation helped to establish the curve of V_{th} and I_D-V_{GS}. From the simulation test, optimum solution is found where the values of V_{th} and t_{ox} are 0.268011V and 0.25 nm. This value corresponds to the value of International Semiconductor Technology Roadmap (ITRS). The ATLAS simulator simulates the electrical characterization of the 65 nm NMOS transistor structure and then compares it with the reported observational

results. The simulated threshold voltage was found to be 0.2V, which correlates well to the experimental value. Furthermore, there are various short channel effects such as punch-through, velocity saturation, and hot electron generation. The parameters include HALO implantation, S/D implantation, compensation implantation, SiO_2 thickness, V_{th} adjustment implant, poly-silicon thickness and silicon annealing time [47]. The experimental development of Taguchi Technique determined system parameters. Threshold voltage (V_{th}) is taken as marginal, the best effects of different variables on the S/N ratio and modification parameter Compensation Implant for NMOS threshold voltage (V_{th}) are considered because this has a large effect on the mean threshold voltage (V_{th}) but almost no effect on threshold voltage deviation (V_{th}). This study demonstrates that Taguchi Analysis can be used efficiently in the development of CMOS devices to find the ideal approach. To find a functioning transistor with threshold voltage and leakage current within the estimation of International Technology Roadmap for Semiconductors (ITRS) at this technology stage in the process. The key finding in this work is that "V_{th} adjust Implant" cannot surprisingly be used as a V_{th} modification parameter but "Compensation implant" can be used to adjust V_{th} to its target value of 0.110 V [48]. Device-level noise in the development of a sub-micron can cause serious problems with circuit incorporation. With lightly and heavily doped substrates, MOS devices are virtually developed and the substrate current is accessed for these devices. Lightly doped substrates increase noise tolerance compared to heavily doped substrates. With the aid of ATLAS, simulation of the substrate conduct is undertaken at 45 nm engineering node device for PMOS and NMOS. Substrate current is calculated for PMOS and NMOS applications for heavily or lightly doped substrates [98]. In the case of highly doped substrates, the substrate current is more intense making it less appropriate at the stage of the device. The substrate current in lightly doped substrate devices is less as compared to heavily doped devices. The lightly doped substrate devices, therefore, have greater resistance to substrate noise and devices built on lightly doped substrates have better drain properties than heavily doped substrate devices. Basically, a comparison of heavily doped and lightly doped substrates is done here [49]. The high levels of substrate doping needed in deep-sub micrometer MOS devices affect device properties strongly [92] This paper presents a technique to reduce the sub-threshold current in MOSFET by changing the doping profile in the substrate region near the channel. The size of MOSFET can be reduced but at the cost of increase in leakage of current from drain to source in its standby mode

[97]. This leakage current dissipates power even if the device is not in use. To avoid this problem, leakage must be reduced so that the advantage of reduced size may be tapped more efficiently [96]. To extract threshold voltage of MOSFET based on the widely used Constant Current Method for calculating, defining and observing the threshold voltage. Using predictive models, the threshold voltage is evaluated and simulated. This approach allows for faster development of reliable analog circuits in state-of-the-art CMOS technologies where voltage ranges are significantly small and only predictive models are active during design. In view of the necessarily limited gate overdrives in low-voltage analog architecture and the widespread use of predictive models for faster time on the market [50].

Silicide was used on the interface of the Poly-Si gate to reduce the resistance of the electrode gate. NMOS device was basically manufactured using the ATHENA module. By using ATLAS module, the electrical characterization of the device was implemented [48] [51]. The resistance of the poly-silicon layer should also be maintained as small as possible to improve the system speed by reducing the time for a transistor to turn on to accumulate charge in the channel Taguchi Method is used to predict the optimal solution to achieve the desired transistor efficiently. With reducing gate oxide thickness, PMOS transistor shows a better interface trap concentration but shows progress in the threshold voltage change and less deterioration in the drain current once a large stress temperature and a huge negative bias area module are applied. Besides that, at a lower drain bias, the strained transistor will show increased current deterioration. This work shows that the density of the interface trap at smaller gate oxides is maximum but the deterioration of the drain current was found to be lower. The current deterioration is important at lower drain bias [52]. The considerations are the implantation of halo, the implantation of Source/Drain (S/D), the temperature of oxide growth and the annealing temperature of silicide. The polysilicon gate is typically used in CMOS. The silicide growth is introduced on the top of polysilicon for a sub nanometer which is less than 100 nm devices in order to produce good devices. A silicide is a compound with more electropositive components in silicon. V_{th} is the main answer studied here because it is the key factor in deciding whether or not the device functions. The resistance of the Poly-silicon layer and the leakage current should be retained as low as possible to increase the system speed by reducing the time for a transistor to turn on to collect charge in the channel. The Taguchi Approach is used to

determine the optimum solution to produce the desired transistor effectively [53]. Due to variations in design parameters induced by short channel effects at deep submicron rates for engineering nodes below 1μm, low power CMOS circuit design has become a difficult task [7]. Threshold voltage modeling further shows that the threshold voltage in long channel devices was constant. MOSFETs have parameters depending on both the method and the model. Threshold Fluctuation is the parameter depending on the process and plays an important role in the development of CMOS circuits. The threshold voltage is a variable depending on the system and remains constant for long channel devices i.e. 1μm for L. Due to short channel effects, the short channel devices exhibit V_{th} variation. V_{th} also depends on device parameters such as channel size, channel width and drain voltage in short channel devices

Leakage and short channel effects (SCE) pose difficulties in the development of CMOS devices as the scale of the device function reaches the regime of nanoscale. Innovative process development of CMOS devices is important to overcome the constraints imposed by SCE. Numerous developments in Source/Drain (S/D) technology have been made to solve SCE problems [54]. This involves halo implant design allowing threshold voltage (V_{th}) roll-off behavior to be modified without significantly deteriorating the saturation current. The halo implant is noticed to have a huge impact on channel doping. A basic rise in channel doping will give threshold voltage greater stability against fluctuations in gate length and low off-current value. In addition, the selective application of forwarding or reverse body bias to ensure maximum leakage enhancement, it can have a major impact on the doping profile and the quality of the devices. Digital Bulk MOSFET manufacturing takes place under the process of Channel Engineering and Source-Drain Engineering [55]. Due to their ability to monitor short channel effects, these structures allow more aggressive system scaling in nano-scale regions. Furthermore, the junction depth should also be reduced during the scaling process which increases parasitic resistance in order to reduce its effects on the device. While using TCAD simulator, the developments are done in manufacturing processes such as lightly doped drain (LDD) to minimize peak electric field and provide shallow junctions adjacent to the tube, halo implantation to lessen punch through effect and therefore called punch through blocker, retrograded p-well protection implant, and $TiSi_2$ metal silicide to minimize sheet resistance. A contrast of an engineered device is produced with a non-engineered device to evaluate an engineered device's improved

overall performance of short channel effects as well as enhanced analog performance. Many sophisticated techniques have been applicable such as retrograde well, halo implant and light doped drain (LDD) to examine the feasibility of these methods to inhibit short channel effects. The large sub-threshold current in deep submicron systems has become a major contributor to the CMOS circuit power dissipation as threshold voltage, channel length and oxide thickness is decreased [19]. Identifying and modeling various leakage components is therefore very significant for estimating and increasing leakage power, specifically in low-power applications. Various leakage issues of the transistor such as the weak inversion, DIBL, the drain leakage prompted by the gate and the gate oxide tunneling. Leakage current is becoming a significant contributor to total power consumption with the consistent scaling of CMOS devices. Subthreshold leakage has become the influential source of leakage in existing deep submicron devices with low threshold voltages and is projected to grow with technology scaling. Gate oxide tunneling in the future is probable to be a problem as the thickness of the gate oxide shrinks. The drain leakage caused by the gate may also be a problem. To handle the rising leakage in upcoming CMOS technologies, circuit-and process-technology-level alternatives for leakage reduction should be actively sought.

2.3 DEVICE PERFORMANCE ENHANCEMENT TECHNIQUES

By replacing poly-silicon with thermally stable, the major issues that obstruct the usage of high-k materials such as reduced drain current and low-work metal gate function, trans-conductance and flexibility are sorted out. Meanwhile the introduction of MOS devices over 40 years ago, SiO_2 has been used as an active dielectric gate. The requirement for higher speed at constant power density has resulted in a decrease in MOSFET dimensions and the oxide thickness is also decreased in step as per the scaling law [56]. With the scaling of sub-100 nm engineering nodes, the introduction of new materials became unavoidable as the scaling of SiO_2 below 3nm poses severe concerns about the current and oxide breakdown of tunnels [24]. The analysis of both technologies reveals the improvement of the electrical features of n-MOSFET by applying partially depleted SOI technology compared to the large structure of n-MOSFET devices. Compared to bulk-Silicon devices partially depleted SOI devices develop the ability to boost electrical characteristics of precisely reduced threshold voltage, steeper sub-threshold swing and decreased leakage. While SOI yields a positive result, when the SOI level is continuously lowered, the parasitic effect will also

tend to increase the sub-threshold and leakage current. The influence of the physical parameters characterizing the layout of the MOSFET transistors on the threshold voltage values was analysed and their impact on critical voltage values [3]. The results obtained illustrate the influence of every single physical variable on the full value of the threshold voltage. The acceptable threshold voltage can be obtained by adjusting the MOSFET physical parameter values. When substrate doping (N_A) decreases, the oxide thickness (t_{ox}) decreases, the oxide interface load (N_{ox}) increases, the threshold voltage decreases. Compact MOSFET models are a vital relationship between technology and design [57]. The inexorable decrease in supply voltage and geometry to and below 45 nm introduces or emphasizes physical impacts that have not been important in the past or therefore the market for MOSFET models continues to increase. Variations in processes, performance and proximity effects, high-k gate materials, and non-classic system structures all challenge modeling at and below 45 nm. This research work offers fundamentals and development of MOSFET compact models as well as approaches to address new issues. The switching velocity of the SOI device is increased due to the decrease in substrate capacitance and the addition of the SiO_2 buried layer [58]. Both of these findings promote the use of these devices in space applications. Insulator Silicon (SOI) is one of IBM's launched architectures. It is predicted that by decreasing power consumption and enhancing the transient response of the system, the substrate current will decrease, parasite capacity will decrease. Using Silvaco ATLAS software simulation, the comparative study of generic MOSFET and SOI structures was carried out. By simulating both traditional and SOI system inverters, output at the circuit level was studied. This has been modeled using the mixed-mode feature of SILVACO TCAD. The existing and transient substrate reaction of SOI structures has been found to be much better than the standard MOSFET. If radiation-hardened systems are required, this device structure will be of significant relevance for space applications. High-k / metal gate technology is growing as a strong alternative for high-performance and low-power requirements to replace standard dielectric oxy-nitride and poly-silicon gates in scaled MOSFETs [23]. Main challenges that complicate the use of high-k products including drain current reduction, trans-conductance and mobility are solved by replacing poly-silicon with thermally stable and low-work-function metal gate. Compared to standard SiO_2 dielectrics, the advantages of using high-k dielectrics and metal gates over poly gates were similar. The outcomes of the simulation show that the gate leakage for HfO_2 – TiN structures is reduced by six orders of magnitude compared

to SiO_2 – polysilicon structures. The effect of different BF_2 concentration was analysed using TCAD technology from SILVACO [60]. It is presented that the characteristics of PMOS device are dependent on threshold voltage, resistivity, conductivity and leakage current. By raising the doping density from 10^{11} to 10^{20} (atoms / cm^3), it can be found that the high threshold voltage, low conductivity, high leakage current, and lower resistivity is achieved. Parameter variation for example threshold voltage, leakage current, ON-state current, output conductance, subthreshold slope, and channel doping concentration I_{ON}/I_{OFF} ratio were provided by comprehensive MOSFET simulations used in the present work. Simulations were made using the simulator of the ATLAS device [61]. Ultimately, considering short channel effects, energy necessity and ON-state current, the optimal channel doping concentration for the DG-MOSFET preferred in this work was addressed. A current model is proposed for estimating sub-threshold leakage current. This method can predict sub-threshold leakage in transistor stacks with variable transistor widths. In the 45 nm Predictive Technology Method (PTM) system when compared to SPICE simulations gives 3% and 10% average error for the two and three transistor stacks. Errors are slightly lower in the 65nm PTM process [62][41].

The state of the sub-threshold conduction depends directly on the threshold voltage, it concludes that the lowering of this value decreases the range of the leakage current of the device [63]. The only other real design parameter accessible that allows mitigating problems with the conductivity of the sub-threshold is the length of the device and as each model predicts the reduction in length of the device. Due to the continuous scaling of gate lengths, gate oxides and threshold voltages as per the scaling rules, the leakage currents must be managed [4]. The leakage currents contribute massively to power dissipation which is a major concern especially for smaller sized devices. Metal gates were used over poly-Si for sub-100 nm CMOS development to have active channel control while reducing chip leakage. In the deep-sub micro-meter environment, MOSFET structures require replacing traditional poly-Si gates with metal gates. Metal gates are used for UTB system V_{th} control and have other benefits. The choice of suitable metal work-function gates for bulk CMOS and SOI engineering results in enhanced regulation of V_{th}. Metal gates show minimized short channel effects as well. In addition, metal gates are more compatible than poly-Si gates with high k gate dielectrics. Large decrease in gate leakage current and sub-threshold swing proposes high-k metal gate technology as an effective solution for future MOS devices of Nanoscale [64]. Sub-Threshold Drain Current Model for the ultra-thin oxide and Nano-

scale halo doped n-MOSFET based on traditional drift-diffusion equation, the surface potential, threshold voltage and inversion layer of active mobility models of the n-MOSFET. The design is built on the basis of two linear pocket doping profiles along the channel from the source on the surface of the device and drain ends to the middle of the channel. Using the established model, the consequence of varying system and pocket profile parameters along with bias potential was studied on sub-threshold drain current. The proposed model after simulation determines the sub-threshold drain current's Nano-scale channel lengths [65]. Small Gate Leakage Current Partitioning Model has been generated and analyzed for Nanoscale Double-Gate MOSFETs by considering the direct tunneling induces the gate current. The circumstances of one layer high k dielectric layer and two layers (low k dielectric materials used as an insulator with a thin SiO_2 layer as an interface layer) are considered. The design computation shows a noble settlement with 2D TCAD statistical device simulations. The main objective of this work is to build a solid analytical model for the separation of the direct tunneling gate leakage current.

Source/Drain implant energy has been defined as one of the most powerful process parameters affecting the response features. Although the dose of the halo implant was recognized as an adjustment element for the NMOS system nominal values of 0.289V at t_{ox}~1.06 nm [66]. The approach involves TCAD simulations and the use of experimental design (DOE) methods for statistical analysis and modeling such as the Taguchi Method. NMOS device structural characteristics included 27nm long polysilicon gate and 1.06 nm equivalent gate-oxide thicknesses. Using Linear Extrapolation Process, the threshold voltage is obtained. Reducing static electricity is aimed at reducing power consumption and increasing electricity flow leads to an improvement in the switching rate simulated by adjusting gate channel length and gate oxide thickness parameters using the SILVACO TCAD tool. Simulation is based on selecting different sizes with variable component characteristics in order to improve the performance [67]. The static power consumption is also reduced if the gate oxide thickness is reduced. Nevertheless, the increased static power absorption is accomplished by reducing only the length of the channel and increasing the frequency of the clock when the length of the channel and the thickness of the gate oxide reduce separately. In addition, the application of horizontal scaling to minimize the channel length leads to an increase in the speed of the clock. Reduction of gate-leakage is the main motivating factor to substitute SiO_2 with alternative dielectric gate [68]. The 45

nm gate length scaled grooved and bulk MOSFETs are evaluated using the SILVACO ATLAS simulator to deliver the most stable and energy-saving dielectric alternative. At the scaled thickness, SiO_2 limits the leakage better than Si_3N_4, whereas for field scaled grooved and bulk devices with increased subthreshold slopes of 51.3mV/dec and 70mV/dec respectively, the increased thickness of the dielectric Si_3N_4 is better. Such research can be useful to those engineers working to achieve results in low power applications. In the Drain Current Model of Symmetrical DG-MOSFETs, 2D potential distribution dependent SS and threshold voltage expressions are obtained and inserted [69]. The model expressions are verified using the SILVACO (ATLAS) tool simulated results. The SS and threshold voltage fluctuations are obtained based on the device's specific channel lengths. The output characteristics of the proposed drain current model were compared with the simulation results at different channel lengths and series source for drain resistances. Lastly, the effects of fixed oxide charges were noted and the simulation results were equated. NMOS BTI is primarily attributed to electron trapping in the areas of the HK bulk and HK / SiON interface layer (IL) on the optimized process. On the other hand, PMOS BTI deterioration is mainly driven by the functionality and is found to be really identical to traditional SiON transistors [70].

For all 10 nm bulks, SOI and DG MOSFETs, a high k gate dielectric and metal gate are required. 10 nm bulks require abrupt doping levels to be regulated in the mid-range of 10^{19} cm^{-3}. DG-MOSFET can reduce the Silicon thickness needed by 4-5 nm, but it is quite difficult to create the DG structure. After all, it indicates that bulk MOSFET is the most logical choice to expand the scaling of CMOS to 10 nm [20]. 10 nm bulk CMOS needs dramatic placing of n-type and p-type dopants at rates > $10^{19}cm^{-3}$ for channel and source-drain regions. This device demands that the thickness of the silicon film be scaled to its 2nm thickness. The criterion for silicon film thickness in double-gate system design is somewhat relaxed. The need for adjustment of a double-gate device makes a manufacturable process very difficult. Silicon engineering development has revolutionized the industry of semiconductors [71]. MOSFET characteristics were consequently weakened by persistent scaling. To address the drawbacks of traditional MOSFETs, a Double Gate MOSFET is suggested. The output of MOSFET is highly performed by short channel effects due to continuous scaling. Short channel effects (SCE) are accountable for increasing the channel gate coupling. A double gate MOSFET is proposed to enhance gate coupling and its comparative analysis is carried

out. 10 nm Double gate MOSFET is developed and examined throughout terms of I-V characteristics on the Visual TCAD method. This provides 0.22V threshold voltage at 1V V_{DD} from the simulation outcomes of 10 nm. The device using an additional gate gives reduced DIBL of 69.6mV/V and the leakage current of 3.05×10^{-8}A. Optimized parameters indicated for minimizing the short channel effects, the device designed at such a dimension is very critical. A Visual TCAD software is used which renders a model of drift-diffusion for carrier simulator transport. The main focus of this research is to perform 10 nm Double Gate MOSFET simulations on Visual TCAD and to extract the device trans-conductance, DIBL, I_{ON}/I_{OFF} ratio and other significant parameters. Through introducing new system architectures and new materials, it focuses on solutions to continuing CMOS scaling. Beginning with an overview of the causes of system performance improvements, they propose engineering solutions to achieve such performance improvements [26]. Such choices include dielectric gate, metal gate electrode, double-gate FET and strained-silicon FET high-dielectric-constant (high-k). Nanotechnology is investigated in order to continue the progress made by silicon microelectronics engineering in electronic systems. The carbon nanotube field-effect transistor is suggested further instead of conventional MOSFETs. Several new structures and techniques have been suggested as "future" technologies that can make CMOS the leading technology [72]. Silicon-On-Insulator technology is a possible technology for forthcoming developments of VLSI systems. SOl technology provides MOS devices with latch-up blocked CMOS, higher packing density and speed. SOl MOS structures give most advantages compared to conventional Bulk MOS transistors. The ground plane impact was addressed on FD SOl MOSFET. In Fully Depleted SOl design, buried oxide layer is incorporated on substrate layer. The additional partial and continuous ground plane length will be addressed and its effect on current driving capacity and current leakage has been analysed. With the aid of the sub-threshold curve, the leakage current is small in GPB-based systems. The development & simulations were carried out using the SILVACO TCAD tool ATLAS system. Due to its unique scaling property, MOSFET is one of the most recommended transistors [73]. Scaling makes it possible to reduce the size of the system without impacting the output. Because of silicon oxide, silicon is the most favored semiconductor. Silicon is an overall normal semiconductor, but SiO_2 is an exceptional insulator in all other respects. SiO_2 has the great benefit that thermal oxidation can make it from Silicon whereas there is a weak oxide in every other semiconductor. SiO_2 is amorphous with very few electronic faults

and a strong interface with Silicon. Scaling is MOSET's special attribute that enables Nano-scale area size to be reduced. Scaling allows for size reduction in all respects but scaling cannot continue forever. The SiO_2 gate oxide was the main material for the scaling of silicon CMOS technology. Nevertheless, continued scaling of the gate oxide is extremely challenging as (a) scaling of gate oxide thickness leads to increased gate leakage and (b) SiO_2 runs beyond atoms for further scaling. The implementation of high-k gate dielectrics has been shown to the transistor by other problems. The association with the existing poly-silicon gates by the high-k material. This contact at the interface resulted in high trap concentrations that reduced the transistor's V_{th}. The second, in the presence of high dielectrics was the loss of channel mobility. The third issue was the high-k dielectric's low performance. High-k metal gate MOS is becoming a significant technology node specification. The material SiO_2 was used as gate oxide material for more than 32 years is to be replaced with a high-k dielectric. Using elevated source/drain, metal gate electrodes and channel technology will also be other improvements. Leakage current is the most restricting aspect for both potential silicon and existing non-silicon Nano-electronic transistors. The substitution of SiO_2 dielectric with high permittivity material and by using metal gate rather than poly gate was made to achieve greater performance improvements. Using a high-k dielectric gate in both the metal gate and the device layers III-V would reduce this leakage and significantly improve the I_{ON}/I_{OFF} ratio. The values extracted from simulation results show an increase in the leakage current. The sub-threshold swing that specifies the frequency of ON-OFF switching was demonstrated for different k-value, faster-switching speed was observed for Al_2O_3. For potential scaling, high k dielectrics must be included in the transistor architecture if gate performance scaling is to continue.

2.4 RECENT TRENDS TO ENHANCE THE PERFORMANCE OF THE MOS DEVICE

The matrix version of the method of Non-equilibrium Green (NEGF) approach for 2D graphene conductor system transport issues [74]. The closest competitor tight-binding model is used to find the dispersion relationship and therefore the tuning of the bandgap energy is observed by adjusting the graphene layer width [140][146]. To measure the NEGF equations, the machine Hamiltonian and self-energy matrices are shaped appropriately. Eventually, by observing various steps in the transmission process, the reliability is checked [75]. A detailed study on the new dielectric, $LaGdO_3$, is found as

a new high-k dielectric material for logic and memory system applications in the research labs. It has extraordinary features with a high dielectric constant ~22 and a large energy bandgap ~5.6 eV, electron and hole band offsets ~2.57 eV and ~1.91 eV respectively required for better thermal stability and lower amounts of gate leakage current. International Technology Roadmap for Semiconductors (ITRS) suggests the electrical thickness limits acceptable for modified Complementary Metal-Oxide Semiconductor (CMOS), Bipolar (Bi) and BiCMOS chip devices.This high-k material has been developed as a forthcoming high-k candidate by examining the temperature and frequency-dependent dielectric structures. Analysis of extremely-thin sheet-based $LaGdO_3$ planar condenser structures demonstrated the validity of this new material for next-generation radio frequency, analog / mixed-signal and adaptive random access memory systems. This detailed work indicates that $LaGdO_3$ poses the best solution high-k material constraints [65]. Graphene Field-Effect Transistors are manufactured using single-crystal hexagonal boron nitride (h-BN), isomorphous graphene, as a dielectric gate.The first GFET observations using Hexagonal Boron Nitride (h-BN) as both a dielectric gate and an associate substrate, resulting in significantly improved transistor current-voltage characteristics. Through a mechanical transfer process, the h-BN layers are extracted from ultra-pure h-BN single crystals and then relocated to predetermined metal gates to create graphene-on-BN substrates [76]. Using computational modeling, graphene field-effect transistor (G-FET) has been modeled to analyze the drain current and conductance. This research work focuses on controlling the conductance of drain using silicon substrates. The examination the effect of various substrates on the performance of G-FET devices equipped for band gaps. To model carriers ' transport behavior for G-FET system 10 nm channel size, a green non-equilibrium feature with mode space (NEGF MS) is used here. The comparison of GFET's drain current saturation on silicon, SiC and SiO_2 substrates at lower drain voltage are done. The prominence of the substrate on an electrical field near the G-FET device drain region is clearly presented here. It can be seen that the different material substrates not only produces a bandgap in graphene, which is essential for current saturation and conductance minimization but it is also relevant to choose the appropriate substrate that can end carrier concentration generation near drain area. Better drain Current saturation of silicon substrates was observed in comparison with SiO_2 and SiC substrates [77]. The strategy to modeling GNR MOSFETs (Graphene Nanoribbon Metal-Semiconductor-Oxide Field-Effect Transistor) steady-state and

small-signal conduct is described. In a professional machine simulator, GNR material parameters and a framework are extracted to compensate for the thickness of single-dimensional structures. This updated method is utilized to measure the current-voltage characteristics, the cut-off frequency and the peak oscillation frequency of GNR MOSFETs. Two-dimensional carbon material based graphene has received considerable exposure over the past ten years. In earlier graphene research, the higher carrier mobility is noted in large-scale graphene exceeded all prospects that graphene might be a fantastic channel material for upcoming generations of MOSFETs [78]. The research of Graphene-based Field Effect Transistor (GFET) RF characteristics is presented here. Radio Frequency variables which specify the higher frequency performance of the device and the influence of reducing the channel length of the device are examined. This research introduces the effective and innovative way of modeling graphene material in simulator and GFET device simulation using any TCAD tool. The gate length is continuously downsized and International Technology Roadmap for Semiconductors (ITRS) aims at gate-lengths of less than 7nm MOSFETs according to Moore's Law by 2020. A new GFET structure has been developed, simulated , Comprehensive Radio frequency performance analysis is provided using TCAD simulator as well as analysing GFET characteristics for specific gate lengths. The parasitic capacitances and the intrinsic trans-conductance are the performance metric parameters to measure the RF quality of the device extracted through ac analysis. Therefore, the cut-off frequency and the peak frequency of oscillation that can be extracted from the graphs can approximate the high-frequency output of GFET by parameter extraction. From the results, it can be observed that the current rises with higher V_{DS} value, the saturation velocity rises with the gate length and graphene downscaling and GFET model can be effectively modeled using TCAD [79]. Graphene has moved from being the sole area of physicists of condensed material to being studied by those in the family of electron devices. Graphene-Based Transistors have evolved fast and are now recognized a post-silicon electronics alternative. Nevertheless, most details remain unknown about the potential performance of graphene transistors in real-world applications. The study of graphene properties are important for electron devices to explore the trade-offs between these properties and analyse their effects on graphene transistor performance in both logic and radio frequency applications. Alternatively extremely thin channel devices can be built that enable graphene field-effect transistors to be scalable to shorter channel lengths and faster speeds without the adverse short

channel effects that limit the ability of older devices. Fantastic graphene transistor challenges include creating a broad and properly defined graphene bandgap, making large-scale graphene transistors that work under the current saturation framework and creating well-defined graphene nanoribbon widths and clear edges. Graphene is a relatively new material that carries hope for digital applications with unique properties [80]. The global research actions on graphene have erupted since 2004 when the first graphene specimens were deliberately produced. In addition to scientists, device designers were also concerned about the new material and soon the opportunities for graphene in electronics were considered. Most of the previous discussions on graphene potential had a predominant positive environment based primarily on the high carrier mobility observed in this material. This has contributed to consistently very pessimistic estimates of the capacity of graphene transistors and a misjudgment of their issues. This research explores the characteristics of graphene applicable to electronic applications describes its advantages and issues and summarizes the advanced graphene transistors. Graphene transistors are a quite new group of devices compared to Si MOSFETs and III – V FETs. Their efficiency is excellent due to the short background of graphene transistors, irrespective of the various problems that still need to be solved and more development is expected. Severe assumptions about upcoming progress in complex areas like graphene and applications that may emerge from them are often hard to make. Demonstration on epitaxial SiC substrate of top-gated graphene field-effect transistors (FETs) has been done here [81]. All graphene FETs have n-type transistor properties and the drain current depends almost linearly on the gate and drain voltage. With regard to low field-effect mobility of 40 cm^2/ (V.s), a peak cut-off frequency of 4.6 GHz and a max oscillation frequency of 1.5 GHz were achieved with a gate length of 1 μm for graphene devices. The graphene was epitaxially grown on SiC. Graphene FETs are manufactured as dielectric gates on semi-insulated SiC substrates with composite stacks. The characteristics of the n-type are observed without strong current saturation. Graphene RF FETs can achieve higher efficiency by further improving the quality of the graphene material and optimizing the device structure. The impact of parasitic capacitance makes MOSFET double gate quite appropriate component than MOSFET single gate for the development of digital logic switches [82]. Then implementing Independent Double Gate MOSFET's maximum capacitance design and contrasting its output parameters with MOSFET Double Gate and MOSFET Single Gate. The Double-Gate MOSFET is the first option to reduce the short channel effect. By incorporating

CMOS based design several logics can be implemented with high efficiency. This is why individual Double Gate Transistors are not suitable as the primary option for high-speed circuits but the key benefit is to be used in low-power circuits.

Developing nano-materials and nanotechnologies such as nanotubes, nanowires, nano-ribbons and specific areas for example, non-charging devices and spintronics have been researched for further developments in computing and data storage [5]. In addition, this type of nano-devices finds possible applications in other significant areas like health and environment, energy conversion and processing, consumer electronics, communications devices, sensors, etc. These new nanotechnologies and nano-electronic devices discuss technical progress and the growth opportunities of combining top-down and bottom-up nano-electronics. Discussion of certain latest semiconductor developments in the era of nanotechnology for modern CMOS transistors is applicable for high-speed and power-efficient VLSI emerging technologies. CMOS sizing and better performance patterns are expected to expand and proceed well into the next decade via these Silicon nanotechnologies. The significant advances have been made and a great deal of concern have been created in researching non-silicon materials and incorporating them into large silicon wafers to boost integrated circuit performance, offer greater flexibility and minimize power dissipation. For example, for imminent high-speed and ultra-low-power digital CMOS applications, III-V compound semiconductors and their incorporation into silicon are currently being researched [83]. The threshold voltage (V_{th}) is a significant factor for the development, simulation and operation of MOSFET. There are numerous exposures and extraction methods for modeling the device's ON-OFF transition characteristics. Due to various short-channel effects and non-idealities found in the device, the results of processing methods vary from the exact values. A new strategy is introduced here to describe and extract the actual value of MOSFET's threshold voltage. The resulting improved SCE-independent V_{th} extraction method named "Hybrid Extrapolation V_{th} Extraction Method" (HEEM) is developed, modeled and compared to few predominant MOSFET threshold voltage extraction methods to validate the findings. All outcomes are verified by detailed 2D TCAD simulation and calculated analytically at different technology nodes. The threshold voltage value is usually derived directly from the characteristics of the system transition. The practical drain voltage magnifies some SCEs such as DIBL, V_{th} roll-off, punch-through, surface scattering, depletion of velocity, effect ionization and hot

electron effect. A two-dimensional (2-D) analytical model for the surface potential variation along the channel in fully depleted dual-material gate silicon-on-insulator MOSFETs is developed to investigate the short-channel effects (SCEs) [161]. The electrical characteristics of a short channel Silicon on Insulator (SOI) transistor with a graphene layer is investigated. The analysis demonstrates that GRDC-SOI transistor can open a window for utilizing Graphene material in digital circuits and system on chip application [140] The potential distribution and Wave function distribution for n-Graphene channel G4-FET and GAA MOSFET have been obtained by solving 2-D Poisson-Schrödinger equation. In the future, transconductance, threshold voltage, Sub-threshold Swing (SS), Drain Induced Barrier Lowering (DIBL), on-off current ratio will be calculated for those structures.[141]. The high work function of hole-doped graphene also helps reduce the quantum mechanical tunneling current from the gate electrode [143]. This indicates that RHD and DM-RHD MOSFETs are interesting structures for improvement of electrical characteristics and reduction of SCEs in SOI technology for analog or digital applications. [131]

2.4 CONCLUSION

The history of issues occurs in current MOSFETs are discussed in this section. The problems arise with the MOSFET scaling. The aim of scaling is to attain optimal performance from each generation of MOSFET to optimize the ON current, reducing the DIBL and the off-state current. The boundaries of traditional MOSFET bulk scaling including measurements and voltage scaling are reached for generations of 22 nm bulk CMOS technology. Scientists and developers are now oriented on resolving the drawbacks of scaling and extend the life span of Moore's Law. OFF-state leakage is reduced by the adoption of new gate stacks with high-k dielectrics such as HfO_2 and new gate materials like metal gates and a full silicide gate. A second way to overcome scaling limitations requires the development of new interface architecture and is preferred to minimize short channel impacts by using different channel materials i.e. graphene. Adjustments in such parameters i.e. substrate doping, source/drain doping, the variance of work-function and threshold adjust implant can also mitigate the effects short channel effects. The halo doping is performed on both sides of the channel in the Dual Halo Dual Material SOI device so that the reduced leakage current can be obtained for low power applications[131].

CHAPTER 3

MODELING AND SIMULATION METHODOLOGY

3.1 DEVICE FABRICATION USING ATHENA SILVACO

The design, analysis and simulation work has been carried out in ATHENA and ATLAS of SILVACO TCAD tool. The virtual fabrication of 45nm NMOS is carried out in ATHENA and simulation work is done in ATLAS. The design flow to fabricate virtually in SILVACO tool as shown in Figure 3.1

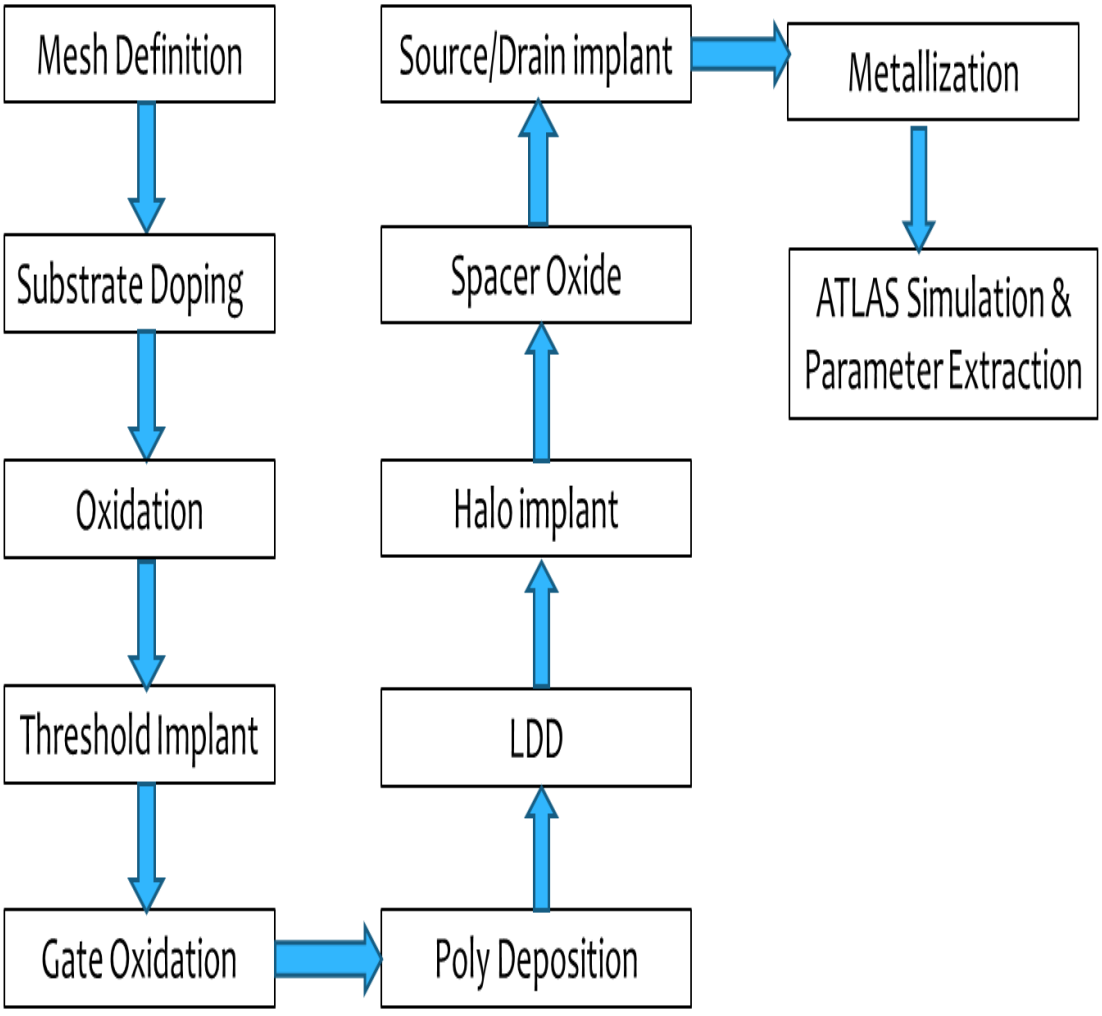


Figure 3.1 ATHENA Design Flow

This tool initializes and manipulates the framework and offers fundamental installations for deposition and etching. ATHENA is usually used in combination with VWF INTERACTIVE TOOLS. DECK BUILD, TONYPLOT, DEVEDIT, MASKVIEWS and OPTIMIZER are the other tools [37]. DECK BUILD offers an interactive environment for runtime. TONYPLOT provides capacities for scientific visualization [38]. DEVEDIT is an interactive instrument for the specification and refinement of

structure and mesh, and MASKVIEWS is an IC layout editor. The OPTIMIZER supports the optimization of black boxes across various simulators. ATHENA is also commonly used in conjunction with the ATLAS device simulator. The physical construction originating from extraction is estimated by ATHENA [84]. ATLAS employs such physical structures from ATHENA as inputs to estimate the electrical characteristics after applying supply voltages. Using ATHENA and ATLAS, the influence of process parameters on device structures can be easily identified. ATHENA users indicate the following problems:

- The structure's original dimensions to be modeled.
- The order of processing steps to be simulated (e.g., ion implantation, dry/wet etching, diffusion, photolithography etc).
- Physical models to use.

ATHENA generally provides the majority of input data in the form of input files. An input file is a text file that is generated using DECK BUILD after running DECK BUILD and setting the present simulator to ATHENA. Then, choose the Define Mesh and the Define Menu of ATHENA Mesh will appear. Now, the original rectangular grid can be specified. The right grid specification is critical in process simulation. The next step is to initialize the substrate region with its points, nodes, triangles, contextual doping, substrate orientation and other parameters. The conformal deposition is the easiest deposition model that is employed in many situations where it is not critical to the accurate shape of the deposited layer. The conformal deposition may also be utilized when doping redistribution instead of oxidizing planar or quasi-planar semiconductor areas. The next step is to deposit a specific thickness of a phosphorus-doped polysilicon layer. An ATHENA simulation's ultimate objective is generally to produce a device framework which can then be used for electrical characterization by a device simulator (generally ATLAS). ATLAS can mention the location of the electrodes and electrodes must be specified in ATHENA in many cases. ATHENA may assign an electrode to any region of metal, silicon or polysilicon. ATLAS is a flexible and expansible tool preferred for simulating devices with one dimensional, two dimensional and three-dimensional semiconductors. It is achieved using contemporary methods in Software Engineering that encourage reliability, maintenance and extensibility. Devices using the ATLAS Framework fulfill the requirements of all semiconductor application fields for device simulation. ATLAS provides visually two dimensional and three-dimensional models for the analysis of semiconductor devices.

ATLAS should only be used in combination with Deck Build, Tony Plot, Dev Edit, Mask Views and Optimizer Tools. Deck Build provides an interactive run time environment. Tony Plot offers scientific visualization capabilities. Dev Edit is a visualizing interactive tool for the specification and modification of the structure and mesh. Mask View is an editor for IC layouts. The OPTIMIZER encourages optimization of multi-simulator black boxes [37]. Together with the ATHENA process simulator, ATLAS is frequently used. ATHENA generates the physical structures after the processing of various virtual fabrication steps, then that file is used by ATLAS to estimate the electrical characteristics of that designed device. UTMOST device characterization and SPICE simulator can use these parameters calculated by ATLAS. Circuit level designers can then supply simplified models for initial circuit design focused on simulated system capabilities. It is possible to predict the influence of process parameters on circuit elements by combining Athena, Atlas, UTMOST and Smart Spice. Within the VWF Automation Tools, Atlas is preferred as simulator to simulate the designed structure. VWF ensures simulation-based testing highly automated and comfortable. VWF is used in a way that reflects innovative research and development methods by using split lots. Hence, it firmly links simulation with technological growth which leads to significantly increased benefits from the use of simulation. ATLAS is a virtual device simulator. The simulation of physical devices is not a valid approach for all engineers.

3.2 DEVICE STRUCTURE AND SIMULATION

The Gradual Channel Approximation (GCA) claims that the parallel and perpendicular components of the electrical field are effectively separated from the surface and therefore cannot add fully to the features of the observed device [85]. These tiny geometry characteristics can critically restrict the operating conditions of transistor and restrict the practical use of the device [43]. Especially for sub-micron MOSFETs, the exact identification and characterization of these small-geometry impacts are essential. The advances in VLSI manufacturing techniques are based mainly on reducing device sizes such as channel length, junction depth and gate oxide thickness [86]. This chapter involves the analytical modeling of potential distribution, threshold voltage, electric field distribution, donor concentration and valence & conduction band diagram of lightly doped 45 nm NMOS. The device is virtually fabricated with lightly doped substrate having $5x10^{15}cm^{-3}$ concentration and effective channel lengths of 40nm and

18nm. By reducing the device dimensions which leads to scaling of various parameters like junction depth, supply voltage and gate oxide thickness that results in the variation of threshold voltage [30]. Threshold voltage variations can cause serious design problems. Hence, threshold voltage can be adjusted in various ways which is the most important parameter of the MOSFET. The analytical modeling, design and simulation of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are done [61]. The expression for potential at source and drain ends and threshold voltage has been derived. The theoretical values are compared with simulated values. From simulation results from SILVACO TAD tool, threshold voltage of 0.22V is achieved at a work-function of 4.12eV. The device structure after simulation is shown in Figure 3.2

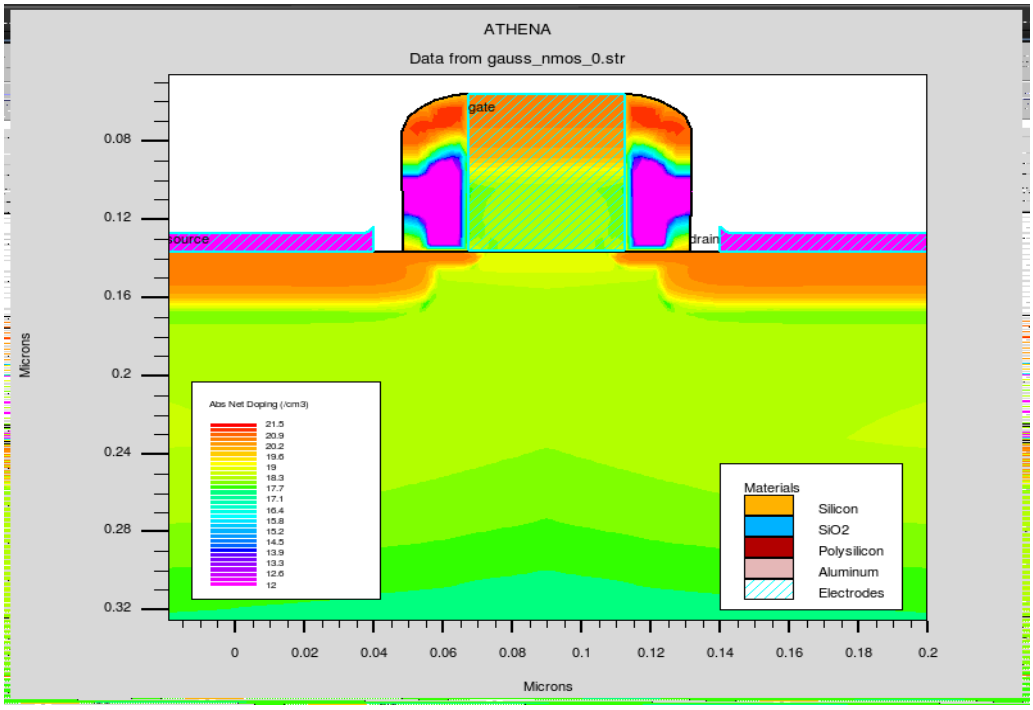


Figure 3.2 Simulated structure of NMOS

The doping profile of NMOS is as shown in the Figure 3.3 after doping of Boron with 10^{12} cm^{-3}, temperature 950°C and time 50 sec respectively.

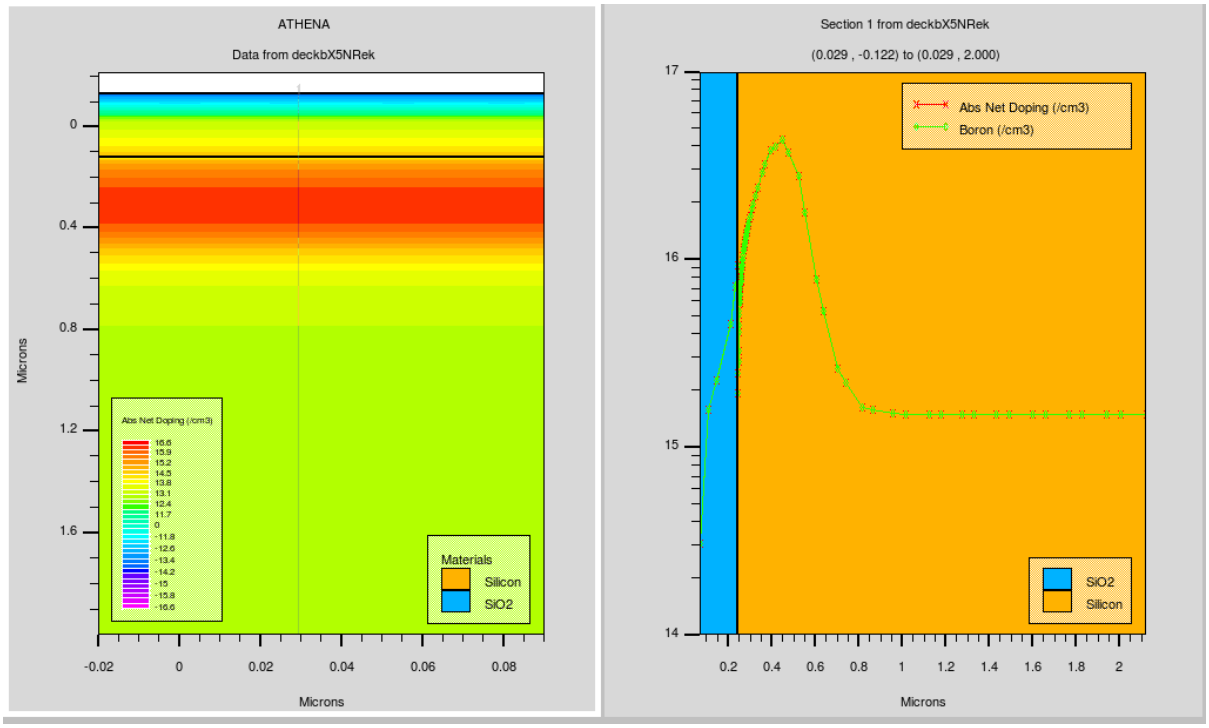


Figure 3.3 Doping Profile

The structure is designed in ATHENA and simulated in ATLAS. The drain current characteristics after the calculation with a constant current method [50] are as shown in Figure 3.4 and Figure 3.5

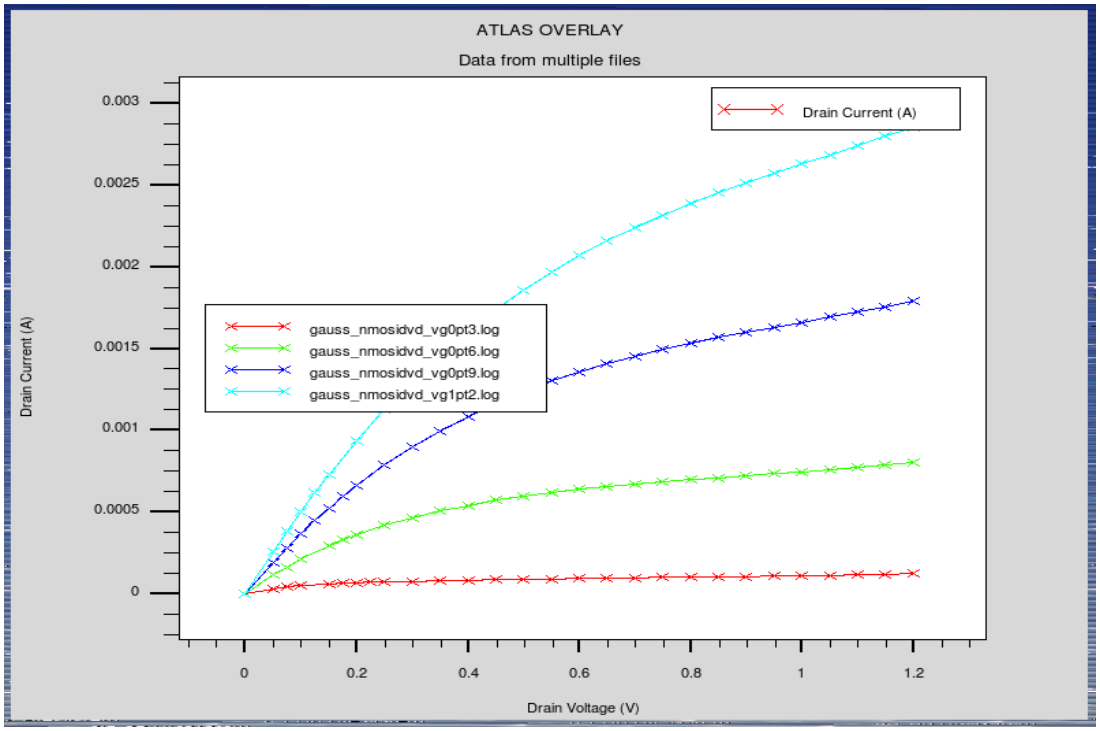


Figure 3.4 I_D- V_{DS} characteristics of MOSFET

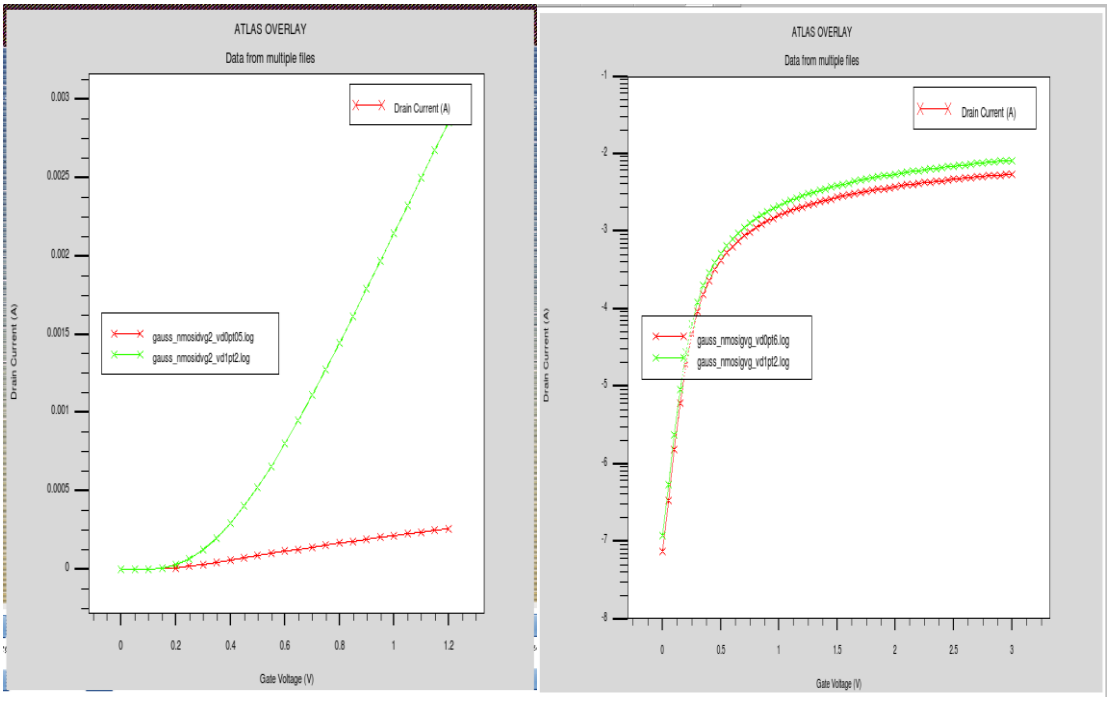


Figure 3.5 I_D- V_{GS} characteristics in linear mode and Log mode

3.3 POTENTIAL DISTRIBUTION EXPRESSION

To obtain the physical behavior characteristics of NMOS, the potential distribution of the gate, drain and source under different biasing conditions must be analysed. Potential distribution can best understand by the Poisson Equation [13][57]. The potential distribution in MOSFET is determined by 2D Poisson's Equation as given in Equation 3.1

$$\frac{\partial^2 \emptyset}{\partial x^2}(x,y) + \frac{\partial^2 \emptyset}{\partial y^2}(x,y) = \frac{\rho(x,y)}{\varepsilon si} \tag{3.1}$$

The Parabolic function is given by:

$$\emptyset(x,y) = C_0(x) + C_1(x).y + C_2(x).y^2 \tag{3.2}$$

and the boundary condition for surface potential is given by Equation 3.3

$$\emptyset(x,0) = \emptyset_s(x) \tag{3.3}$$

The electric field at y=0 is resolved by the Gate voltage V_{GS} or the electric flux at the gate oxide interface is

$$\left|\frac{\partial \emptyset}{\partial y}\,(x,y)\right|_{y=0} = \frac{\epsilon ox}{\epsilon si}\cdot\frac{\emptyset_s(x)-V_{gs}}{t_{ox}} \tag{3.4}$$

$$\left|\frac{\partial \emptyset}{\partial y}\,(x,y)\right|_{y=0} = \frac{cox}{\varepsilon si}\left(\emptyset_s\,(x)\;-\;V_{gs}+\;V_{fb}\,\right) \tag{3.5}$$

where

$$V_{fb} = \emptyset_m - \chi_{si} - \frac{E_g}{2Q} - V_T \ln\left[\left|\left(\frac{Na(xi)}{ni}\right)\right|_{y=0}\right]$$

The bandgap of silicon at room temperature

$$E_g = \left\lfloor 1.16 - \left(\frac{7.02*10^{-4}}{1108+T}\right)\right\rfloor \quad , \quad ni = 3.1 * 10^{16}\, T^{\frac{3}{2}} \exp\left(\frac{E_g}{2KT}\right) \quad \text{and} \quad V_T = \frac{K_T}{q}$$

$$\emptyset(x,y) = V_{bs} \qquad \text{and} \qquad \left|\frac{d\emptyset}{dy}\,(x,y)\right|_{y=tsi} = 0$$

The surface potential at source end is

$$\emptyset(0,0) = \emptyset_s\,(0) = V_{bi}$$

The surface potential at drain end is

$$\emptyset(L,0) = \emptyset_s\,(L) = V_{bi} + V_{ds}$$

Now we have

$$\emptyset(x,y) = C_0(x) + C_1\,(x).y + C_2\,(x).y^2 \tag{3.6}$$

$\emptyset(x,0) = C_0(x) = \emptyset_s\,(x)$ at y=0

Put the value in Equation 3.6

$$\emptyset(x,y) = C_0(x) + C_1(x).y + C_2(x).y^2 \quad (3.7)$$

Differentiate w.r.t y

$$\frac{\partial \emptyset}{\partial y}(x,y) = C_1(x) + 2y.C_2(x)$$

$$\left|\frac{\partial \emptyset}{\partial y}(x,y)\right|_{y=0} C_1(x) = \frac{\epsilon ox}{\epsilon si} . \frac{\emptyset_s(x) - V_{gs}}{t_{ox}}$$

Put the value of $C_1(x)$ in Equation 3.2

$$\emptyset(x,0) = \emptyset_s(x) + \frac{\epsilon ox}{\epsilon si} . \frac{\emptyset_s(x) - V_{gs}}{t_{ox}} .y + C_2(x).y^2 \quad (3.8)$$

Now

$$\left|\frac{\partial \emptyset}{\partial y}(x,y)\right|_{y=tsi} = \frac{\epsilon ox}{\epsilon si} . \frac{\emptyset_s(x) - V_{gs}}{t_{ox}} .+ 2y.C_2(x) = 0$$

$$C_2(x) = -\frac{\in_{ox}}{2 \in_{si} t_{si}} \frac{\emptyset_s(x) - V_{gs}}{t_{ox}}$$

Put the value of $C_2(x)\ in$ Equation 3.8

$$\emptyset(x,0) = \emptyset_s(x) + \frac{\epsilon ox}{\epsilon si} . \frac{\emptyset_s(x) - V_{gs}}{t_{ox}} .y - \frac{\in_{ox}}{2 \in_{si} t_{si} t_{ox}} \emptyset_s(x) - V_{gs} .y^2 \quad (3.9)$$

The potential distribution graph after doing calculations and simulations are as shown in Figure 3.6

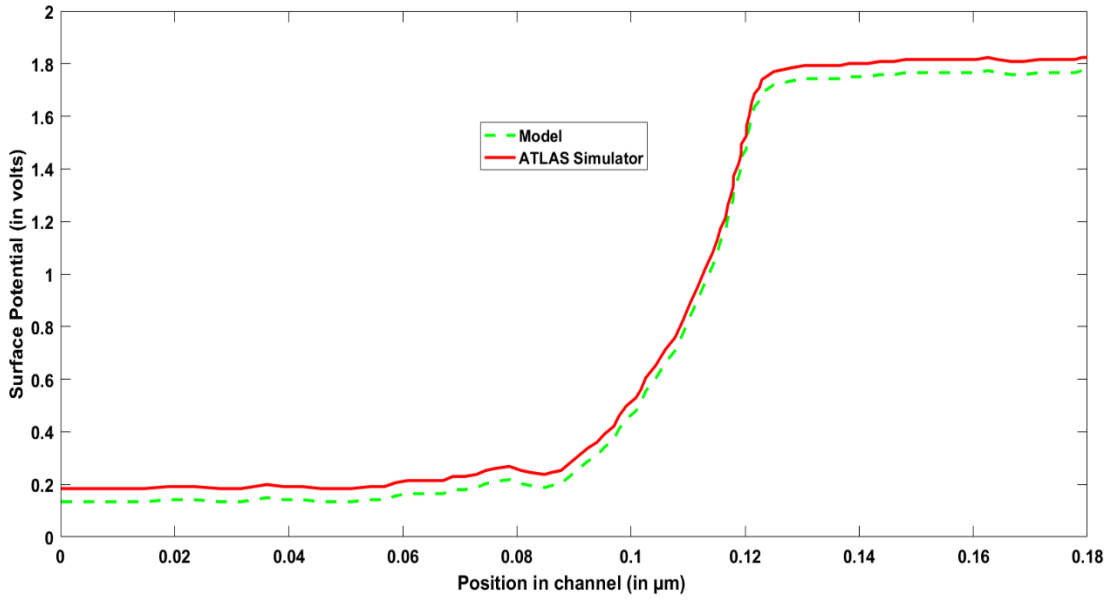


Figure 3.6 Variation of Surface Potential with position in channel

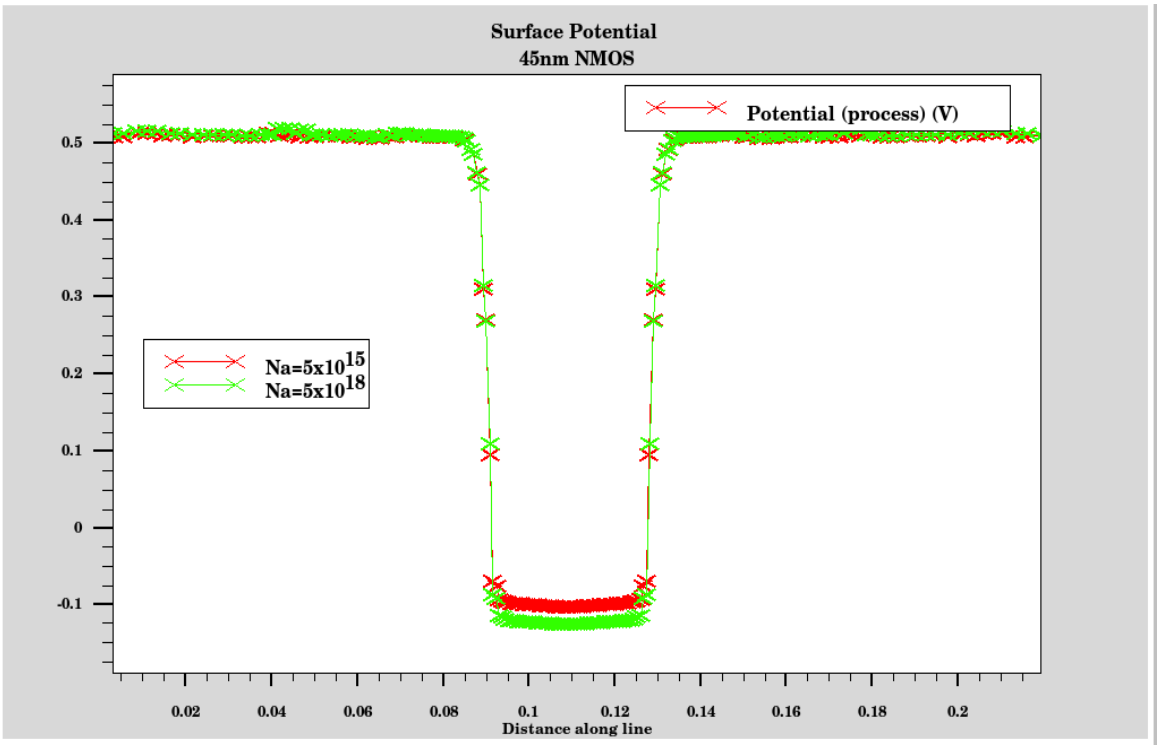


Figure 3.7 Surface Potential at Different Doping Concentrations

Figure 3.7 shows the surface potential at different substrate doping concentrations. The surface potential is shown for a lightly doped substrate having a concentration of $5x10^{15}cm^{-3}$ and heavily doped substrate having concentration of $5x10^{18}cm^{-3}$.

3.4 THRESHOLD VOLTAGE EXPRESSION

The minimum gate to source voltage V_{GS} required to cause surface inversion is well known as the threshold voltage [85][87]. Threshold voltage depends on the work-function difference between the gate and channel, the gate voltage element to change the surface potential, the voltage element of the gate oxide and the silicon oxide interface to balance the fixed charge carriers[15][43]. The first component of threshold voltage, the work-function difference between the substrate and the gate indicates the built-in potential of the MOS device. Depending on the gate material, the work function difference is

$$\emptyset_{GC} = \emptyset_F(substrate) - \emptyset_F(gate) \tag{3.10}$$

The first part of the threshold voltage reports the voltage drop across the MOSFET that is built-in potential [85] [83]. The input gate voltage is varied stepwise to accomplish surface inversion i.e. to adjust the surface potential by -2$\emptyset_F$. This reports the second component of the threshold voltage. The third component of the applied gate voltage is demanded to offset the depletion region charge which is due to the fixed acceptor ions located in the depletion region.

$$Q_{B0} = -\sqrt{2q.N_a.\varepsilon_{si}.|-2\emptyset_F|} \tag{3.11}$$

The depletion region charge density can be expressed as a function of source-to-substrate voltage, V_{SB}

$$Q_{B0} = -\sqrt{2q.N_a.\varepsilon_{si}.|-2\emptyset_F + V_{SB}|} \tag{3.12}$$

The component that neutralizes the effect of depletion region charge is equal to $-Q_B/C_{ox}$ where C_{ox} is the gate oxide capacitance per unit is.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

The generalized form of the threshold voltage can also be written as in Equation 3.10

$$V_{T0} = \emptyset_{GC} - 2\emptyset_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (3.13)$$

The depletion region charge density must be modified to indicate the influence of V_{SB} upon that charge is given by:

$$V_{T0} = \emptyset_{GC} - 2\emptyset_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (3.14)$$

The generalized form of the threshold voltage can also be written as

$$V_T = \emptyset_{GC} - 2\emptyset_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B - Q_{B0}}{C_{ox}} = V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

$$\frac{Q_B - Q_{B0}}{C_{ox}} = -\sqrt{\frac{2.q.N_a.\varepsilon_{si}}{C_{ox}}}.\left(\sqrt{-2\emptyset_F + V_{SB}} - \sqrt{|2\emptyset_F}\right)$$

The most general expression of the threshold voltage is

$$V_T = V_{T0} + \gamma.\sqrt{|-2\emptyset_F + V_{SB}| - \sqrt{|2\emptyset_F|}} \quad (3.15)$$

where the parameter γ

$$\gamma = \sqrt{\frac{2.q.N_a.\varepsilon_{si}}{C_{ox}}}$$

According to the expression of threshold voltage [71], gate oxide thickness (t_{ox}) is inversely proportional to Oxide Capacitance (C_{ox}) [88]. Theoretically, if the t_{ox} is decreased from 2nm to 1nm, the value of C_{ox} increases and Cox is directly proportional to threshold voltage. The increased value of C_{ox} will increase the value of threshold voltage [66]. The theoretical and simulated value of threshold voltage is matched here to analyse the effect of threshold voltage. The expression of threshold voltage for short channel MOS devices is given in Equation 3.10

$$V_{T0(SCE)} = V_{T0} + \Delta V_{T0} \quad (3.16)$$

$$V_{TH(SCE)} = V_{T0(SCE)} + K1.\left(\sqrt{\emptyset_F - V_{SB}} - \sqrt{\emptyset_S}\right) - K2.V_{DS} \quad (3.17)$$

where V_{T0} is the threshold voltage of long channel devices and the parameters K1, K2 and V_{T0} are used as model parameters [89][90]. The threshold voltage is also dependent on non-uniform lateral doping for short channel devices short channel effects cause limitation on channel length, channel width and drain supply voltage due to the DIBL effect.

3.5 CONDUCTION AND VALENCE BAND ENERGY DIAGRAM

An intrinsic semiconductor has equal number of holes and electrons so its Fermi level is in the middle of valence and conduction band. Fermi level is represented by Fermi-Dirac Function which is dependent on temperature. It is represented as:-

$$F(E) = \frac{1}{1+e^{(E-E_F)/KT}} \quad (3.18)$$

where K denotes Boltzmann constant. After the simulation, the energy band diagram is as shown in Figure 3.8

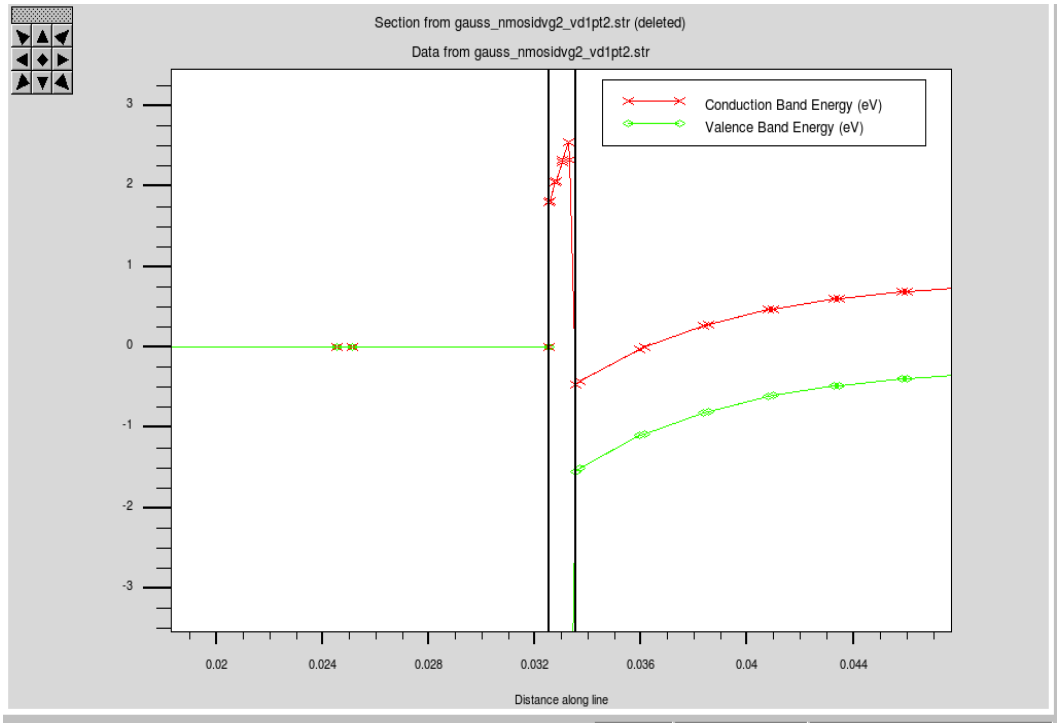


Figure 3.8 Conduction Band and Valence Band Energy

3.6 DONOR CONCENTRATION

In NMOS, the channel is created to make electrons flow from source to drain. P-type substrate is to be doped with n-type donor impurity to make the source and drain [44] as shown in Figure 3.9

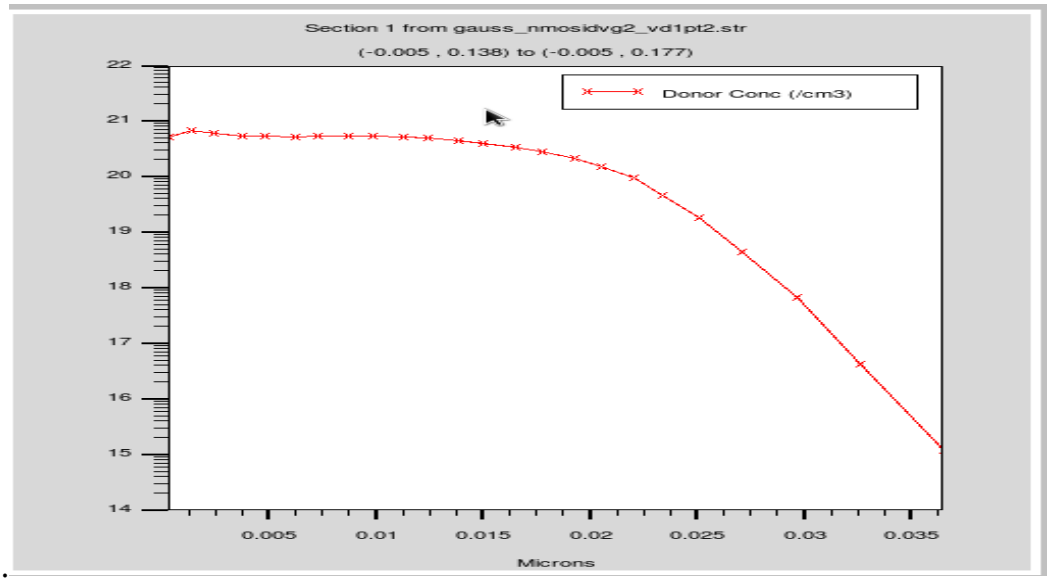


Figure 3.9 Donor Concentration

3.7 ELECTRON CURRENT DENSITY

When a voltage is applied at gate greater than the threshold voltage and drain positive than a source. The electrons flow from source to drain. The electron current density after simulation of device is as shown in Figure 3.10

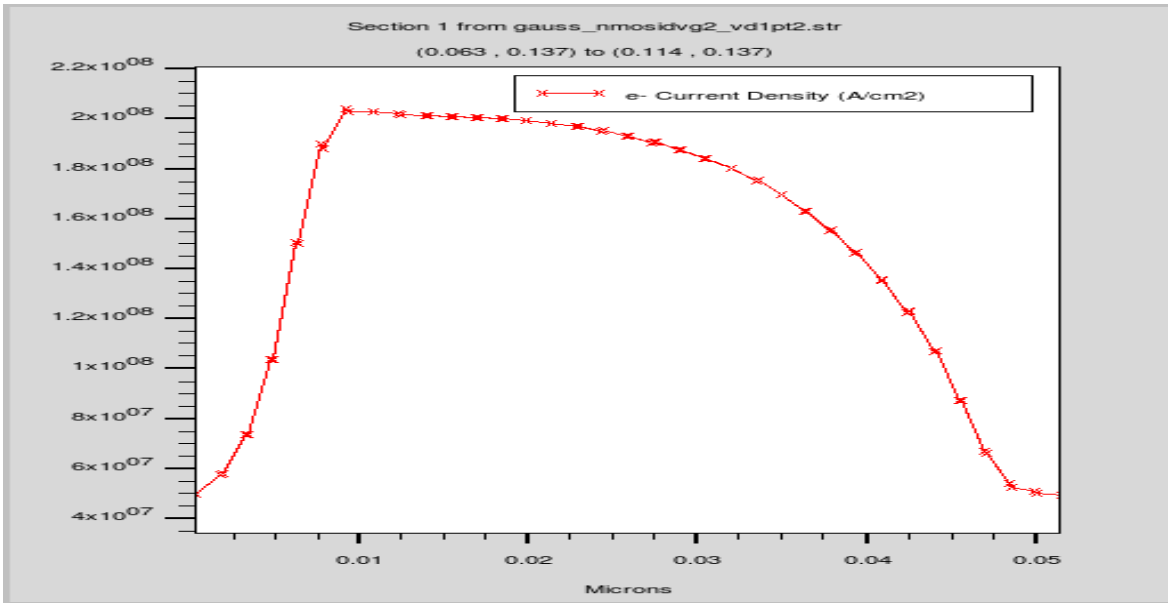


Figure 3.10 Electron Current Density

3.8 CONCLUSION

This chapter gives the introduction of SILVACO TCAD tools- ATHENA and ATLAS which are used for the design, virtual fabrication and modeling of a silicon MOSFET. The mathematical expression of surface potential and the threshold voltage has been derived here. Various parameters like electron current density, conduction band, valence band profiles and donor concentration are extracted after simulation of the device. The surface potential is modeled with high and low doping concentration of the substrate to check the effect of substrate doping on performance of the device.

CHAPTER 4

ELECTRICAL CHARACTERISTICS OF NOVEL SILICON MOSFET

Actual scaling of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) requires not only a reduction in the size of the device i.e. the length & width of the device but also a minimization of all other aspects such as gate/ source and gate/drain alignment, gate oxide thickness and width of depletion layer [91]. All the devices were previously fabricated using heavily doped substrates. There are a lot of problems with designing the NMOS and other device structures due to the use of the heavily doped substrates. Due to low resistivity, it provides Latch-up problem and offers low soft error rates (SER). It also provides substrate resistance to the low shunt. Heavily doped substrates result in an increase in the MOSFET Snapback voltage which is the main cause of CMOS latch-up. In order to undergo MOSFET Snapback voltage, MOSFET must achieve a higher substrate current as the substrate resistance decreases. Instead of using heavily doped substrates, lightly doped substrates for the manufacture of device structures is a good idea because it provides low substrates capacity and good noise insulation. In Lightly doped substrates, the capacitance of the collector to the substrate is lower which results in an increase in the power gain of unity cut off frequency. Snapback voltage is lower in lightly doped compared to heavily doped substrates. Robustness of electrostatic discharge (ESD) is greater than that of heavily doped leakage. ESD is the main problem of reliability that is good for light doping. Lightly doped substrates possess less cost than heavily doped substrates[92].

4.1 DESIGN CONSIDERATIONS OF N-CHANNEL DEVICE BY VARYING THE WORK-FUNCTION

Prior to the fabrication of Integrated circuits, the electrical parameters are analytically modeled & simulated using any computer-aided design tool. The ever increasing demand for the features of the electronic appliances has forced to put more and more transistors in a small IC chip. The main target of the integrated circuit design and fabrication is to achieve more functionality at higher speed using less power, less area and low cost. In order to match each other, various parameters such as threshold voltage, sub-threshold leakage current and sub-threshold slope etc. are analytically

derived and simulated. In this section, a 45nm n-channel metal-oxide-semiconductor field-effect transistor (NMOS) has been designed in SILVACO to provide low off-state leakage current by increasing the gate work-function. In this section, the design of NMOS and its electrical characterization of low-power 45nm channel length have been simulated using SILVACO TCAD Tools. ATLAS tool of SILVACO software has been used to simulate transistor threshold voltage and relationships with drain current to gate and drain voltages are done and then compared with the analytical results of literature. The device is designed & simulated in SILVACO TCAD tool consists of ATHENA and ATLAS which is a process and device simulation tool respectively. The fabrication steps to design any device are written in ATHENA and simulated using ATLAS tool. Figure 4.1 shows the lightly doped substrate NMOS device which shows the doping of the substrate equals to $5x10^{15}$ atoms/cm^3 which is a lightly doped substrate.

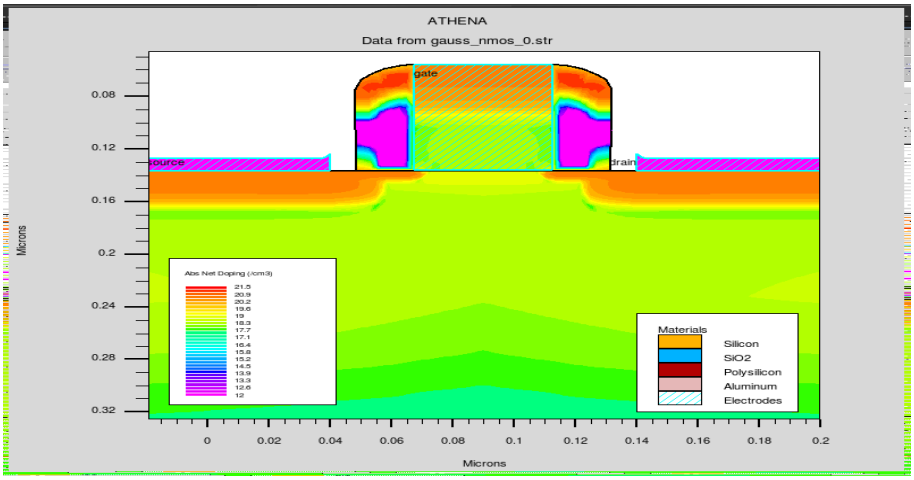


Figure 4.1 Structure of Lightly Doped 45 nm NMOS

NMOS device has been designed using these user-defined specifications. Physical gate length is considered as 40nm with 1nm gate oxide thickness. The threshold implant and S/D doping considered $5x10^{12}$ cm^{-3} and $3.5x10^{15}$ cm^{-3} respectively with 1.2V supply. ATLAS has been used to simulate the device after designed in ATHENA and doping concentration with different dose levels of different layers can be modified in ATHENA. The device performance can be enhanced by varying various parameters.

Work-Function Engineering is used to reduce off-state leakage current in lightly doped substrate devices. The work function is a significant parameter in device structure fabrication. Lightly doped substrates provide greater leakage current but with the gate work-function variation of 4.0-4.4eV, less leakage current is achieved in off-state [93].

MOSFET current-voltage features were plotted as shown in Figure 4.2 in Tony-Plot. The drain current is plotted at various work-functions at the w.r.t gate voltage. The work-function of the poly-silicon gate has ranged from 4.0 to 4.4 eV. V_{GS} varies from 0.05V to 1.2V at steady drain voltage to achieve the I_D-V_{GS} curve. After the simulation, it is possible to extract from this curve device parameters such as threshold voltage, sheet resistance, ON current, leakage current, sub-threshold slope, and DIBL. In order to achieve the gate voltage I_DV_{DS} curve, V_{GS} was set at a constant gate voltage to 0.1V to 1.2V. The output characteristics can be viewed in Tony Plot.

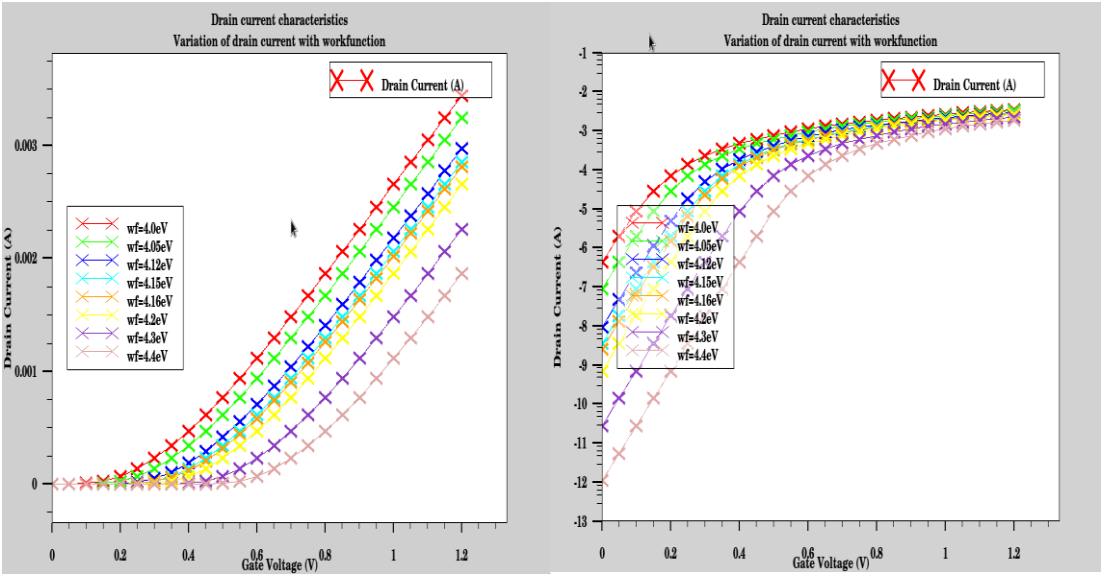


Figure 4.2 I_D-V_{GS} Plot in linear Scale and Log Scale for Different Gate Work-Functions

The result shows that the device sub-threshold behavior improves as the work-function of the poly gate increased to a higher value [62][63]. It is because the rise in the poly gate work-function improves the associated threshold voltage which in turn decreases the off-state leakage current and improves the efficiency of the NMOS device [55].

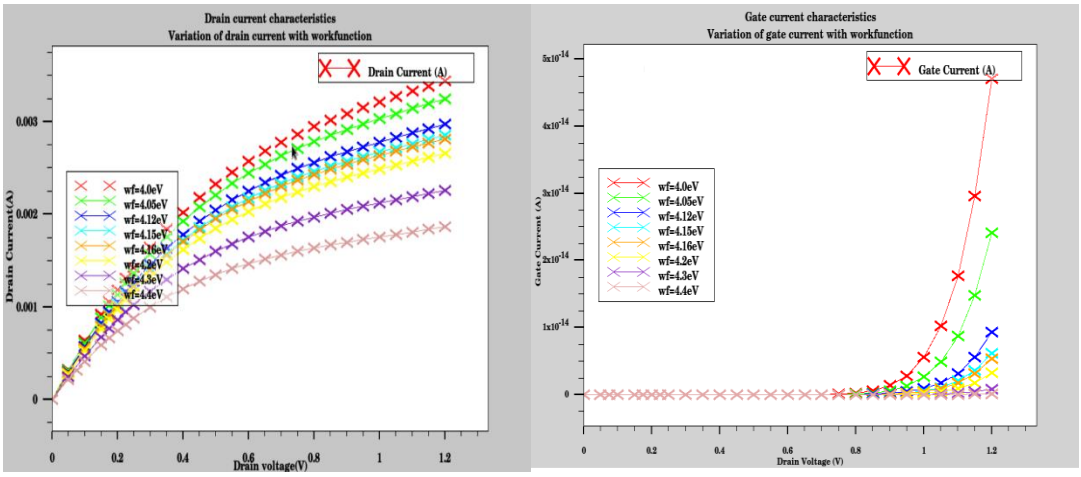


Figure 4.3 I_D versus V_D Plot and I_G versus V_D Plot for different gate work-functions

Figure 4.3 illustrates the variation of drain current at different ranges of work-functions with drain voltage at different gate work-functions [94]. As the work-function increases, drain current decreases.

4.1.1 Impact of Work-Function on Threshold Voltage

As the work function of the poly gate can be adjusted to satisfy a specific threshold voltage demands, the selection of particular work-function material to be employed for the metal gate in that device depends on which metal provides work function suitable for the specific threshold voltage performance [4]. The threshold voltage is the minimum voltage required at the gate to establish a strong inversion layer or virtual channel or the gate voltage that causes surface inversion is called the threshold voltage. The threshold voltage depends upon the flat band voltage built-in the MOS system, twice the bulk potential, the voltage across the gate oxide owing to the load on the depletion layer and inversely proportional to the oxide capacitance given in Equation 4.1 below:

$$V_T = V_{FBV} + V_{CH} + 2\phi_F + \frac{q(N_A - N_D)}{C_{ox}}\sqrt{\frac{2\varepsilon_s 2\phi_F}{q(N_a - N_d)}} \tag{4.1}$$

where, the flat-band voltage [135], V_{FB} is given by:

$$V_{FBV} = \phi_{MS} - \frac{Q_f}{C_{ox}} \tag{4.2}$$

$$\phi_{MS} = \phi_M - \phi_S = \phi_M - \left(\chi + \frac{E_c - E_i}{2q} + \phi_F \right) \tag{4.3}$$

and $$\phi_F = V_t \ln \frac{p}{n_i} = -V_t \ln \frac{n}{n_i} \tag{4.4}$$

The work function is the difference between potentials of metal and semiconductor as shown in Equation 4.3 and Equation 4.4 termed as Fermi Potential. Work-function is the energy needed to eliminate an electron from a conductive material's surface to point with zero kinetic energy just outside the surface. Due to the complication described in modeling, the accuracy of the work function is difficult to predict theoretically. The gate work function is generally smaller for metals with an open lattice and higher for metals where the atoms are arranged in a structure that is much closer. It has been observed that the corresponding threshold voltage increases to the recommended value by increasing the work function of MOSFET.

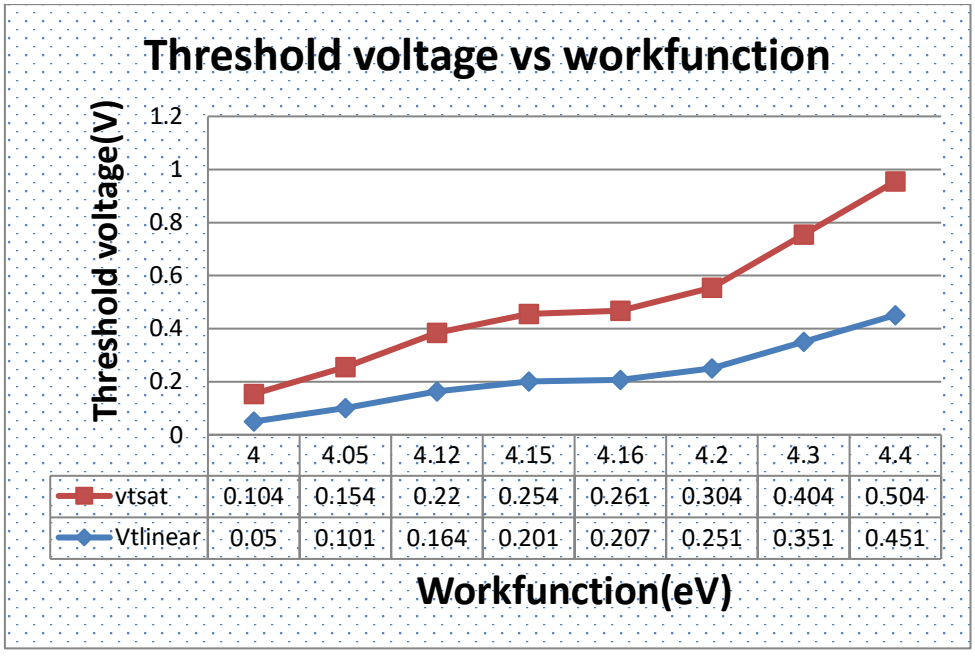


Figure 4.4 Variation of Threshold Voltage at Higher Drain Voltage with Work-Function

Figure 4.4 depicts the threshold voltage equivalent to 1.2V and 0.05V respectively at higher and lower drain voltage rises with the gate electrode work-function. The threshold voltage dependence function of the Poly-silicon gate works as a linear relationship which can be proved by Equation 4.1. The result as shown in Figure 4.4

for a device with gate length, L_G=40 nm, EOT=1 nm and V_{DD}=1.2V sustaining higher threshold voltage needed for low power applications and can be attained more efficiently by increasing the gate work function [55].

4.1.2 Impact of Work-Function ON Current and Sub-Threshold Current

Figure 4.5 illustrates the device ON current behavior as a function of the gate work function. From the simulation results, it has been observed that ON current of the device is reduced by increasing the work-function of the gate electrode for low power devices.

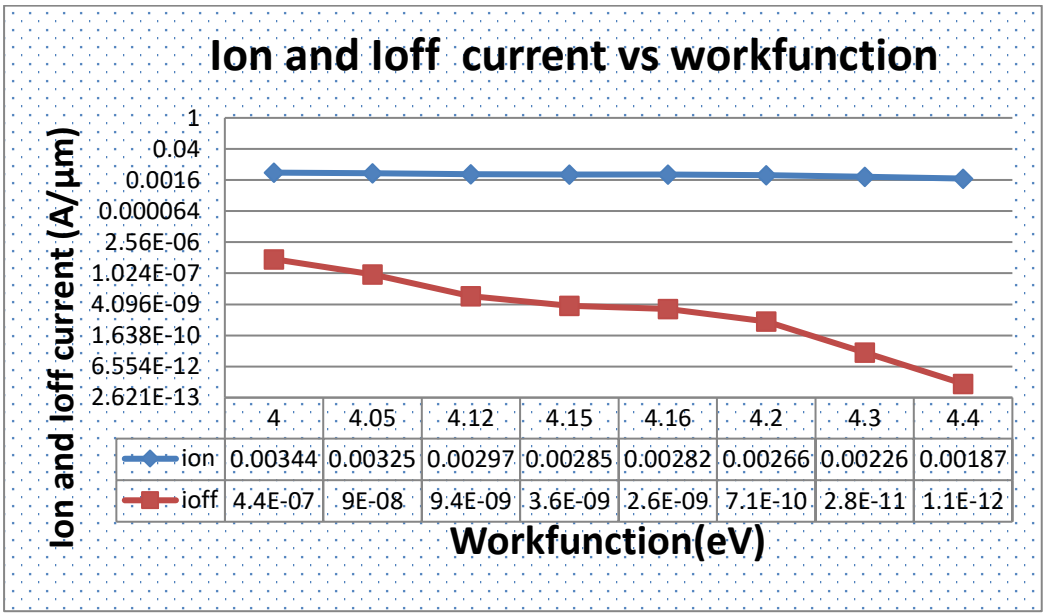


Figure 4.5 illustrates the on current and off current of the device.

From the off-state current characteristics as shown in Figure 4.5, it has been observed that this tolerable OFF-state current of the MOSFET can be fulfilled by a higher gate work function of nearly 4.4eV. The off-state leakage current is reduced by increasing the work function of the gate electrode.

4.1.3 Impact of work-function on On/Off ratio

After the device simulation, higher the ON/OFF current ratio has been observed and improved further by increasing the gate work function of MOSFET. The current of the device can be decreased to some range with an enhanced gate work-function but an increase in the ON/OFF current ratio is a positive sign of a general enhancement of the drive current with a necessary small off-state leakage current for LSTP technology. Figure 4.6 shows the ON/OFF ratio increases with the increase of work-function.

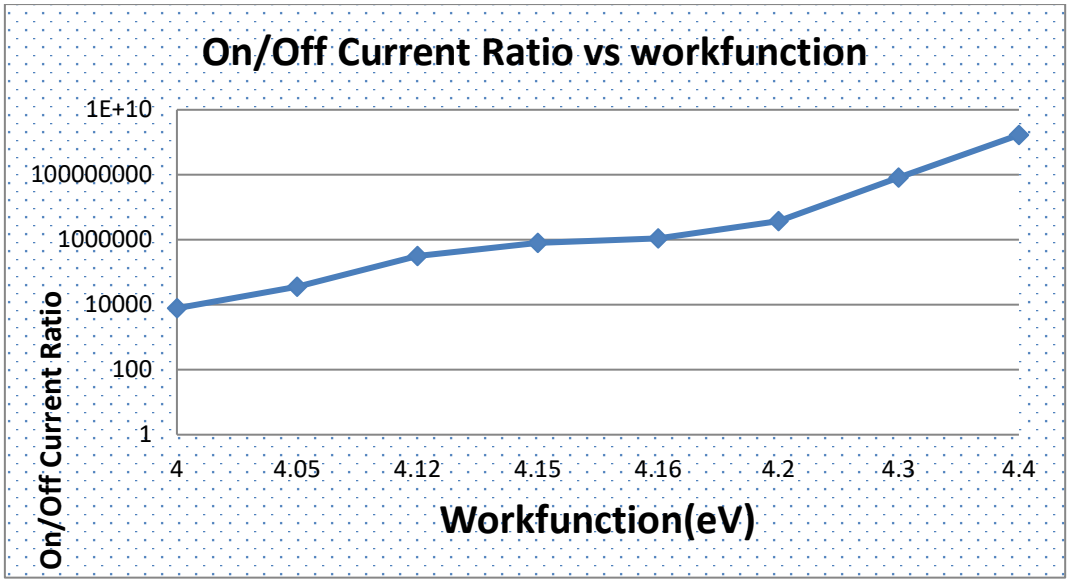


Figure 4.6 Variation of ON/OFF current with Work-Function

4.1.4 Impact of Work-Function on Sub-Threshold Slope

The sub-threshold current in long channel devices is greater than a few V_T independent of the drain voltage for V_{DS}. The gate voltage-dependent is exponentially the reverse of the Log_{10} (I_{DS}) path versus the Sub Threshold Slope features as shown in Equation 4.5.

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L} (m_0 - 1)(V_T)^2 e^{(V_G - V_{th})/m_0 v_T} (1 - e^{-V_{DS}/v_T}) \tag{4.5}$$

where

$$m_0 = 1 + \frac{C_D}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{w_D}$$

$$S_t = \left(\frac{d(\log_{10} I_{ds})}{dV_{gs}} \right)^{-1} = 2.3 \frac{m_0 kT}{q} = 2.3 \frac{kT}{q} \left(1 + \frac{C_D}{C_{ox}} \right) \tag{4.6}$$

Sub-threshold Slope demonstrates how quickly the transistor can be switched off (I_{OFF} reduction rate) when V_{GS} is lower than the threshold voltage. For bulk CMOS processes, SS lies between 70 and 120 mV/decade. Figure 4.7 depicts the decrease of sub-threshold current with the increase of work-function as desired for low power

devices.

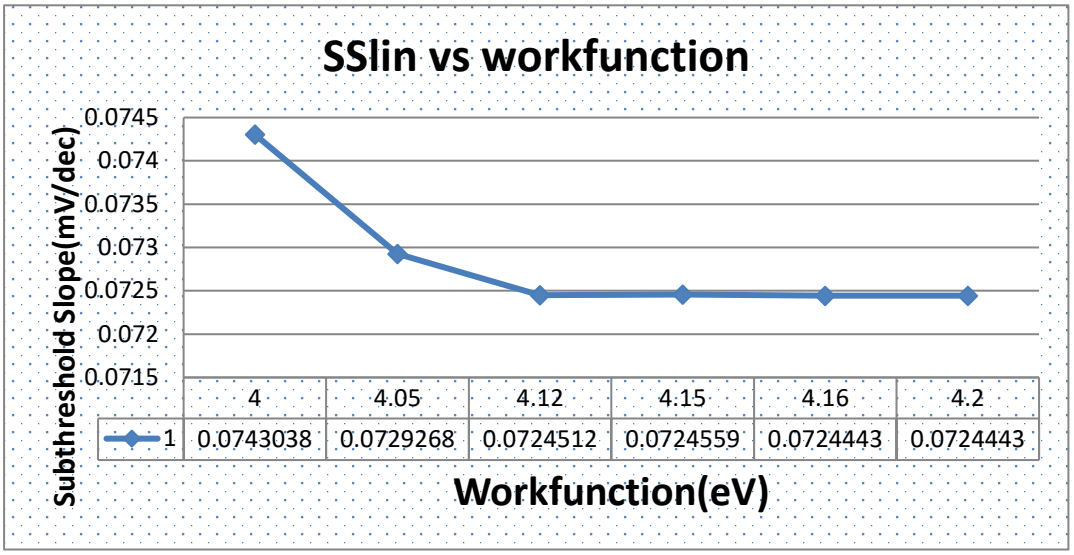


Figure 4.7 Variation of SS linear with work-function

4.1.5 Impact of Work-Function on DIBL

Source and drain are segregated far away in lengthy channel MOSFET devices that their depletion regions in most of the devices have no impact on prospective or field pattern [48]. The threshold voltage is not dependent upon the channel length and drain bias for these devices. In short channel devices, the source and drain depletion width in vertical direction and source-drain potential has a powerful impact over a substantial part of the device on band bending. Therefore, short channel device threshold voltage and sub-threshold current differ with drain bias [15] [65]. This impact is known as DIBL (reducing barrier caused by drain).

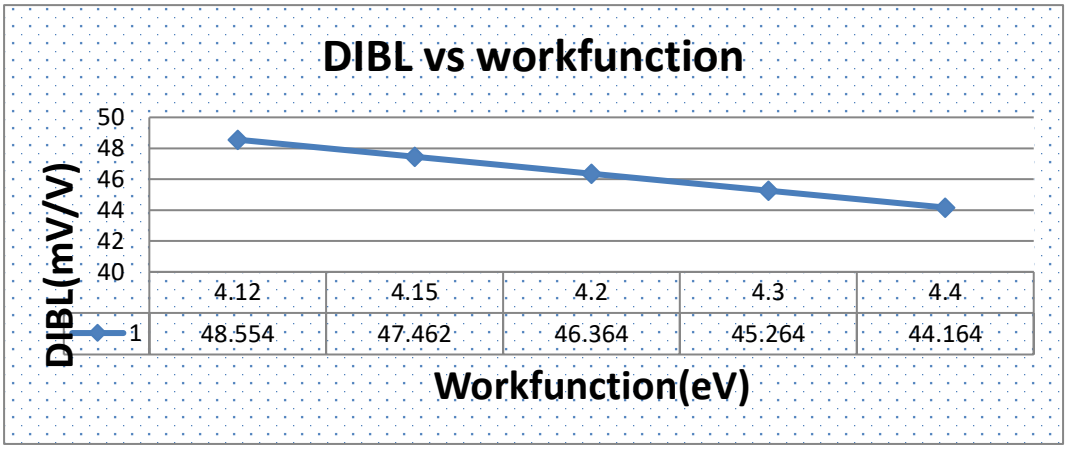


Figure 4.8 Variation of DIBL with work-function

DIBL happens when the drain depletion region interacts with each other near the surface of the channel to reduce the potential of the surface [95]. It reduces the height of the barrier when the elevated drain voltage is applied to short channel devices which further leads to reduction in threshold voltage. The source injects the carrier into the surface of the channel. With high drain voltage and shorter channel length [67], DIBL is improved. DIBL does not alter the path of the sub-threshold but lowers V_{th}. In practice, DIBL can be calculated accordingly given below in Equation 4.7 and also shown in Figure 4.8

$$DIBL = -\frac{V_{th}^{\ DD} - V_{th}^{\ LOW}}{V_{DD} - V_{D}^{\ LOW}} \tag{4.7}$$

Where V_{th}^{DD} or V_{tsat} is the threshold voltage estimated at a high drain voltage applied and V_{th}^{LOW} or V_{tlin} is the threshold voltage estimated at a very small drain voltage, typically 0.05 or 0.1V. V_{DD} is the supply voltage or high drain voltage and V_{D}^{LOW} is the low drain voltage (for a linear portion of computer I-V). The minus sign in the DIBL Equation 4.7 shows a positive DIBL value. This is due to the high drain threshold voltage, V_{th}^{DD} which is always lower than a low drain threshold voltage, V_{th}^{LOW} and it is typically measured in mV/V. DIBL also reduces by the gate increased work-function. DIBL can decrease the frequency of operation of the device as outlined in the equation:

$$\frac{\Delta f}{f} = -\frac{2DIBL}{V_{DD} - V_{th}} \tag{4.8}$$

V_{DD} is supply voltage and V_{th} is threshold voltage.

4.1.6 Impact of Work-Function on Substrate Doping

Because of its low sensitivity to Latch-up issues, low soft error rate and low shunt to substrate strength, the heavily doped substrates were chosen earlier. As the resistance decreases, MOSFET must attain a greater substrate current to undergo MOSFET snapback which is the significant disadvantage of heavily doped substrate devices[96]. Lightly doped substrates are preferred instead of heavily doped which have better characteristics. Lightly doped substrates provide low capacitance of substrates and excellent isolation of noise with decreased costs. By reducing the capacitance, this results in a rise in cut-off frequency of unity power gain. ESD robustness of lightly

doped substrates is higher than the heavily doped substrates. It also has low snapback voltage which is the best feature of lightly doped devices. This segment shows that in terms of noise immunity, the lightly doped (LD) substrates are much better than the heavily doped (HD) substrates. In MOSFETs, the impact ionization happens because high electric fields trigger an impact that produces a couple of hole-electrons. The electrons flow out the drain and the holes flow into the substrate resulting in the flow of a substrate current. The impact ionization is the physical mechanism for substrate current generation. The electric field close to drain region creates impact ionization at a substantial pace as the channel length of MOSFETs is lowered to the sub-micrometer range. As the substrate current rises, the generated hole current in the MOSFET flows into the substrate[97]. Substrate current can trigger issues in short channel devices such as latch-up, threshold voltage change and trans-conductance degradation. The substrate current also adds to the development performance and the breakdown features in the saturation region. This section explores the impact on a 40 nm channel length Metal Oxide Semiconductor Field Effect Transistor (MOSFET) of lightly doped (LD) and heavily doped (HD) substrates. In terms of drain current, substrate current, sub-threshold current, on-off current ratio, sub-threshold swing, threshold voltage and the impact of variation of the p-type substrate doping concentration (from 10^{15} to 10^{18} cm^{-3}) is explored. The findings of the simulation indicate that the lightly doped substrate devices with high functionality provide enhanced off-state leakage current[98]. It was also noted LD structures even at small gate oxide density have increased drain current. In SILVACO TCAD software, all the simulation & design work was performed. 45 nm NMOS device was designed using a lightly doped substrate with a $5x10^{15}$ cm^{-3} doping concentration and a heavily doped substrate [99] with a $5x10^{15}$ cm^{-3} doping concentration. The distinction in both devices is only the concentration of doping. The length of the physical gate is 40 nm. The structure of the NMOS device is as shown in Figure 4.9.

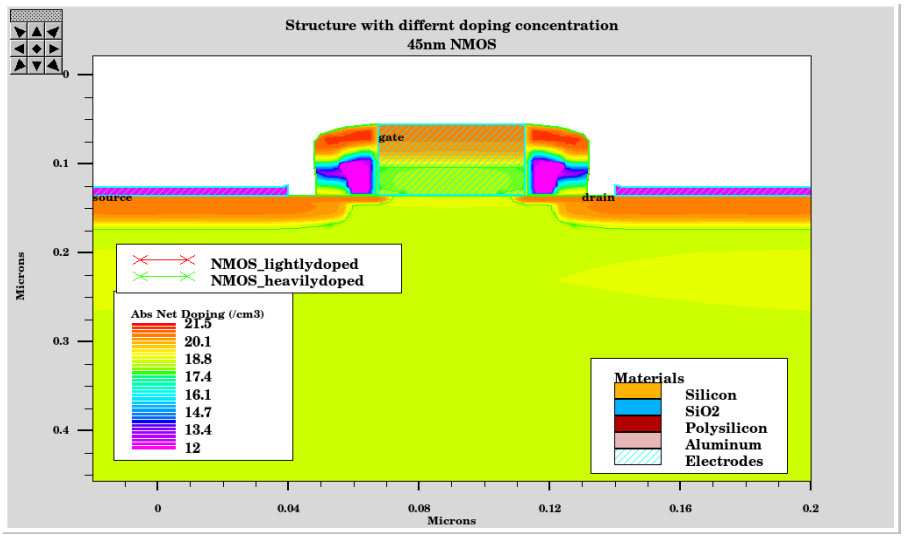


Figure 4.9 Structure of NMOS devices (LD and HD)

Figure 4.9 illustrates the structure of the NMOS device [100] with lightly and heavily doped substrate which has been designed in ATHENA of SILVACO software and simulated using ATLAS of SILVACO software. The drain current model is as follows:

$$I_D = \mu_n C_{ox} \frac{W}{dy} (V_G - V_S - V_C - V_T) dV_C \tag{4.9}$$

where the drain-source voltage is substituted by the channel voltage. By integrating the equation on both sides from the source to the drain, integrate left side from 0 to the gate length, L, and right-hand side from 0 to the drain to source voltage [101], V_{DS}

$$\int_0^L I_D \mathrm{dy} = \mu_n C_{ox} W \int_0^{Vds} (V_G - V_S - V_C - V_T) dV_C \tag{4.10}$$

The drain current, I_D, is constant so that integration results in:

$$\mathrm{I_D} = \mu_n \mathrm{C_{OX}} \left[(\mathrm{V_{GS}} - \mathrm{V_T}) \mathrm{V_{DS}} - \frac{\mathrm{V^2_{DS}}}{2} \right], \text{for } \mathrm{V_{DS}} < \mathrm{V_{GS}} - \mathrm{V_T} \tag{4.11}$$

First, the drain current rises linearly with the applied drain-to-source voltage (V_{GS}), the extents to a peak value [102][22]. The current would even reduce and ultimately become negative according to the above equation. At the drain end of the channel, the charge density is almost zero and the drain current decreases. The charge in the inversion layer goes to zero and reverses the signal as the interface accumulates holes. However, the reversed-biased p-n junction diode forms between the drain and the substrate stop the flow of holes into the drain and these holes cannot add to the drain

current. The current instead touches its highest value and retains that value for greater voltages from drain to source. A depletion layer positioned at the drain end of the gate incorporates the extra drain-to-source voltage. This behavior is stated as drain current saturation. The drain current in the saturation region, $I_{D,}sat$ is given by means of :

$$I_{D\,sat} = \mu_n C_{OX} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} \text{ , for } V_{DS} > V_{GS} - V_T \qquad (4.12)$$

The drain current model explains a MOSFET drain current versus drain voltage characteristics which are usually plotted for different gate-to-source voltages. The simulated drain voltage characteristics at various drain voltages and gate voltages are as shown in Figure 4.10.

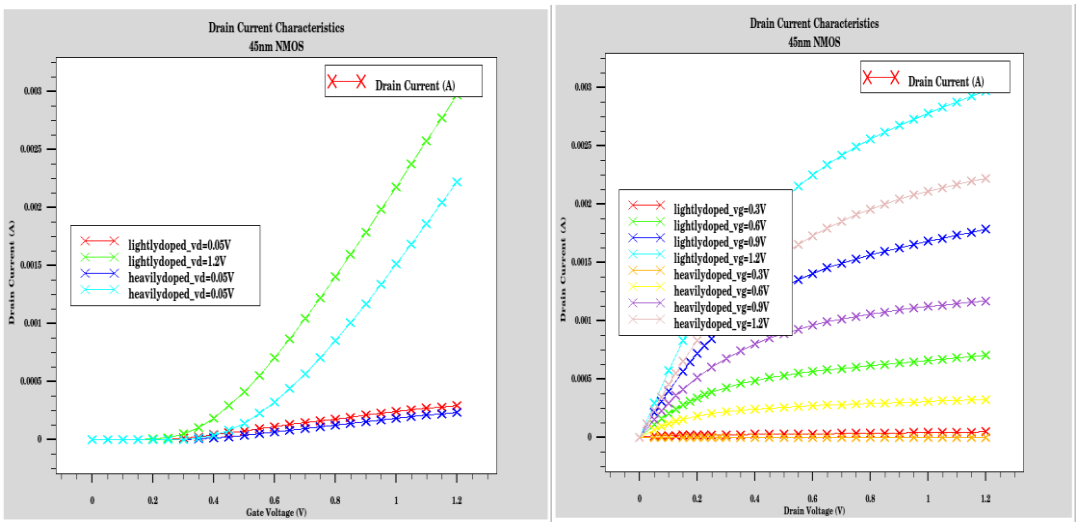


Figure 4.10 I_D versus V_{GS} Plot and I_D versus V_{DS} Plot

Figure 4.10 shown above shows that the maximum drain current is achieved using lightly doped devices. NMOS device with a channel length of 45nm has been simulated in ATLAS SILVACO. By increasing the substrate doping concentration, both the drain current and leakage current are decreasing at larger substrate doping. The rate of reduction in the off-current is faster than the ON current in such a way ON/OFF current ratio becomes very high at a substrate doping concentration from 10^{15} to 10^{18} cm^{-3}. If the thickness of the gate oxide is further reduced, the electric field across the oxide will increase. Together with low gate oxide thickness, the high electric field results in electrons tunneling. This phenomenon occurs through the gate oxide from the substrate to the gate and from the gate to the substrate. Figure 4.11 shows that there is

a prominent gate leakage current in heavily doped NMOS device as compared to a lightly doped NMOS device.

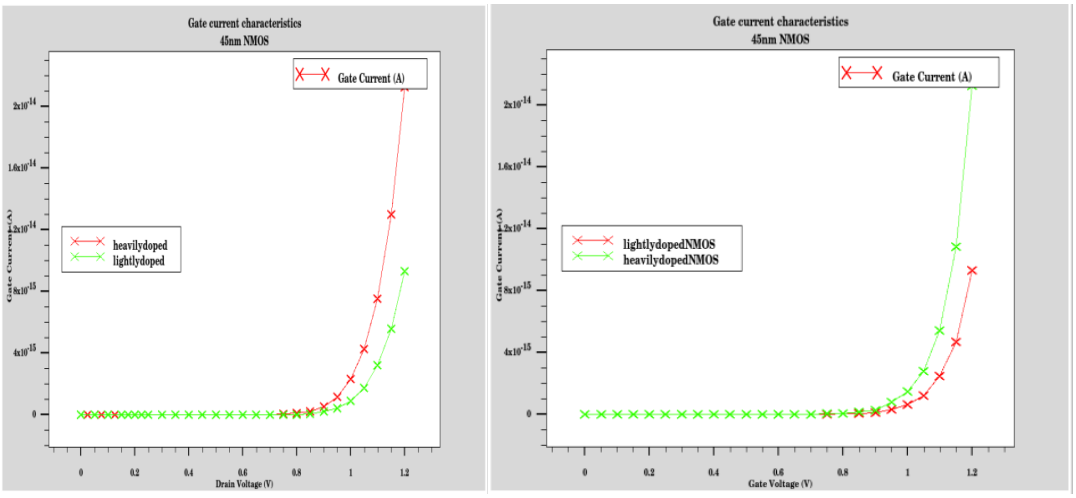


Figure 4.11 I_G versus V_{DS} Plot and I_G versus V_{GS} Plot

The current expression of the substrate can be derived by integrating the carrier impact ionization coefficient across the channel's speed-saturated region

$$I_{sub} = I_{DS} A_i \int_{y=0}^{y=ld} \exp\left(-{B_i}/{E_{s(y)}}\right) dy \qquad (4.13)$$

where A_i and B_i are the coefficients of impact ionization. $E_{s(y)}$ is the electric field along the direction of the channel, y=0 is at the edge of the channel velocity-saturation region, ld is the velocity-saturation region length and I_{DS} are the drain current without taking into account the effect of ionization. In the saturated region of velocity, $E_{s(y)}$ can be found in a Pseudo-Two-Dimensional Analysis. There is an exponential relationship between $E_{s(y)}$ and distance, where E_{sat} is the critical field of velocity saturation and lt is the characteristic length of the exponentially rising electric field given by:

$$lt = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} X_J} \qquad (4.14)$$

Where t_{ox} is the thickness of gate oxide and X_J is the depth of drain/source junction. The dielectric permittivity of silicon dioxide and silicon are ε_{ox} and ε_{si} respectively [44]. The above expression can also be expressed within the saturation region in terms of voltage. Substrate current is noted more in LD devices after simulation of LD and HD

devices but can be reduced by increasing the work-function to 8.277x10^{-07}A as shown in Figure 4.12

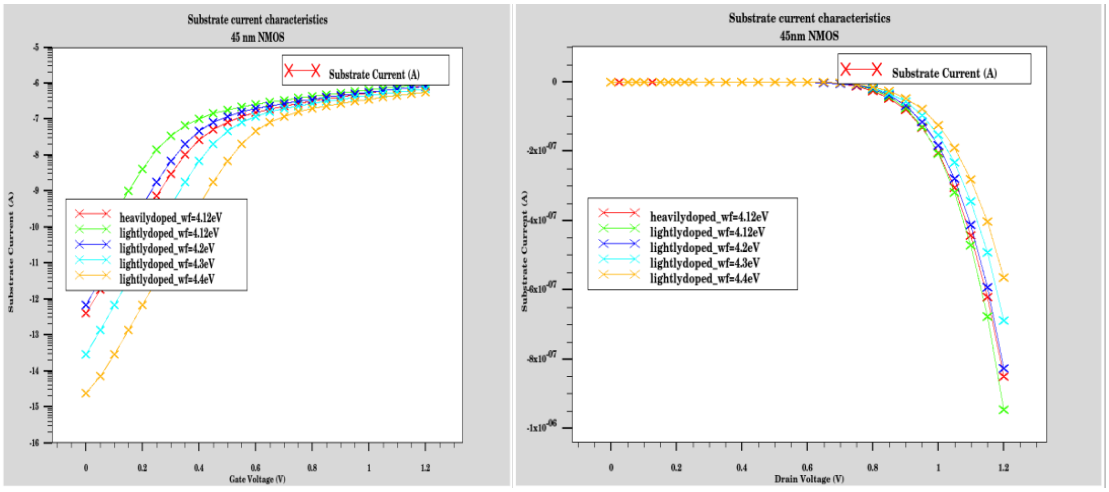


Figure 4.12 I_{SUB} vs V_{GS} and I_{SUB} vs V_{DS} Plot Plot at Different Work-Functions

The thickness of the gate oxide [103] is scaled between 2 nm and 1 nm. As the thickness of the gate oxide varies from 2 nm to 1 nm, the drain current in lightly doped NMOS is higher than in heavily doped NMOS as shown in Figure 4.13

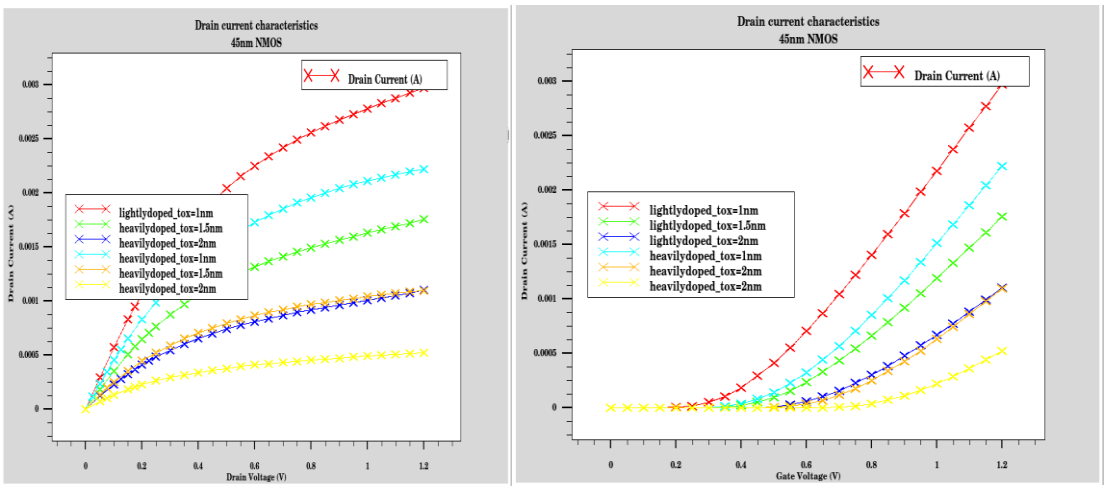


Figure 4.13 I_D vs V_{DS} Plot and I_D vs V_{GS} Plot at Different Gate Oxide Thickness

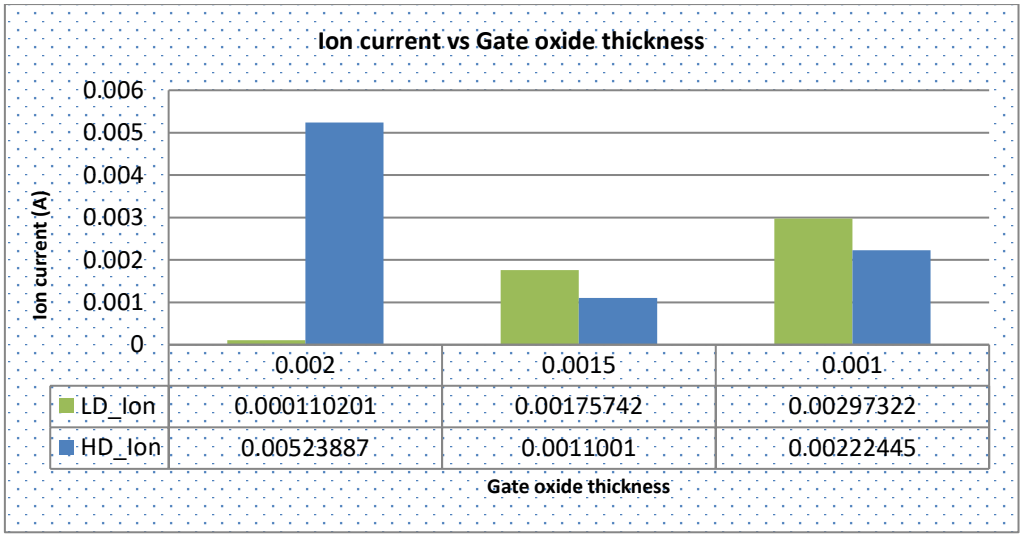


Figure 4.14 Variation of I_{ON} current with Gate Oxide Thickness

Figure 4.14 illustrates the current simulation for lightly doped and heavily doped devices. The graph shows that as the gate oxide thickness is scaled down, the drain current of the heavily doped NMOS decreases but the drain current of the lightly doped device increases as the gate oxide thickness decreases.

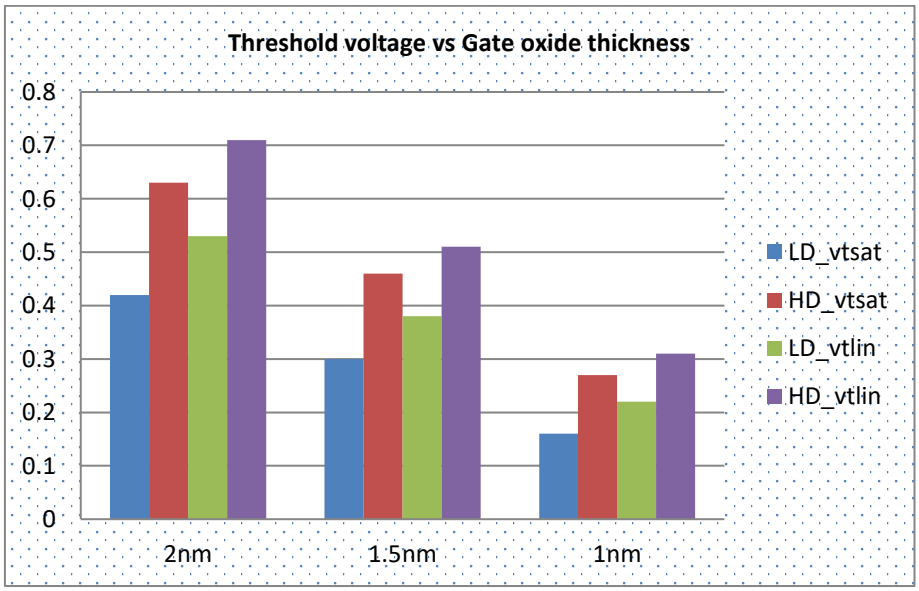


Figure 4.15 Variation of Threshold Voltages with Gate Oxide Thickness

Figure 4.15 demonstrates the decrease in threshold voltages (V_{tsat} at V_{DS} =1.2Vand V_{tlin} at V_{DS} =0.05V) of lightly doped and heavily doped devices but lightly doped NMOS has achieved the best value of 0.22V threshold voltage as per ITRS guidelines.

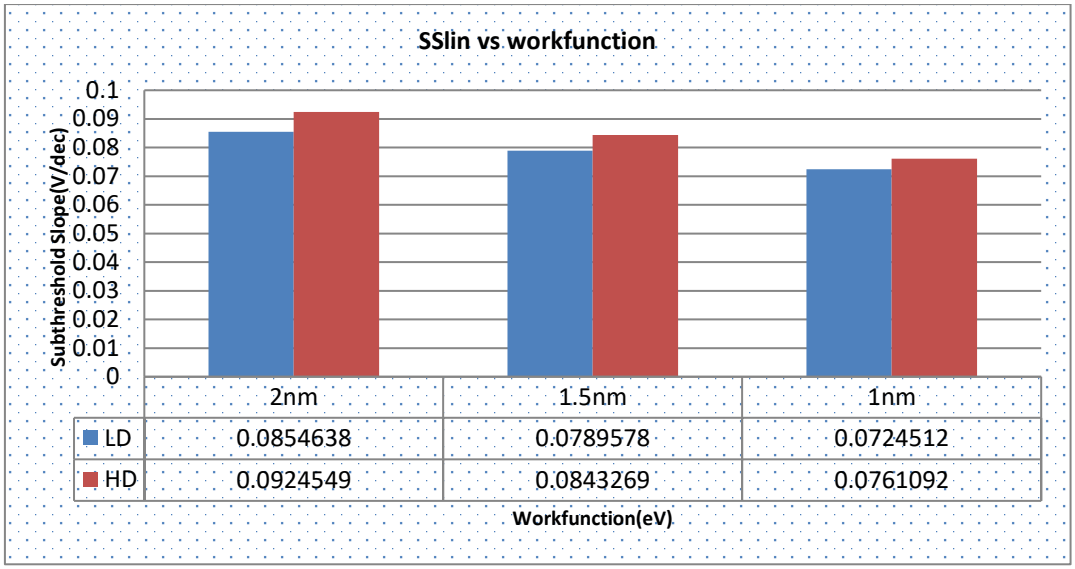


Figure 4.16 Variation of Sub-Threshold Slope with Gate Oxide Thickness

Figure 4.16 shows that there is a reduction in sub-threshold slope with t_{ox} in both lightly doped and heavily doped device but the lightly doped device has achieved reduced sub-threshold slope of 72 mV/decade as compared to heavily doped device. Table 4.1 shows the comparison of research work done here with previous research work.

Table 4.1 Comparison of Simulated Results with Literature

Parameters	LD NMOS S.Sharma et al [49]	LD NMOS (Simulated Data)	HD NMOS S.Sharma et al [49]	HD NMOS (Simulated Data)
V_t	0.254 V	0.251V	0.262 V	0.263V
Ion	2.14 mA	2.65 mA	1.88 mA	2.22 mA
Ioff	3.79 e-09 A	7.06 e-10A	2.69 e-09 A	4.50 e-10A
Ion/Ioff Ratio	5.63 e+05	3.76 e+06	6.98 e+05	4.94 e+06
SS	79.2 mV/dec	71.0 mV/dec	79.8 mV/dec	75.0 mV/dec
DIBL	36.3 mV/V	46.3 mV/V	32.0mV/V	35.3 mV/V

4.2 DESIGN CONSIDERATIONS OF N-CHANNEL DEVICE BY VARYING THE THRESHOLD VOLTAGE IMPLANT

Modeling and simulation of devices can be used to estimate any device's electrical characteristics. Scaling down MOSFETs leads to improved packaging density, speed, and power dissipation. Before performing a very expensive and time-consuming manufacturing process, virtual fabrication can be done using any Technology Computer-Aided Design (TCAD) tool to calculate design and manufacturing parameters which is a great tool for decreasing design expenses, enhancing device design yields and achieving superior device and technology designs. The threshold voltage, theoretically, is just the voltage applied gate-to-source to turn on an MOS device. By solving the one-dimensional Poisson Equation, the threshold voltage for a long channel device can be approximated:

For an n-channel device

$$V_T = V_{FB} + 2|\emptyset_p| + \frac{1}{c_i}\sqrt{2\varepsilon_s q N_a (2|\emptyset_p| - V_B} \quad (4.15)$$

Here V_{FB} is the flat-band voltage, c_i is the capacitance of the insulator, q is the density of the carrier, ε_s is the dielectric permittivity and V_B is the bias of the bulk. While

$$\emptyset_n = \frac{KT}{q} \ln \frac{n_i}{N_A} \quad (4.16)$$

N_A is the concentration of acceptor dopant in the substrate, k is the constant of Boltzmann, T is the absolute temperature, n_i is the intrinsic density of the electron. The threshold voltage is strongly dependent on doping concentration. Halo implant concentration and threshold implant concentration are two important parameters to adjust the vital parameters of the MOSFET [54]. The threshold voltage, sub-threshold current and DIBL can be adjusted during the fabrication process by adjusting the concentration of these two parameters to increase the device's efficiency. 45 nm NMOS device has been designed and virtually fabricated in ATHENA and ATLAS of the SILVACO TCAD tool. Atlas is a simulator of 2D and 3D devices that performs DC, AC and transient analysis for devices based on silicon, binary, ternary and quaternary material. Atlas allows semi-conductor devices to be characterized and optimized for a

wide range of technologies. The concentration of the halo implant and threshold implant is varied in this section to estimate the MOSFET's sub-threshold leakage current and substrate current [104]. A lightly doped NMOS with a channel length of 40 nm was designed in ATHENA and simulated in SILVACO TCAD tool ATLAS. Following simulation results, it is observed that as the threshold implant and halo implant concentrations increase, both off-state sub-threshold leakage and substrate current decrease as required for an ideal MOSFET. Other parameters have also been estimated such as ON current, DIBL and threshold voltage. The length of the physical gate is 40 nm and the substrate has a doping concentration of $5x10^{15}cm^{-3}$, $5x10^{12}$ cm^{-3} threshold implant and furthermore, the effects of concentration on leakage current, ON current, OFF current, DIBL, threshold voltage and substrate current are analysed differently. The drain current versus gate voltage characteristics is plotted after the design and simulation of the NMOS device as shown in Figure 4.17

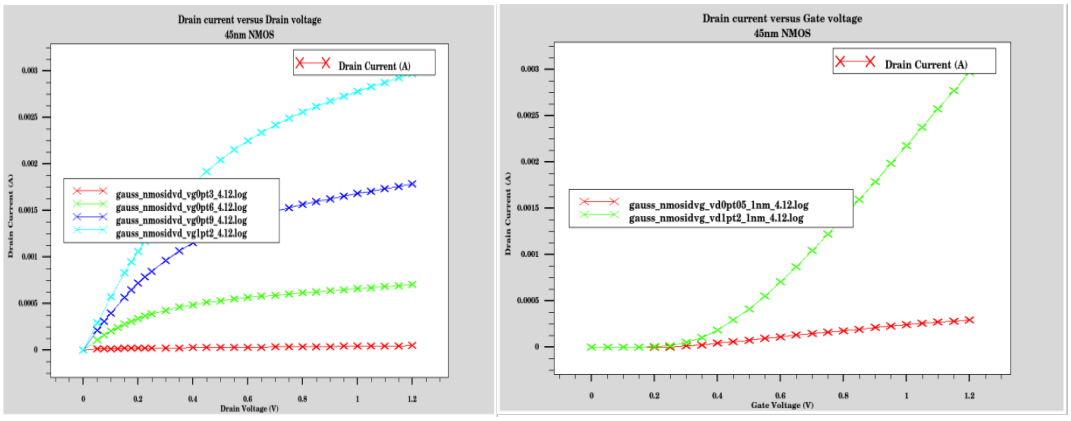


Figure 4.17 I_D - V_{DS} and I_D versus V_{GS} Plot in linear Scale for different gate voltages

MOS process consistently uses ion implantation now a days to perform doping the channel region which is also called the threshold adjust implant that alters the doping profile near the silicon substrate surface [105]. By altering the dose and energy of the threshold implant, the optimized threshold voltage can be achieved. The threshold voltage is a variable quantity and varies with the source to bulk voltage. Figure 4.18 shows the structure with different threshold implants and characteristics of drain current are as shown in Figure 4.19 below.

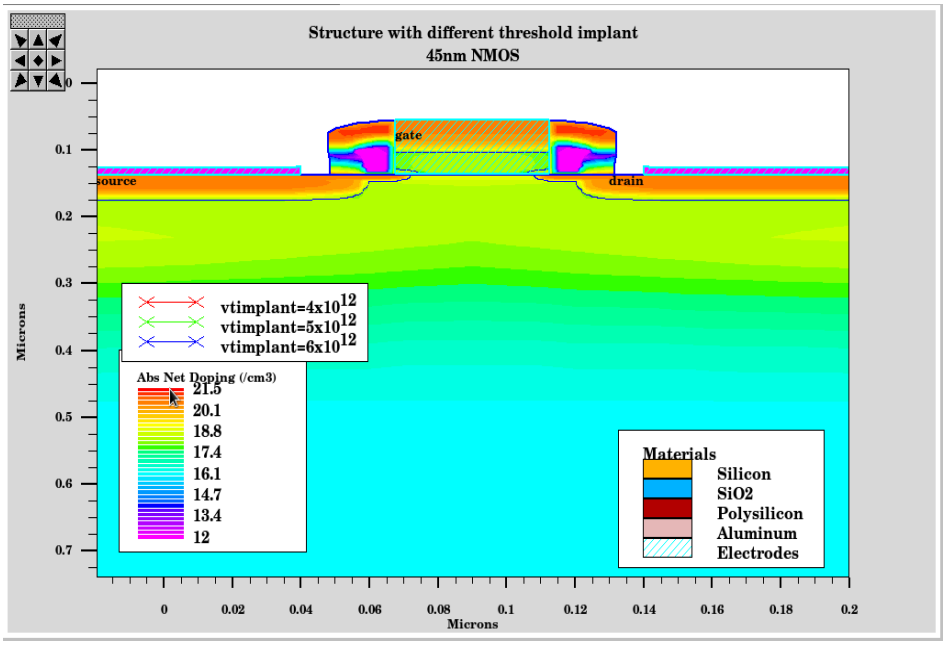


Figure 4.18 NMOS Structure with different threshold implants

As the threshold implant concentration increases, the threshold voltage increases as shown in Figure 4.19 and the drain current begins to decrease. The threshold voltage adjustment of this implant is basically required.

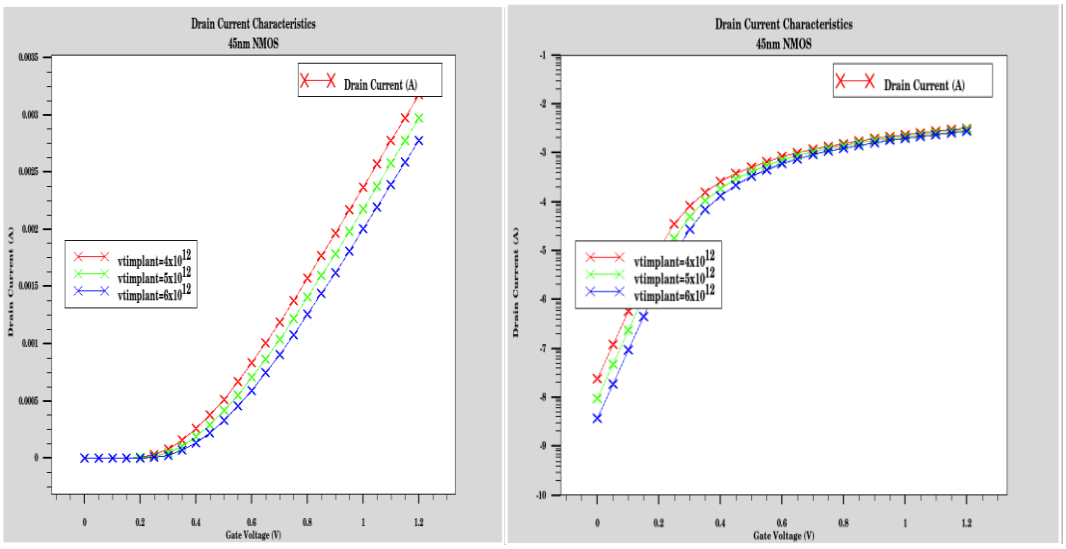


Figure 4.19 I_D -V_{GS} and I_D -V_{GS} plot in linear Scale for Different Threshold Implants

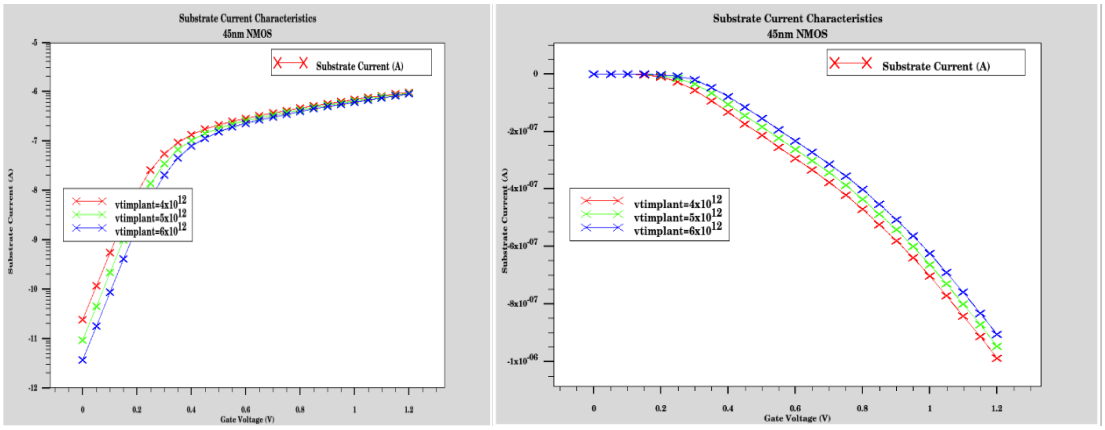


Figure 4.20 I_{SUB} - V_{GS} Plot in Linear and Log Scale for different Threshold implants

As the concentration of the threshold implant increases, the substrate current of the device decreases as needed for an ideal device. After simulation in the ATLAS simulator, various parameters are extracted. It shows that as the concentration increases, the ON current decreases, the OFF state leakage current decreases, the ON / OFF ratio increases, the sub-threshold slope improves, the substrate current decreases and the DIBL decreases play a significant role in leakage current of the device [10] [104] as shown in Figure 4.20

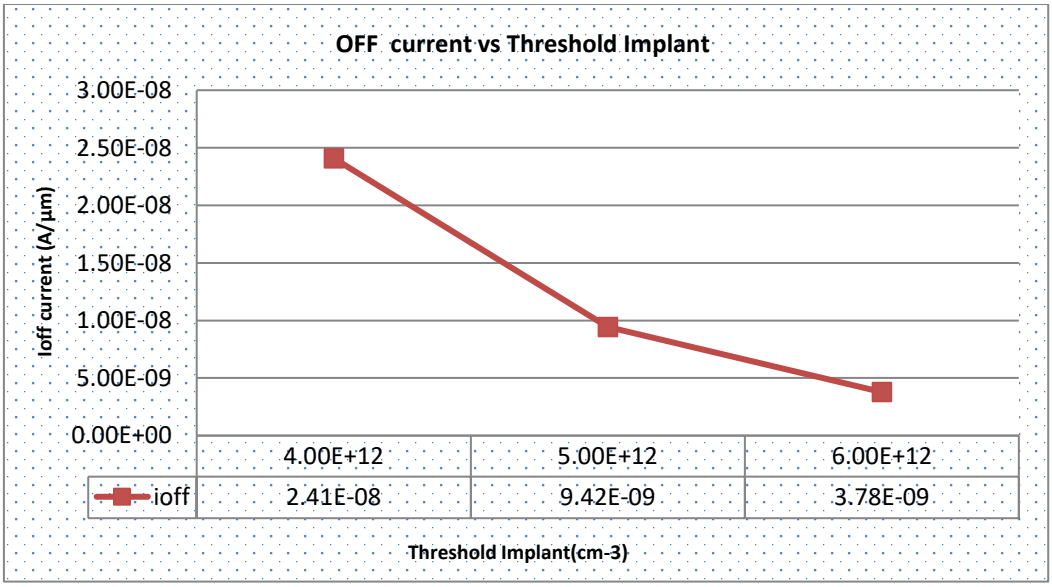


Figure 4.21 OFF current at different Threshold implants

Figure 4.21 shows the decrease of OFF-state leakage current in the subthreshold region at different threshold implant concentrations.

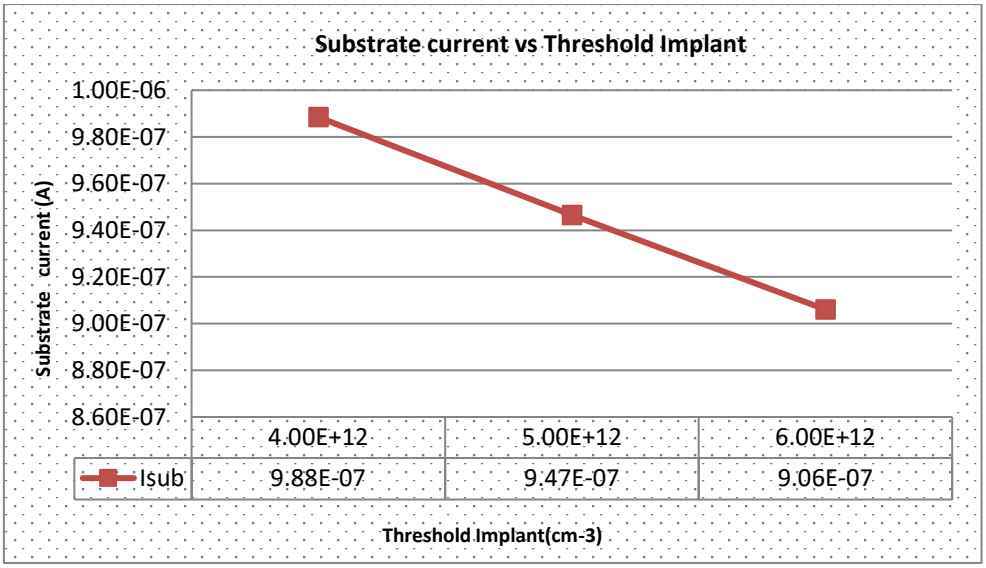


Figure 4.22 Substrate current at different Threshold implants

Figure 4.22 shows the decrease in substrate current as the threshold adjusts implant increases.

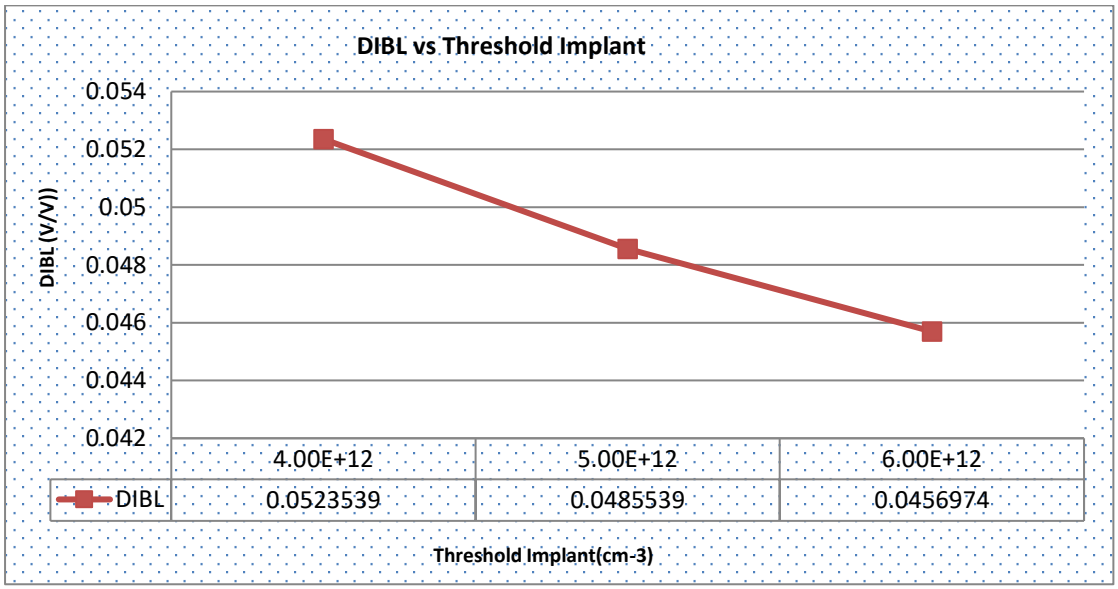


Figure 4.23 DIBL at different Threshold implants

Figure 4.23 shows that the Drain current barrier lowering (DIBL) decreases as the threshold voltage implant concentration increases. The threshold voltage is a measure of the barrier strength from the source to the channel against carrier injection. The depletion region formed in the drain area has reduced the potential barrier from the source to the channel junction as the voltage between the source and drain increases.

This section concludes that to get the optimized device, the threshold implant's best value appears to be $5x10^{12}$ cm^{-3}.

4.3 DESIGN CONSIDERATIONS OF N-CHANNEL DEVICE BY VARYING HALO IMPLANT

Another method that can shrink short channel effects and thus control the threshold voltage roll-off is the variation in the concentration of halo/pocket implants. Another way to regulate threshold voltage dependence on channel length is halo doping or non-uniform channel profile in a lateral direction. Very highly p-doped regions are created near ends of the channel for n-channel MOSFETs which reduces the source and drain charge-sharing effects. The effects of charge sharing are reduced which further reducing the threshold voltage of the device. The threshold voltage thus becomes almost independent of the length of the channel. Hence, the off-state leakage current becomes less sensitive to the variation in channel length.

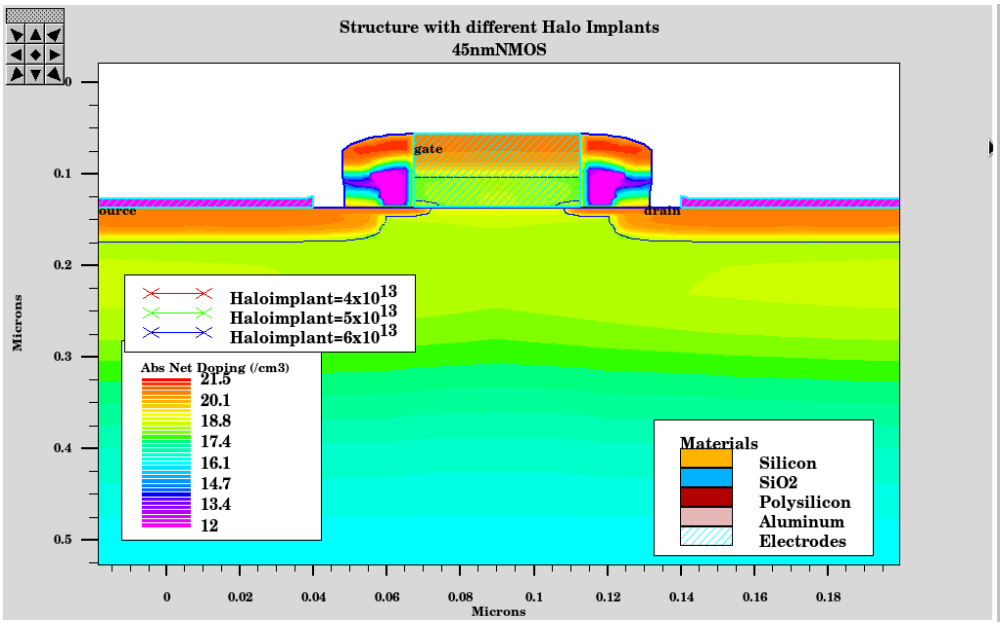


Figure 4.24 NMOS Structure with different Halo implants

Figure 4.24 shows the structure with different pocket implant concentrations.

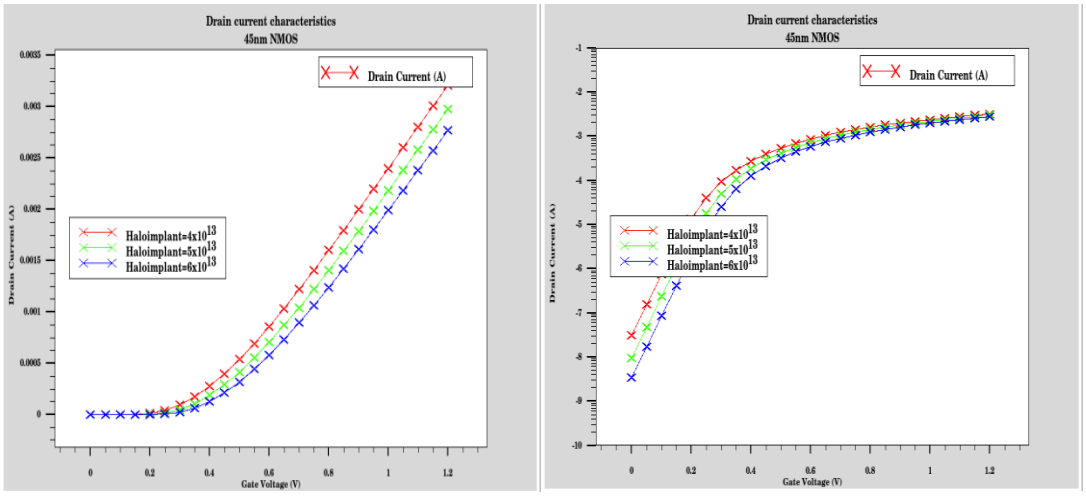


Figure 4.25 I_D - V_{GS} Plot in linear Scale and Log scale for different Halo implants

Figure 4.25 shows the linear and log scale variation of drain current with gate voltage at various drain voltages. As halo implant concentration increases, the threshold voltage increases and the device current decreases [106]. This implant is primarily intended to reduce the off current by neglecting the device's current.

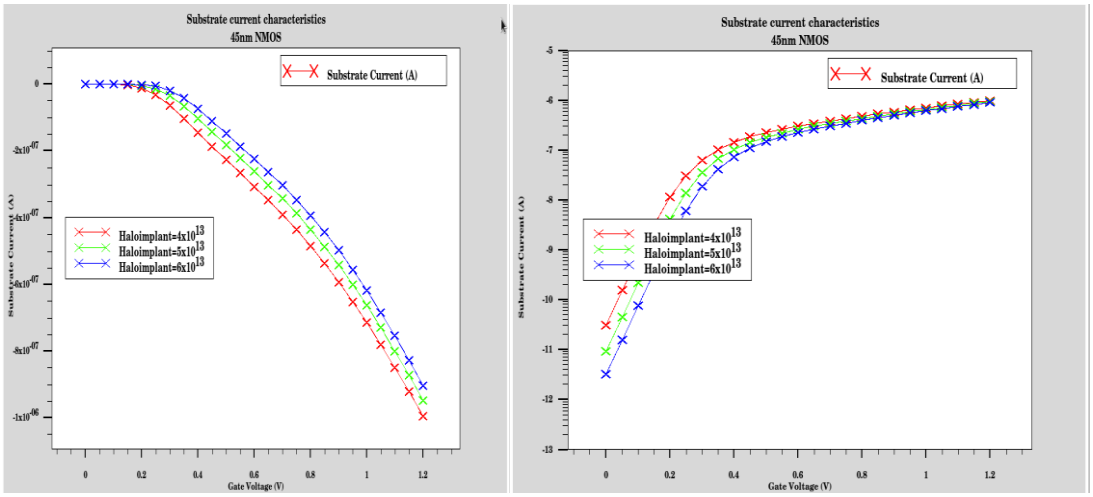


Figure 4.26 I_{SUB} - V_{GS} Plot in linear and log scale for different Halo implants

Figure 4.26 represents the decrease of substrate current with the increase of Halo Implant Concentration. As the halo implant concentration increases, threshold voltage increases, ON current decreases, sub-threshold leakage current decreases, ON/OFF ratio increases, the sub-threshold slope has been improved, substrate current and DIBL decreases which contribute in short channel effects.

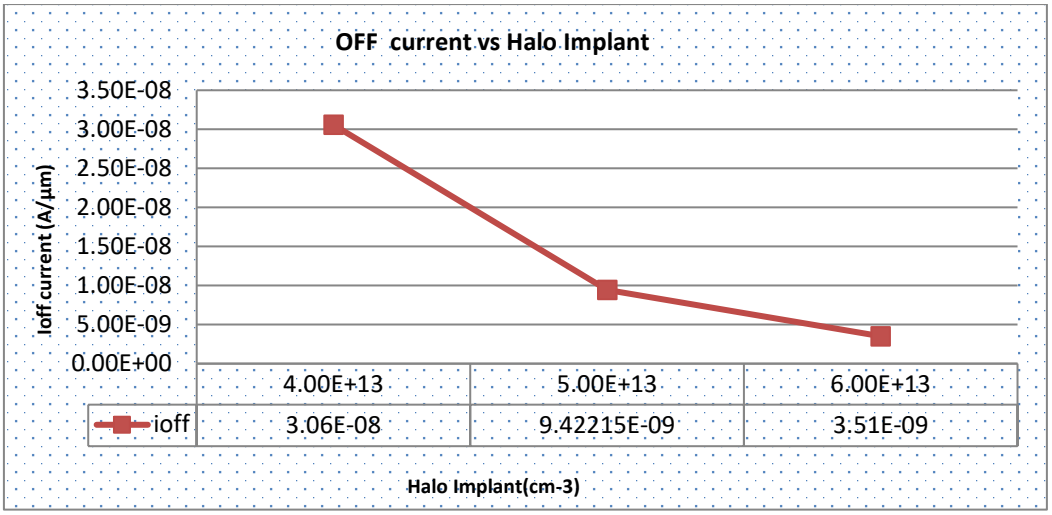


Figure 4.27 OFF current at different Halo implant

Figure 4.27 shows the decrease of OFF current with the increase in Halo Implant Concentration.

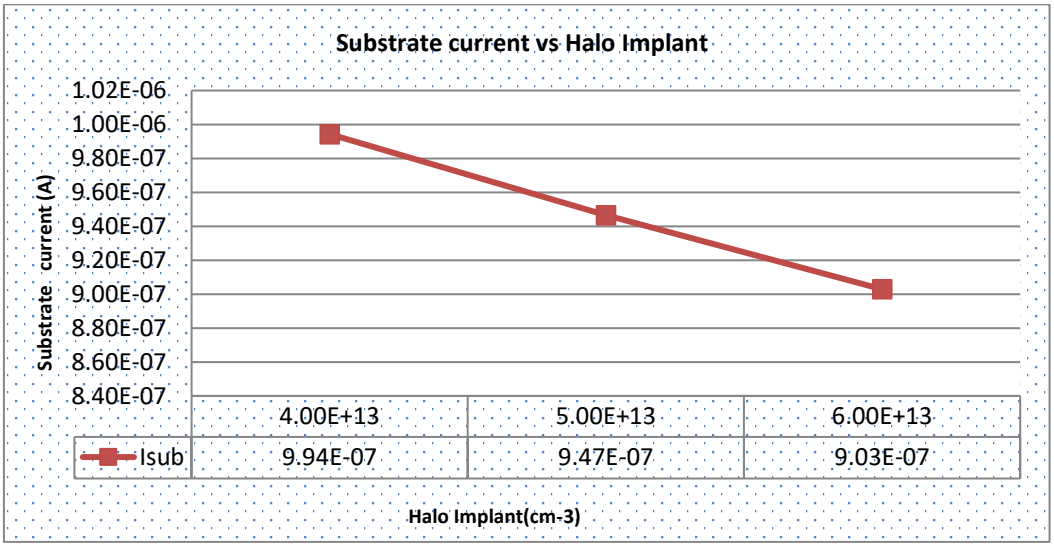


Figure 4.28 Substrate Current at Different Halo Implant

Figure 4.28 shows a reduction in substrate current with an increase in the concentration of Halo Implants

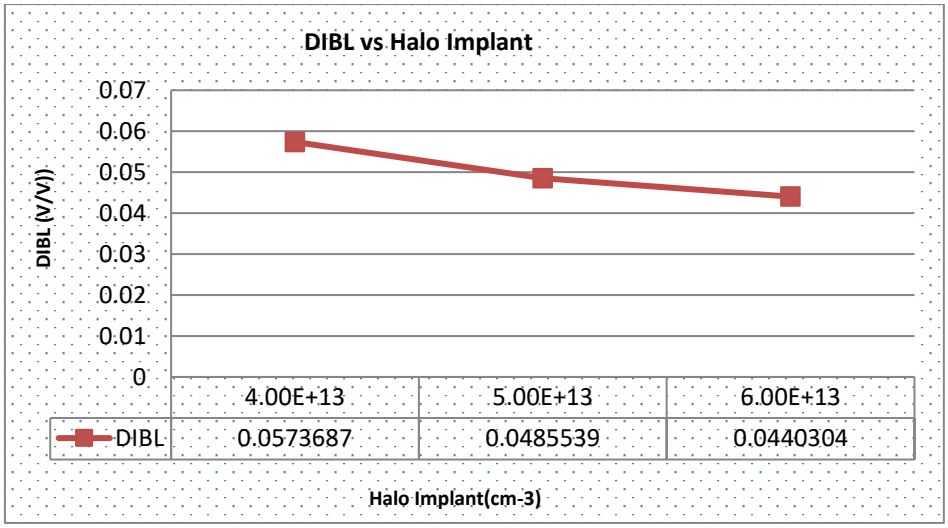


Figure 4.29 DIBL at Different Halo implant

Figure 4.29 shows a reduction in DIBL with an increase in the concentration of halo implants. When the barrier between the source and the channel is lowered, more electrons will be added to the channel region initiating additional injection of charge carriers into the channel region and providing increased off-state leakage current. This results in lowering the threshold voltage and lowering the channel current control by the gate. This is known as DIBL.

4.4 DESIGN CONSIDERATIONS OF N-CHANNEL DEVICE BY VARYING POLY DOPING

Polycrystalline silicon can be deposited on arbitrary substrates and does not need exposed silicon underneath. It is used as the gate electrode in CMOS technology and for local interconnects and resistors [107]. Its excellent heat stability, excellent interface with silicon dioxide, excellent conformity and easy deposition and handling make it a core of silicon microelectronics technology. Depending on P or N channel MOSFET, polysilicon can be doped either n-type or p-type [108]. The source and drain doping profiles are modeled using Gaussian distribution or Pearson distribution. A 45nm NMOS is fabricated using Gaussian doping profile of Poly-silicon layer and Source-drain regions. Poly-silicon doping and Source/Drain doping are two important parameters to adjust the various parameters of the MOSFET. The OFF current, threshold voltage, sub-threshold current and DIBL can be adapted to enhance the device efficiency during the fabrication process. The concentration of poly-silicon doping and Source / Drain doping was varied in this research work to achieve the approximation of

the N channel MOSFET sub-threshold leakage current [109]. A lightly doped NMOS was developed using 45 nm ATHENA technology and simulated in the SILVACO TCAD tool ATLAS. After simulation results, it has been observed that as the poly-silicon doping and source-drain doping concentrations are decreased, there is a decrease in off-state leakage current, substrate current and DIBL. The ON/OFF current ratio has also been increased. The physical gate length is 40nm and the substrate is lightly doped having a doping concentration of $5x10^{15}$ cm^{-3}. Initially, the device is designed using poly doping of concentration $1.5x10^{15}cm^{-3}$and Source/Drain doping of concentration $3.5x10^{15}cm^{-3}$. It is varied to analyze the effects of concentration on off-state leakage current, ON current, DIBL, threshold voltage and substrate current. The drain current versus gate voltage characteristics is plotted after the design and simulation of the NMOS device as shown in Figure 4.30

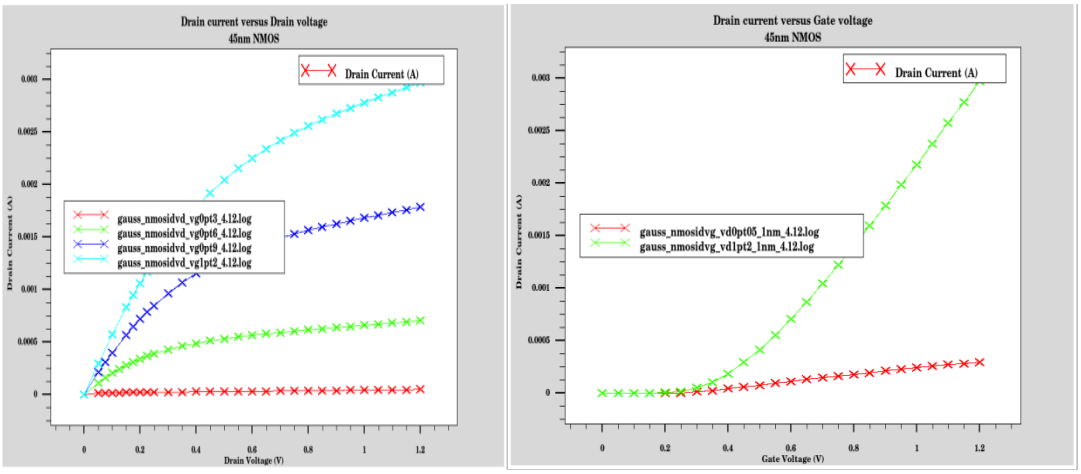


Figure 4.30 I_D -V_{DS} Plot and I_D -V_{GS} Plot in Linear Scale for different Gate voltages

The Poly-silicon material is a conductive material which acts as a gate material in MOSFETs. The concentration of Poly material affects the electrical characteristics of the device. In this section, the variation of concentration of Poly-Si material is shown after the simulation with various concentrations. The structure with different Poly-Silicon Concentration is as shown in Figure 4.31.

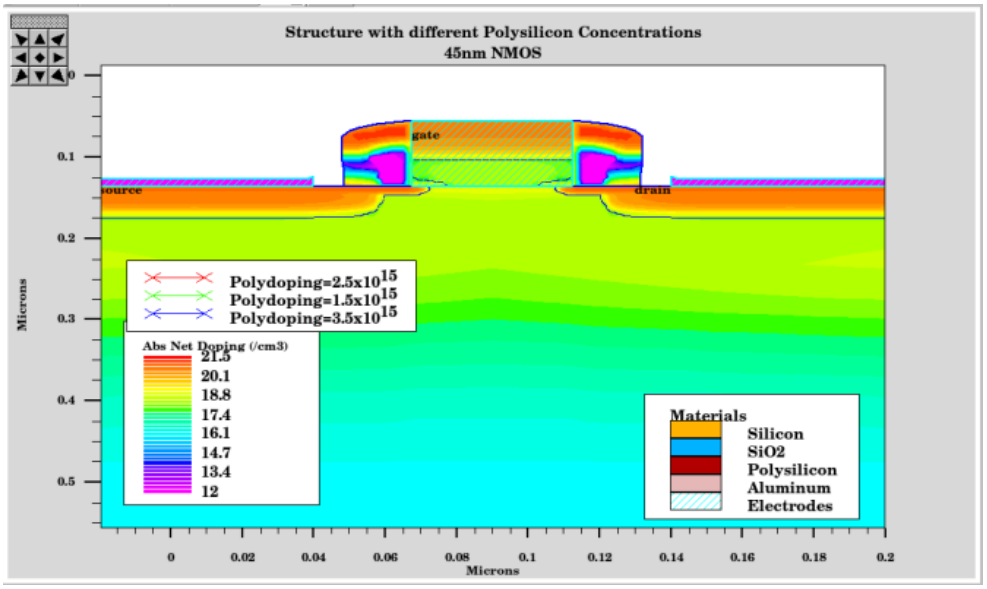


Figure 4.31 NMOS Structure with different Poly-Silicon Concentration

As Poly-silicon gate doping reduces, the threshold voltage improves the drain current as shown in Figure 4.32. As the Poly-silicon concentration decreases, the substrate current of the device decreases as required for an ideal device.

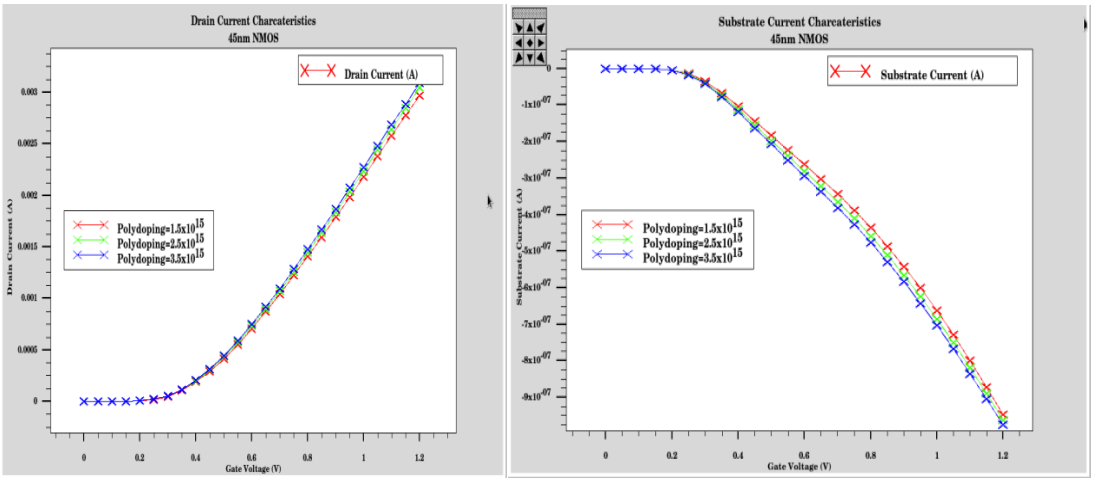


Figure 4.32 I_D-V_{GS} Plot and I_{SUB} -V_{GS} Plot in Linear Scale for Different Poly Doping

Its simulation findings indicate that as the concentration reduces, the ON current reduces, the OFF state leakage current decreases, the ON / OFF ratio improves, the sub-threshold curve improves, the substrate current reduces and the DIBL reduces which plays a significant part in the device's leakage current.

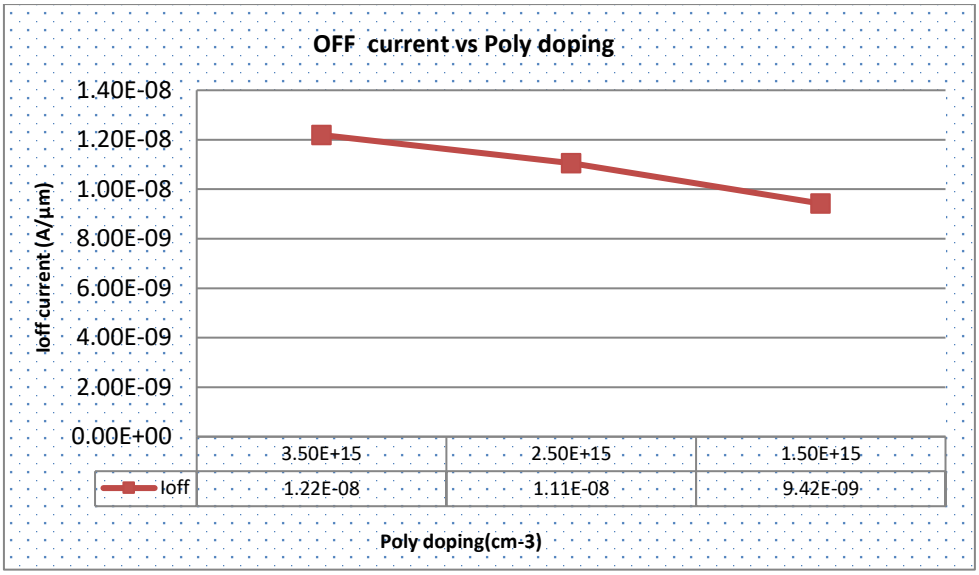


Figure 4.33 OFF current at different Poly-Silicon Concentration

Nowadays, Off-state leakage current contributes a lot in short channel effects. Figure 4.33 shows the decrease of OFF-state leakage current in the subthreshold region at different Poly-Silicon Concentrations.

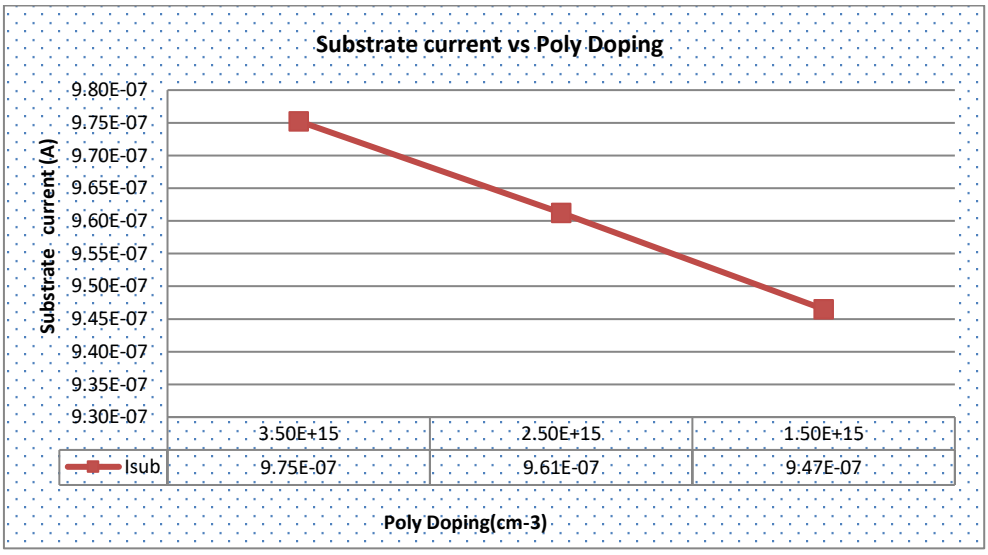


Figure 4.34 Substrate Current at different Poly-Silicon Concentration

The Poly-Silicon doping is decreased from $3.5x10^{15}$ cm^{-3} to $1.5x10^{15}$ cm^{-3} then the substrate current decreases as shown in Figure 4.34 above.

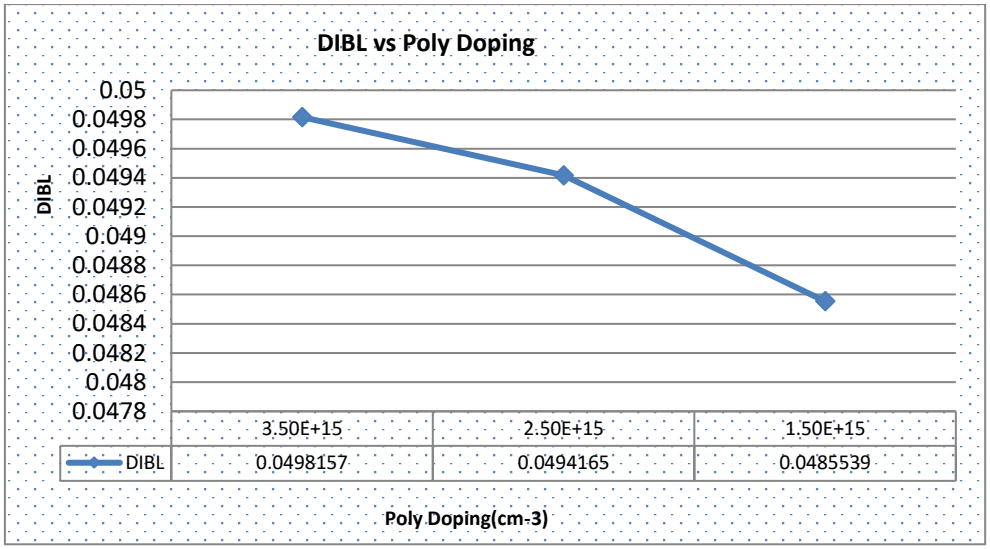


Figure 4.35 DIBL at different Poly-Silicon concentration

Drain-Induced Barrier Lowering (DIBL) is also a short-channel effect observed in MOSFETs that initially refers to reduce the transistor threshold voltage at greater drain voltages. Poly doping decreases, the rise in threshold voltage results in a reduction in the DIBL effect. Figure 4.35 shows that as the concentration of Poly-Silicon Concentration decreases, the Drain Current Barrier Lowering (DIBL) decreases.

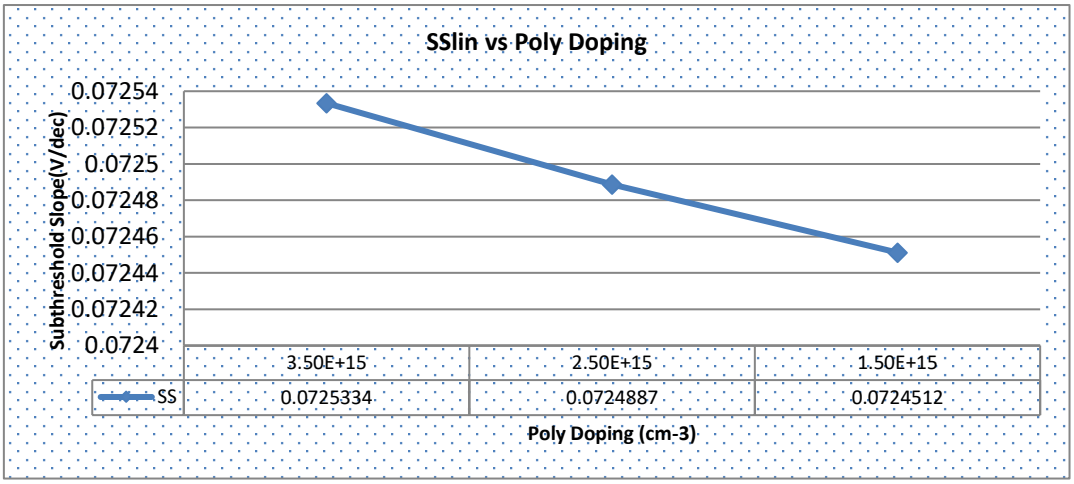


Figure 4.36 Variation of SS with Poly Doping

The decrease of the subthreshold slope with poly doping is shown in Figure 4.36. From the above analysis, it has been observed that as the poly-silicon doping is decreased from $3.55x10^{15}$ cm^{-3} to $1.5x10^{15}$ cm^{-3}, the threshold voltage increases, ON current decreases, OFF-state leakage current decreases, On/Off current ratio increases, substrate current and DIBL decreases.

4.5 DESIGN CONSIDERATIONS OF N-CHANNEL DEVICE BY VARYING SOURCE/DRAIN DOPING

The two regions named Source and Drain of the MOSFET are heavily doped with an n-type impurity having Gaussian Doping Profile. The doping concentration is considered during fabrication is $3.5x10^{15}$ cm^{-3}.

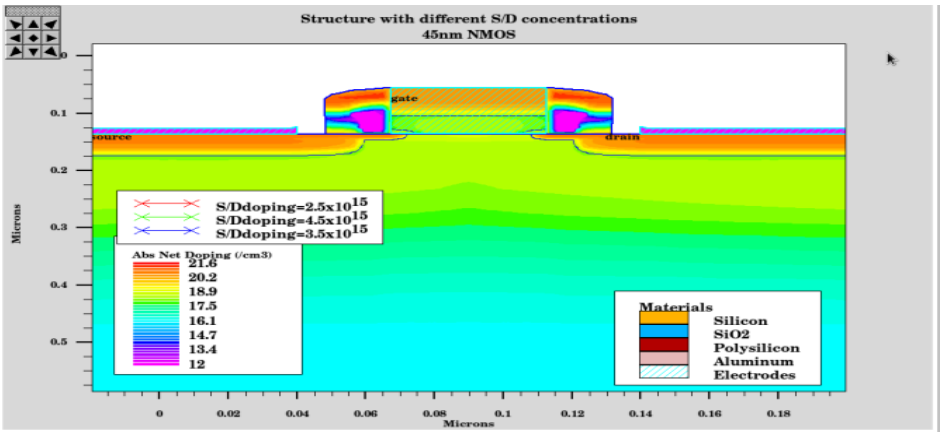


Figure 4.37 NMOS Structure with Different Source/Drain Concentration

In this section, the effect of variation of source and drain doping concentration is shown after simulating NMOS device [110]. Figure 4.37 shows the structure with different Source/Drain Concentration and the drain characteristics are as shown in Figure 4.38

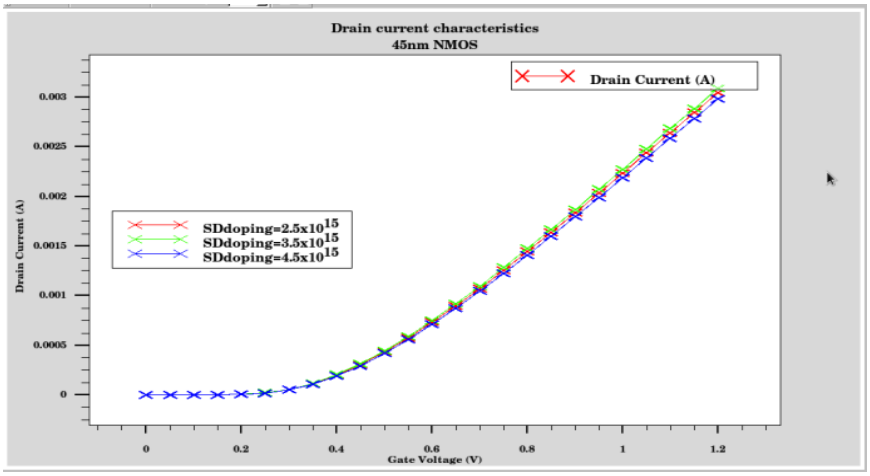


Figure 4.38 I_D - V_{GS} Plot in Linear Scale for Different Source/Drain Concentration

As the Source / Drain concentration decreases, the threshold voltage increases and the device ON current decreases. This implant is basically for reducing the off current neglecting on the current of the device. As the Source/Drain Concentration decreases,

threshold voltage increases, ON current decreases, OFF-state leakage current decreases, ON/OFF ratio increases, substrate current and DIBL decreases which contribute in short channel effects.

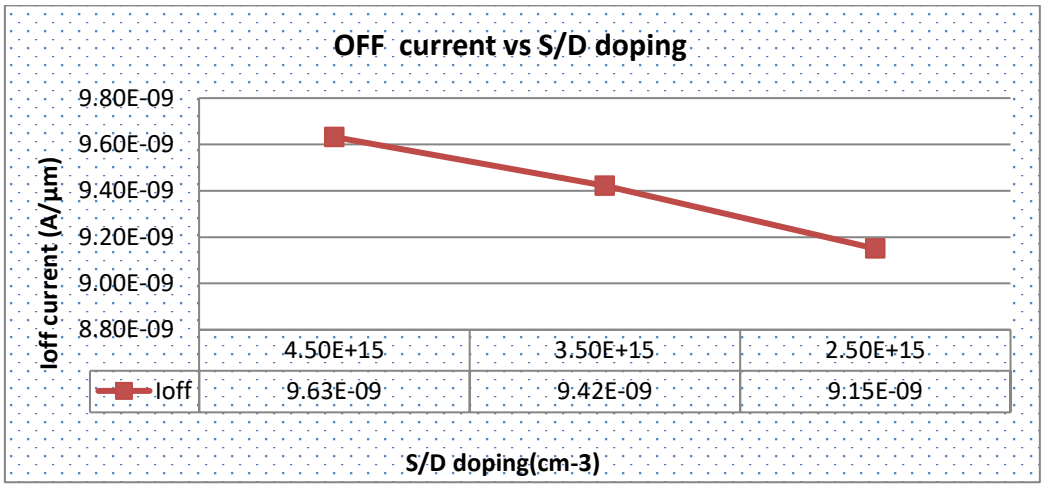


Figure 4.39 Off current at Different Source/Drain Concentration

Substrate current is a measure of hot electrons injected into the substrate during unfavorable conditions between the gate and drain voltages for hot electron generation at the drain. Figure 4.39 shows the decrease of OFF current with the decrease in Source/Drain Concentration

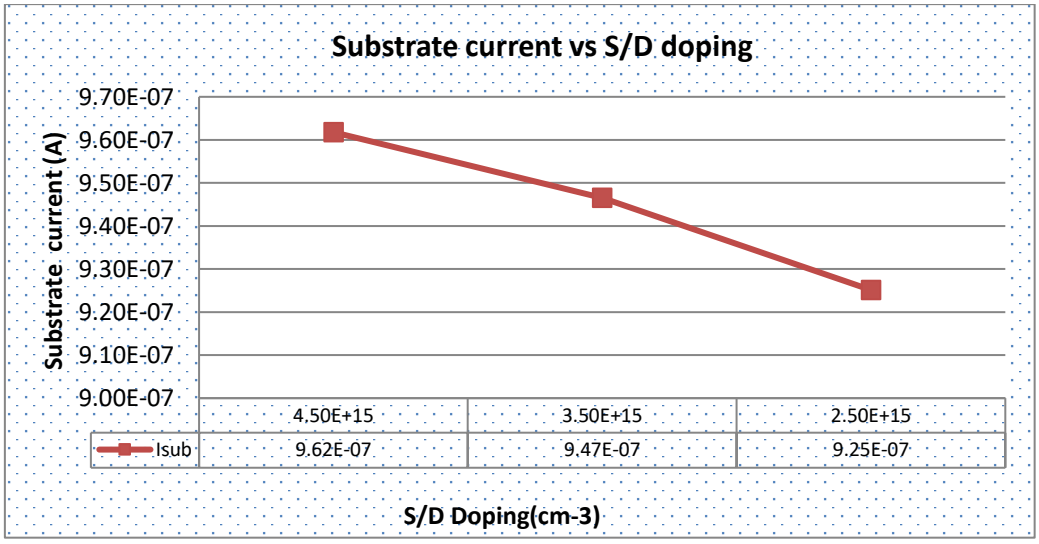


Figure 4.40 Substrate current at Different Source/Drain Concentration

Figure 4.40 shows the decrease of substrate current with the decrease in Source/Drain Concentration.

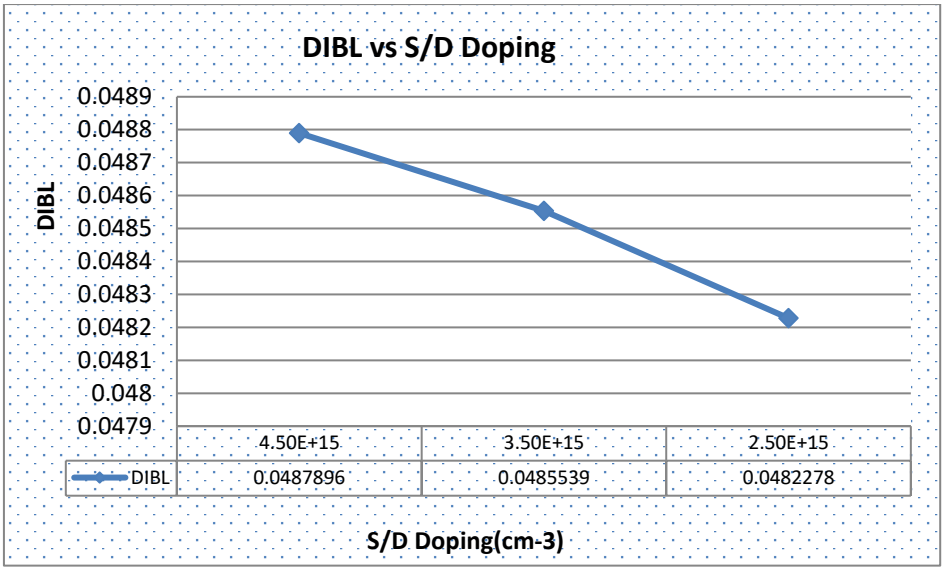


Figure 4.41 DIBL at different Source/Drain Concentration

Figure 4.41 shows the decrease of DIBL with the decrease in Source/Drain Concentration. From the above analysis, it has been observed that as the S/D doping is decreased from $4.5x10^{15}$ cm^{-3} to $2.5x10^{15}$ cm^{-3}, the threshold voltage increases, ON current decreases, OFF-state leakage current decreases, ON/OFF current ratio increases, substrate current and DIBL decreases.

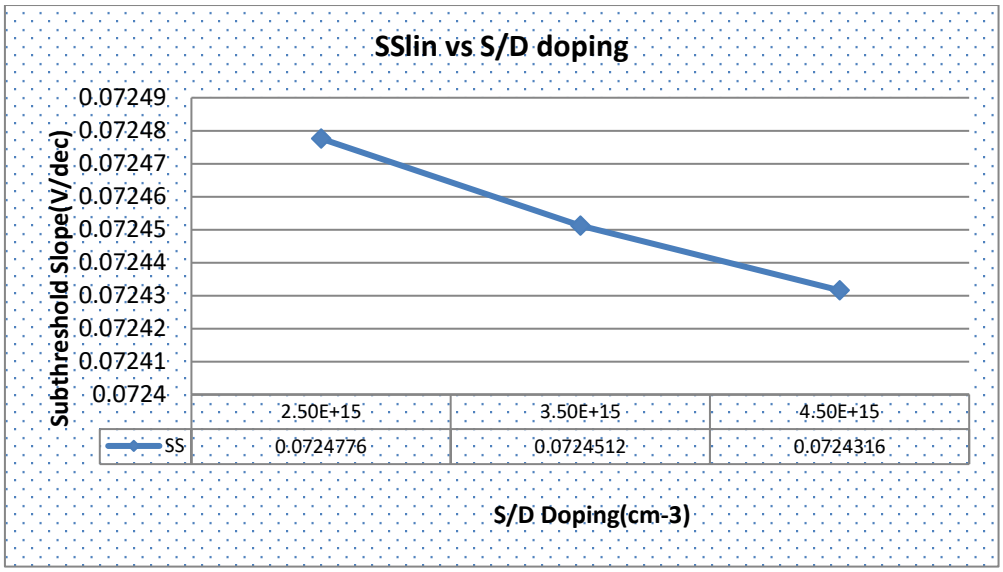


Figure 4.42 Variation of SS with S/D doping

The sub-threshold slope improves by increasing the S/D doping concentration to 4.5x 10^{15} cm^{-3}. The variations of SS with source-drain doping are as shown in Figure 4.42.

4.6 DESIGN CONSIDERATIONS OF N-CHANNEL DEVICE BY VARYING THE DOPING DISTRIBUTIONS

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are the cornerstone of today CMOS Technology. The current research in this field is mainly aimed at increasing the density of the device through a destructive scaling of the device feature sizes. Doping goes into to the addition to a semiconductor of specified impurities to alter its electrical properties. The amount of impurities that can be added to Silicon is dependent on the solubility of the solid opted. The gate tunneling in the MOSFETs can be reduced by using the high-k dielectric gate, while in a MOSFET with a channel length of approximately 10 nm; the off-current is a significant value leading to an increase in the sub-threshold swing (SS) [111] and a reduction in both the drain-induced barrier and the threshold voltage. Channel Doping is also a technique to reduce the short-channel effects and controls the threshold voltage [46]. In addition, it should be noted that due to the ion-implantation steps required during the fabrication process, the nature of the actual in-practice transistor-channel doping profile becomes closer to that of the Gaussian and Pearson Doping Profile. In this section, Gaussian and Pearson Doping Profiles of Source/Drain regions are considered to compare the electrical characteristics of lightly doped NMOSFET [69]. The effects of drift parameter (Gaussian or Pearson doping profile in the S/D region), ON current, OFF-state leakage current, On/Off ratio and threshold voltage have been investigated. The virtual fabrication is performed in ATHENA and then simulated with ATLAS of SILVACO TCAD tool [37]. Gaussian and Pearson Doping Profile used to control the short-channel effects in the Single Gate MOSFET. These are investigated with the use of a two dimensional (2D) quantum simulation where MOSFET channel length is of 40 nm. The model results suggested are validated by comparing them with the corresponding SILVACO TCAD simulation data obtained using a 2D ATLAS tool, SILVACO two-dimensional Device Simulator. It has been observed that Pearson Doping Profile gives the best performance in the terms of reduced leakage current equals to 6.92924nA and Gaussian Doping Profile gives the best performance in terms of substrate current. The absolute net doping profiles are also compared for both Gaussian and Pearson Doping Profiles. The effect of gate oxide thickness is also varied and drain current characteristics have been plotted with various gate oxide thicknesses.

(a) Gaussian Doping Profile

In this scenario, at the beginning of the diffusion process, the total amount of dopant atoms is a constant and the concentration of atoms on the surface steadily decreases over time. Let Q_T be the total amount of dopants per unit area on the surface (at the beginning of the diffusion). The concentration, C(x, t), is given by

$$C(x,t) = D_T\sqrt{\pi Dt}\ \exp\left(-x^2.4D_T\right. \tag{4.17}$$

For a constant concentration of the surface, this is a Gaussian function. It is possible to obtain the change in surface concentration as a function of time from Equation 4.18 with x = 0. This gives

$$\mathrm{C}(0,\mathrm{t}) = \mathrm{QT}\sqrt{\pi \mathrm{D_T}} \tag{4.18}$$

(b) Pearson Doping Profile

Gaussian distribution is used for symmetric doping. Pearson distribution is used for asymmetrical cases. With the following differential equation, Pearson Function can be solved:

$$\frac{\mathrm{df(x)}}{\mathrm{dx}} = \frac{\mathrm{(x-a)f(x)}}{\mathrm{b_0+b_1x+b_2x^2}} \tag{4.19}$$

where f(x) is the function of frequency. The constants a, b_0, b_1 and b_2 are associated with f(x) moments:

$$a = -\frac{\Delta R_p \gamma(\beta+3)}{A}\ ,\ b_0 = -\frac{\Delta {R_p}^2(4\beta+3\gamma^3)}{A}\ ,\ b_1 = a,\ b_2 = -\frac{2\beta-\gamma^2-6}{A}$$

where A = 10β −12γ2 −18, with γ and β, are the skewness and kurtosis, respectively.

A 40 nm MOSFET was virtually fabricated for this research work using the SILVACO ATHENA [38] module and simulated the device's electrical features using the SILVACO ATLAS module. The device's requirements are drawn with a p-type silicon substrate with a doping concentration of $5x10^{15}$ cm^{-3} and <100> orientation. The substrate is taken with low doping concentration. The p-well implantation was doped with Boron at $1x10^{12}$ cm^{-3} doping concentration. The threshold implant layer was

then implanted to adjust the device's threshold voltage. The concentration of threshold implant adjust was considered as $5x10^{12}$ cm^{-3}. The source-drain doping concentration was taken as $3.5x10^{15}$ cm^{-3}. After the design and fabrication, the combined structure of the fabricated NMOS device with Gaussian and Pearson Doping Profiles is demonstrated in Figure 4.43.

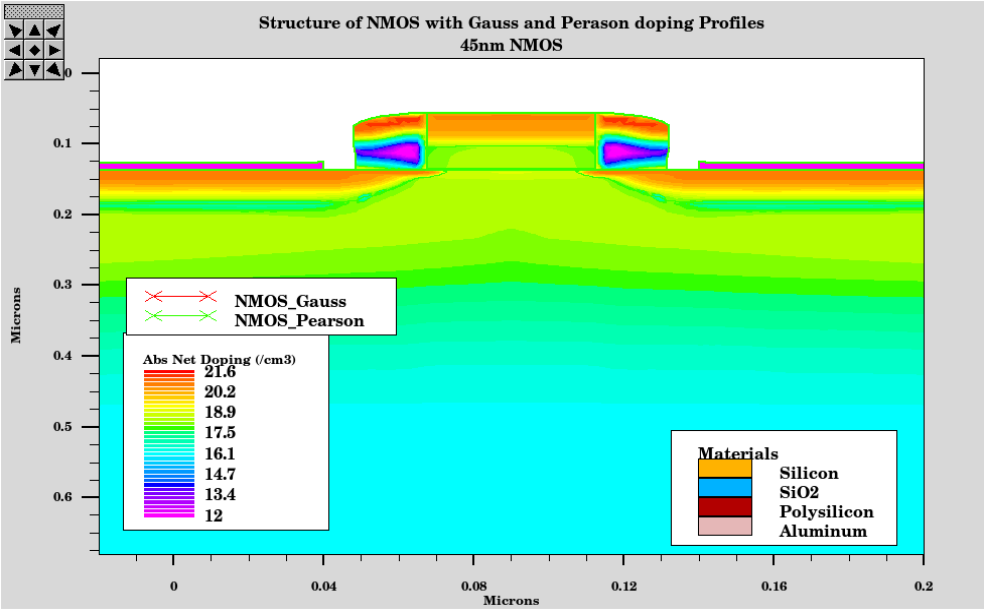


Figure 4.43 Structure of NMOS with Gauss and Pearson doping profile

A 40 nm gate-length NMOS device of 45 nm is designed and fabricated. Based on ON current, OFF current, on/off current ratio, Substrate current, sub-threshold slope, and DIBL, the comparison of both doping distributions are made. Based on simulation outcomes, the comparative findings were shown in this chapter. The absolute net doping concentration of both profiles is as shown in Figure 4.44.

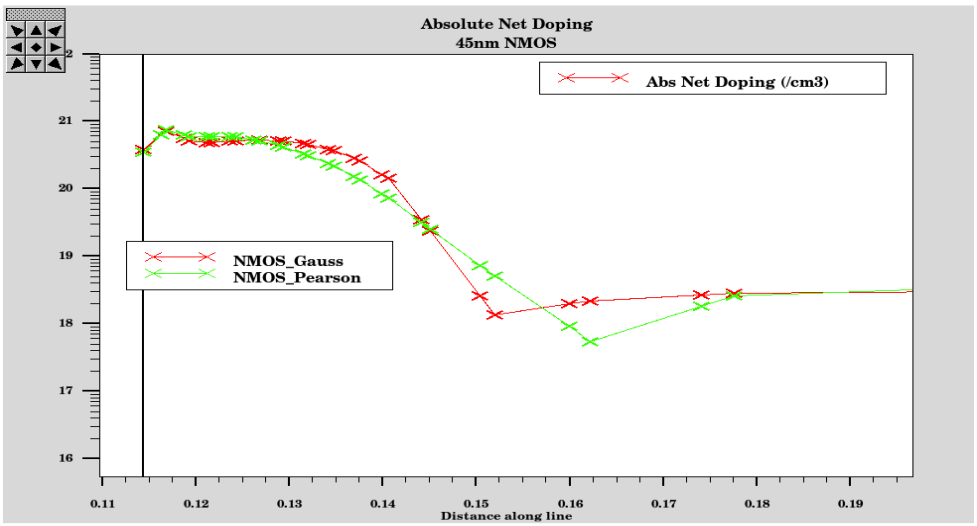


Figure 4.44 Absolute net doping of NMOS with Gaussian & Pearson Doping Profile

The absolute net doping at source and drain ends is as shown in Figure 4.45 .

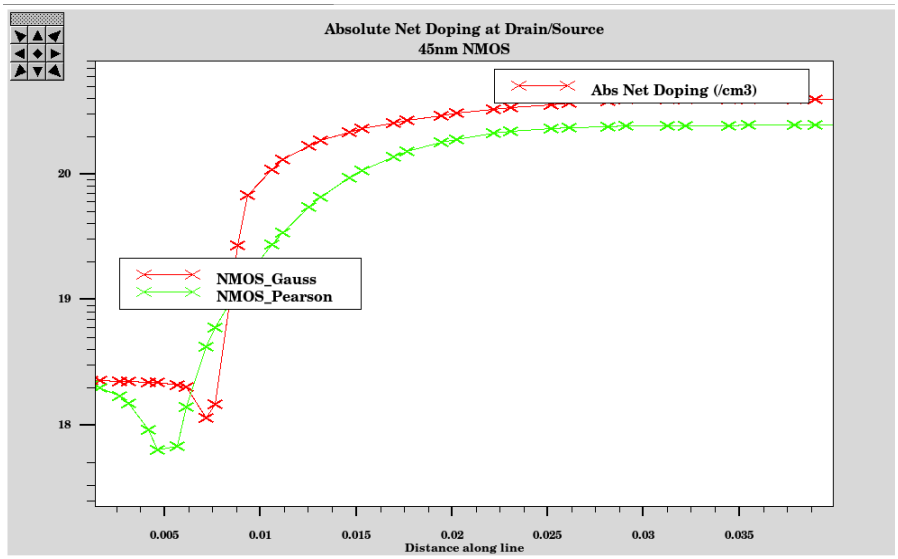


Figure 4.45 Net doping with Gaussian & Pearson Doping Profile at Drain/Source

In the ATLAS SILVACO tool, the drain current characteristics of 45 nm NMOS are simulated with different drain current versus gate and drain voltage, gate current versus drain voltage and gate voltage, substrate current versus gate voltage and drain voltage. The features of the drain current are shown in Figures below.

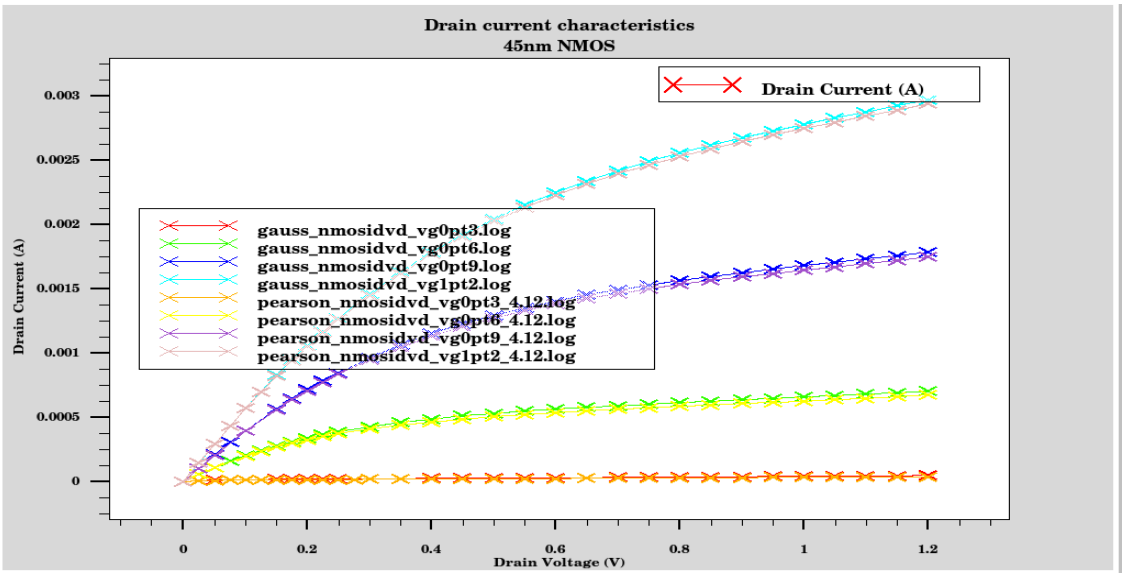


Figure 4.46 I_D-V_{DS} of NMOS with Gaussian & Pearson Doping Profile

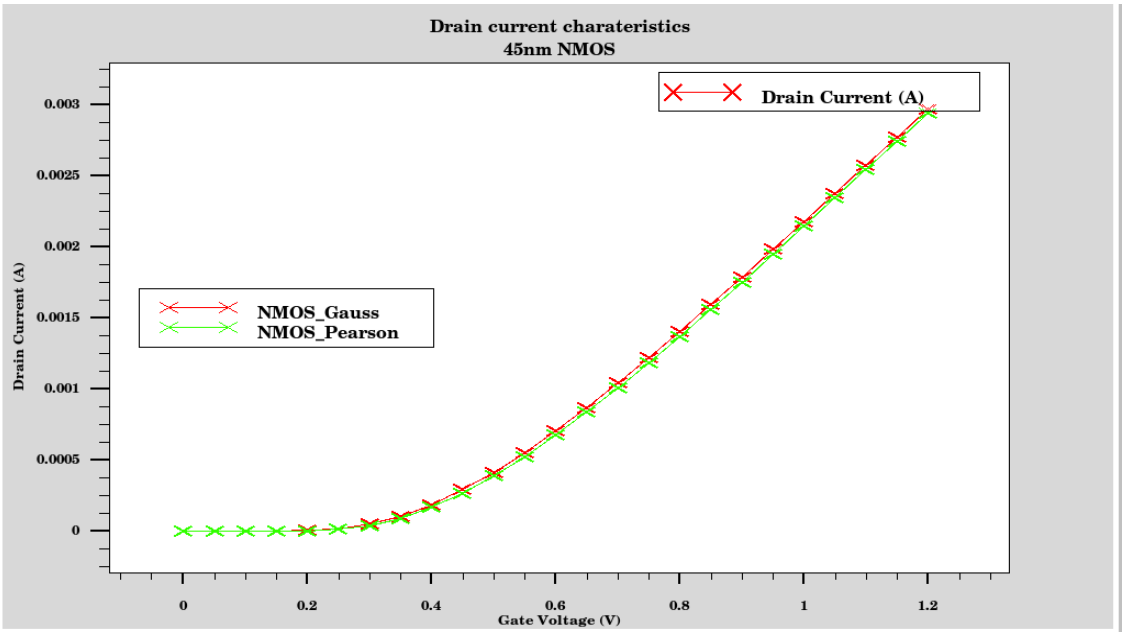


Figure 4.47 I_D -V_{GS} of NMOS with Gaussian & Pearson Doping Profile

The drain current versus drain voltage and gate voltage are shown in Figure 4.46 and Figure 4.47. It demonstrates the variation of drain current at distinct gate voltages with drain voltage and drain current at different drain voltages with gate voltage. The supply voltage is 1.2V. The peak drain current is estimated at 2973µA in the Gaussian Doping Profile and 2941µA for Pearson. The gate and drain voltage range is as shown in Figure 4.48 and Figure 4.49.

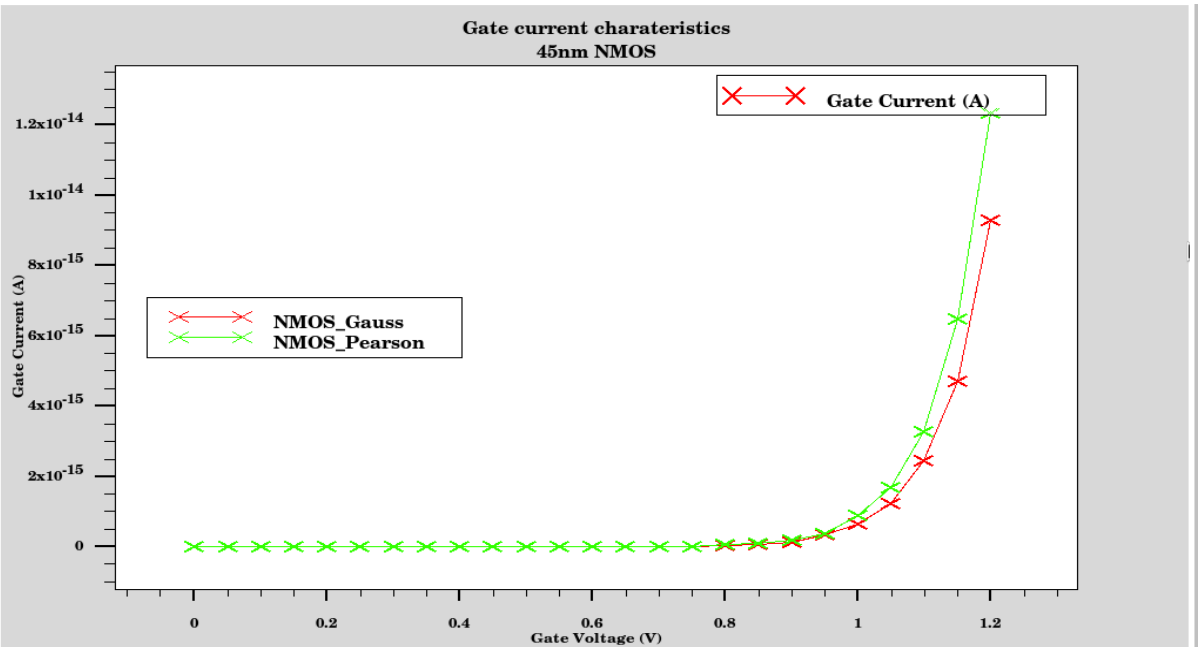


Figure 4.48 I_G - V_{GS} of NMOS with Gaussian & Pearson Doping Profile

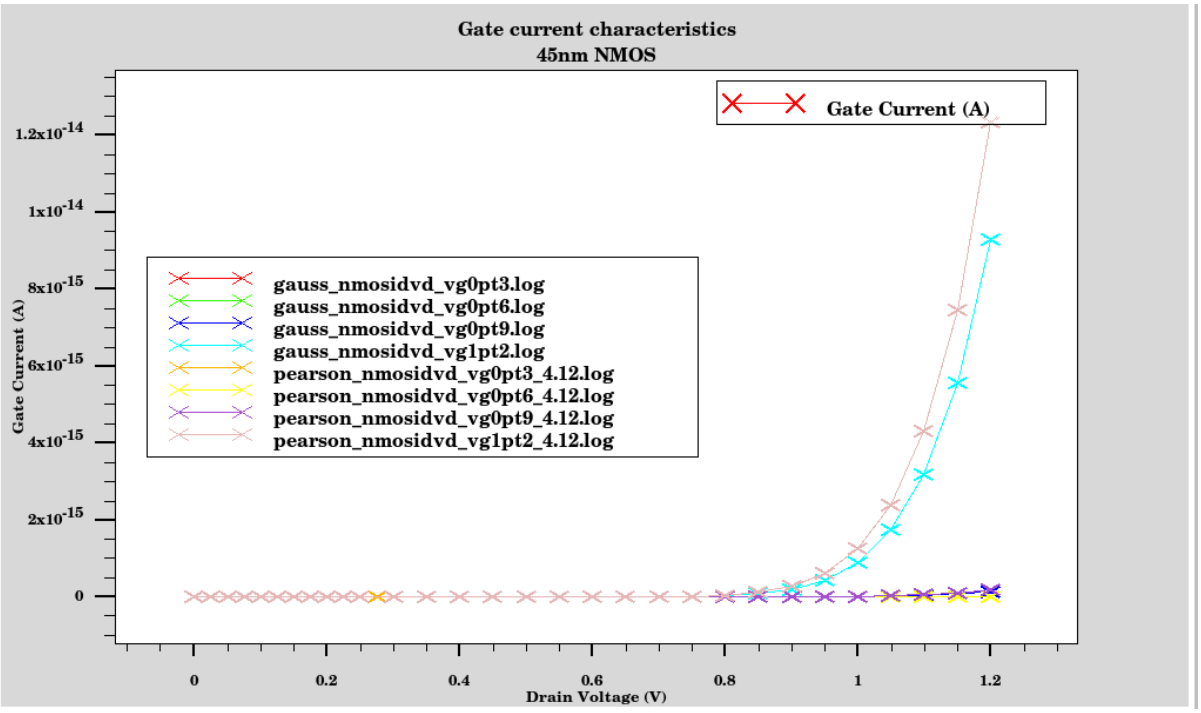


Figure 4.49 I_G - V_{DS} of NMOS with Gaussian & Pearson Doping Profile

The substrate current characteristics are as shown in Figure 4.50 and Figure 4.51. The estimated substrate current for the Gaussian Doping Profile is 9.46504x 10^{-7} and for Pearson Doping Profile is 1.02065x 10^{-6} which is more in this profile.

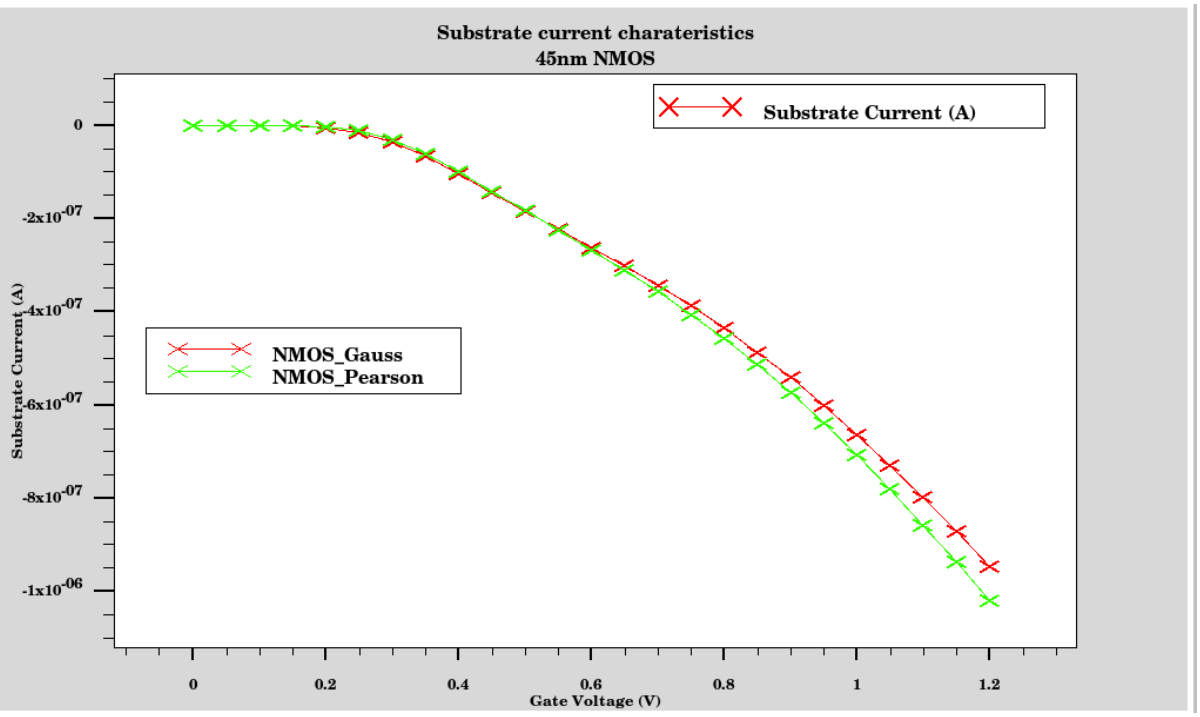


Figure 4.50 I_{SUB} -V_{GS} of NMOS with Gaussian & Pearson Doping Profile

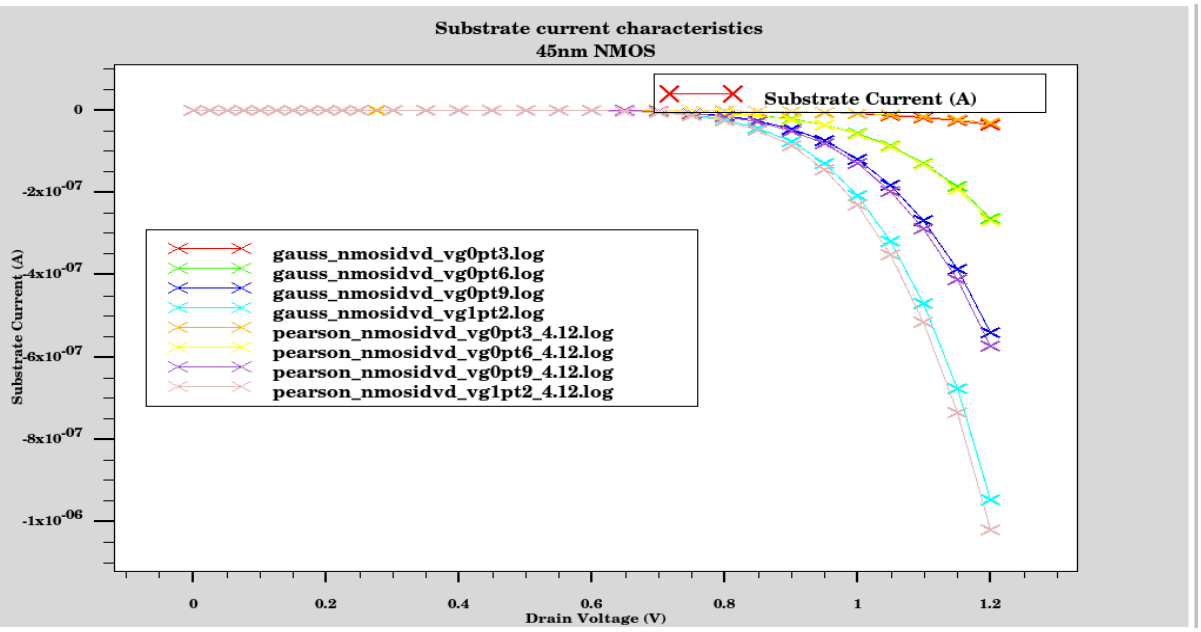


Figure 4.51 I_{SUB} -V_{DS} of NMOS with Gaussian & Pearson Doping Profile

4.6.1 Effect of Gate Oxide Thickness on Gauss and Pearson Doping Profiles of NMOS

The thickness of the gate oxide plays a significant part in MOSFET scaling. The impact of gate leakage comes into the picture as the gate oxide thickness is reduced or scaled-

down. The effect of scaling down of t_{ox} from 2nm to 1nm, with Gaussian and Pearson Doping Profiles are shown after the simulation of NMOS device. The drain current characteristics are as shown in Figure 4.52 and 4.53.

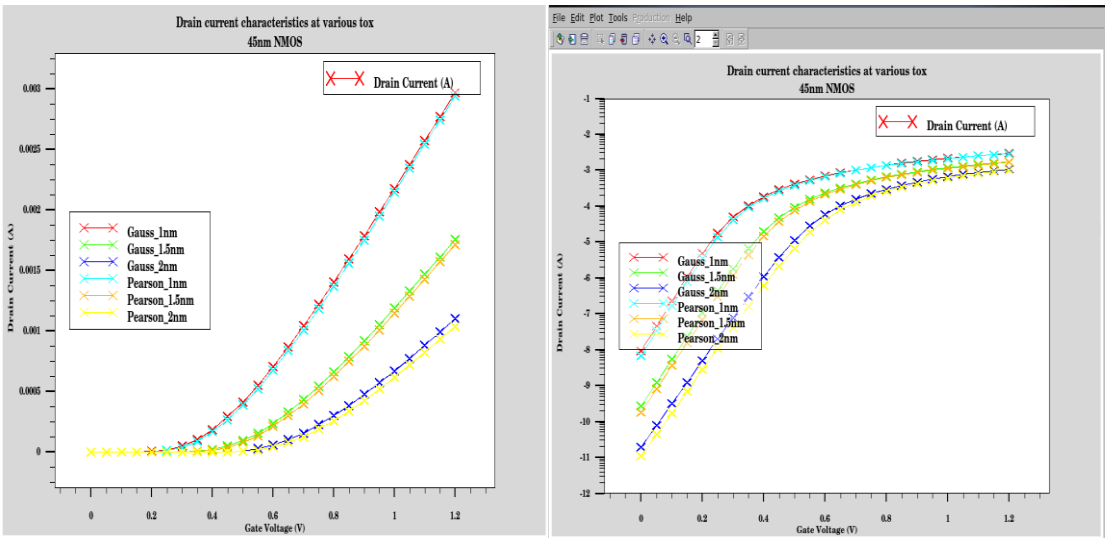


Figure 4.52 Gauss and Pearson dopings at various t_{ox} in linear mode and Log mode

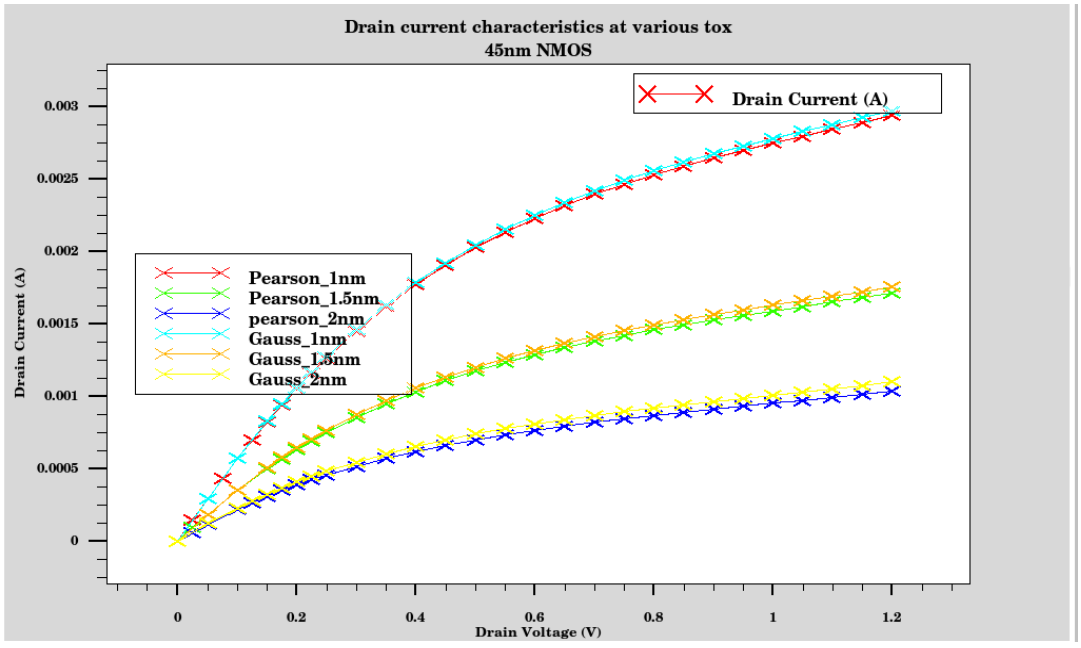


Figure 4.53 Gauss and Pearson doping comparison at various t_{ox}

The comparative Figures below show more precise results after the extraction of parameters after the simulation. Figure 4.54 shows the two threshold voltages, V_{tsat} at high drain voltage equals to 1.2V and V_{tlin} at low drain voltage equals to 0.05V. It shows both threshold voltages, V_{tsat} and V_{tlin} are more in Pearson Doping Profile.

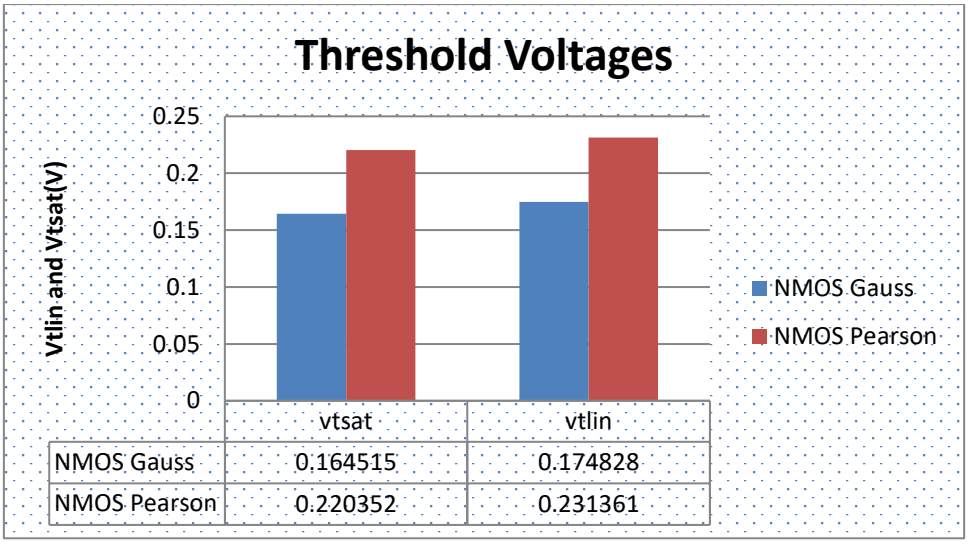


Figure 4.54 Vtsat and Vtlin for Gauss and Pearson doping Profiles

Figure 4.55 shows that OFF current with NMOS Gaussian Doping Profile equals to 9.42215nA is less as compared to Pearson Doping Profile equals to 6.92924nA.

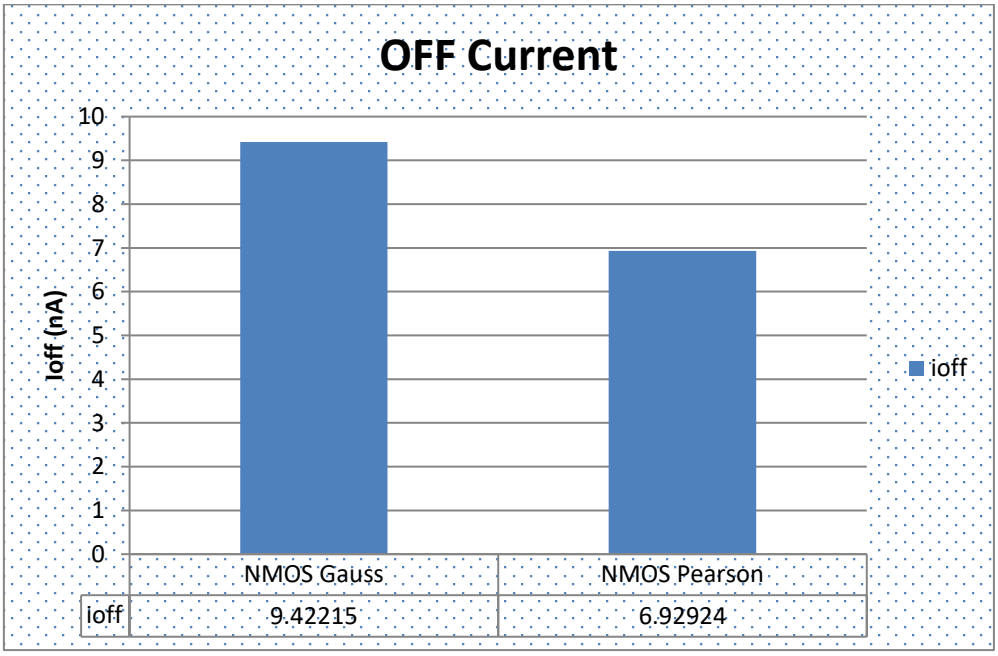


Figure 4.55 OFF current for Gauss and Pearson doping Profiles

Figure 4.56 shows the substrate current in Gaussian Doping Profiles equals to 9.74×10^{-7} A is less as compared to the Pearson Profile equals to 1.02×10^{-6}A

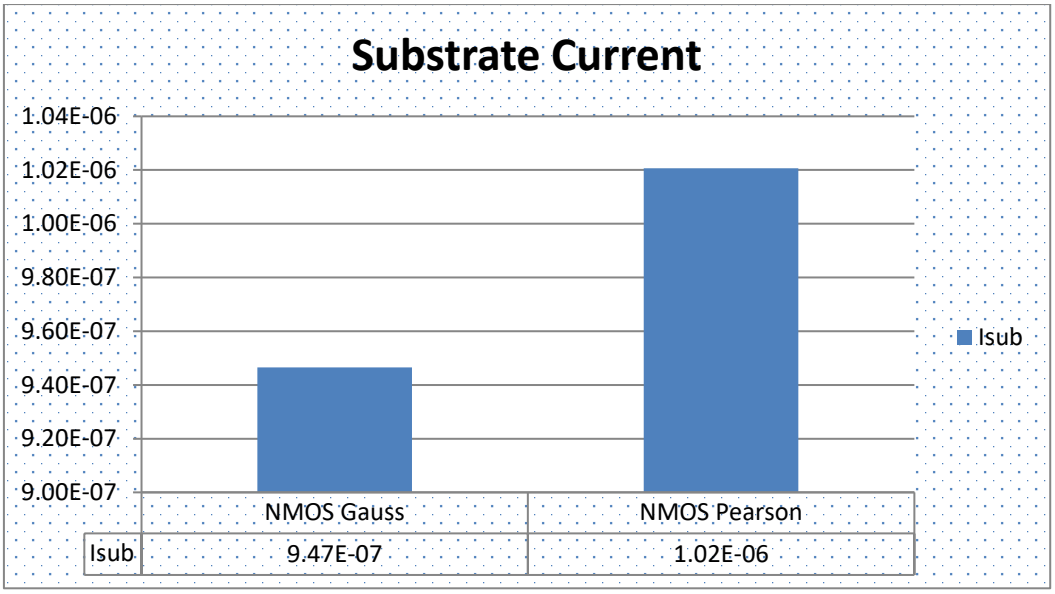


Figure 4.56 Substrate current for Gauss and Pearson doping Profiles

4.7 DESIGN CONSIDERATIONS OF P-CHANNEL DEVICE BY VARYING WORK-FUNCTION

Due to its excellent scalability, the bulk device has been the leading device structure for integrated circuit design over the last several years. Such type of devices is expected to continue to the 10 nm channel length. In order to effectively calculate the characteristics of future bulk Complementary Metal Oxide Semiconductor (CMOS), it is necessary to identify the scaling developments of main model parameters such as threshold voltage [3] and gate oxide thickness, their association in estimating the device characteristics should be well included for accurate model prediction. The parameters are slightly varied step by step and the threshold voltage effect is observed using SILVACO TCAD tool. There can be millions of transistors on a small piece of silicon in the future scope of ICs. Without computer aids, the manufacture and design of these ICs cannot be done. Both the manufacture and design of these ICs require Electronic Design Automation (EDA) tools. Highly accurate software tools are required to analyze, simulate the design and manufacture of integrated circuits. Much research has been done on these issues and is still going on. As a result, we have very useful tools for designing and manufacturing Integrated Circuits. This section maintains stress on 45 nm p-type MOSFET device design, virtual fabrication, and analysis using SILVACO TCAD tool. The analysis was based on a variation of different parameters such as oxide thickness, threshold implant and halo implant (pockets) for threshold

voltage analysis [112]. Tony-Plot is used to plot the drain versus gate and drain versus gate plots. It has been observed that the threshold voltage is also increasing as the thickness of the oxide increases. Various other parameters are also calculated for different oxide thicknesses such as ON current, off-state current, ON / OFF current ratio and DIBL. From the simulation results, the optimum threshold voltage of -0.026V has been achieved. A 45 nm PMOS bulk device has been designed having substrate doping $5x10^{15}$ cm^{-3} with orientation <100> and with gate oxide thickness 1nm. The design and fabrication of PMOS device are done with ATHENA at 45 nm technology.

In ATHENA, a PMOS device is designed and simulated in ATLAS [113][114]. After design and simulation, the fabricated structure is acquired which displays the different layers of conductor, insulator and semiconductor and also demonstrates absolute net doping in the structure. The analysis of the device with any TCAD tool gives an easy way to study the effects of the process parameter on device efficiency and can optimize both the device structure and the fabrication process. The simulated structure of PMOS is as shown in Figure 4.57.

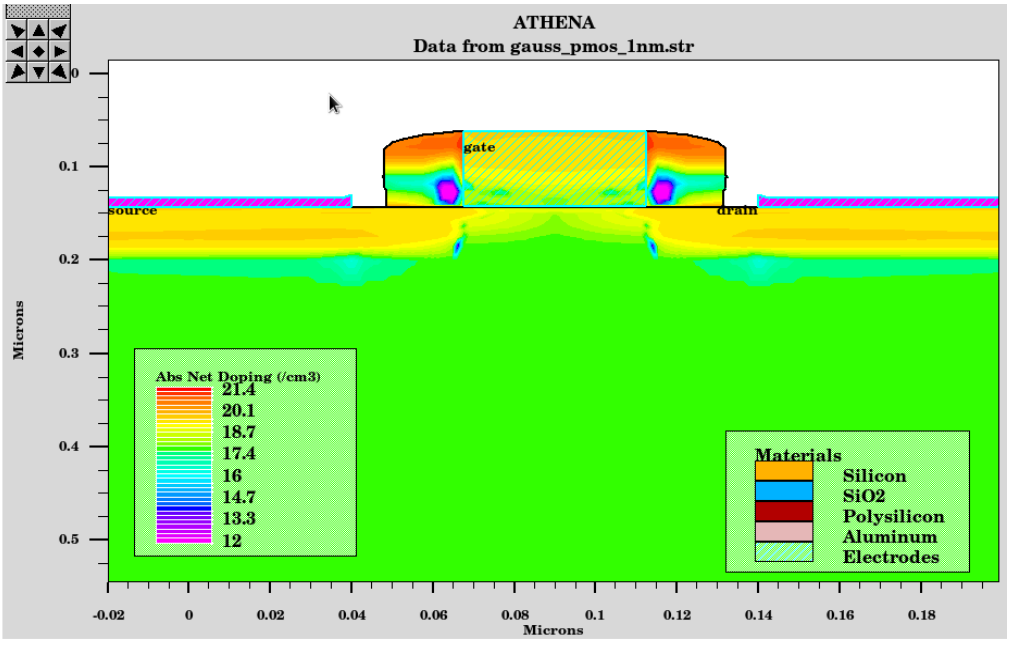


Figure 4.57 Structure of 45nm PMOS in ATHENA

After designing the structure, it is simulated to acquire the features of drain current versus gate voltage that can be seen and evaluated in the graph as shown in Figure 4.58.

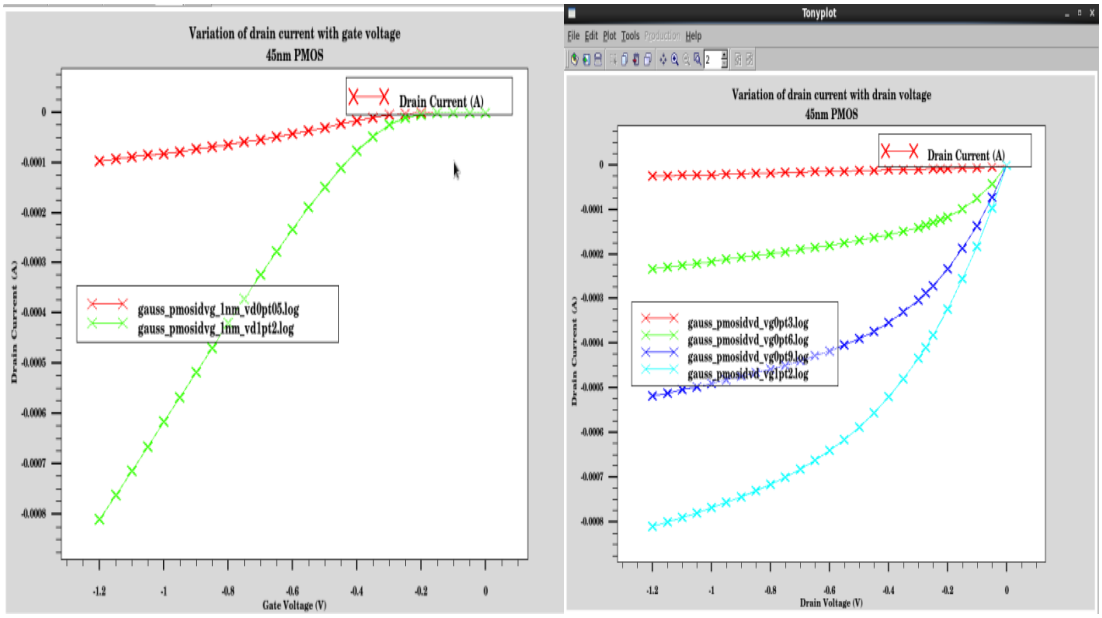


Figure 4.58 I_D-V_{GS} curve and I_D-V_{DS} curve at different drain voltages

Figure 4.58 shows I_D-V_{GS} curve at different drain voltages. It validates the variation of drain current in relation to gate voltages at distinct drain voltages. As the gate voltage rises, the drain current rises linearly and it saturates after reaching a peak value. The features of the I_D-V_{GS} were noted at various drain voltages at V_{DS}=0.05V and V_{DS}= 1.2V to obtain a clear knowledge of the drain current versus the characteristics of the gate voltage. As the drain voltage increases, there is also an increase in the drain current for different gate voltages. After drain voltage has risen to a certain value, the peak value is achieved by both drain voltage and drains current and does not rise beyond that.

Different PMOS parameters are noted after simulation, including gate oxide density, ON current, OFF present, DIBL and threshold voltage. These parameters play a major role in determining the PMOS device behavior [115]. By varying the gate oxide thickness, the threshold voltage may be increased or decreased. Various parameters such as oxide thickness, implant doping concentration threshold adjustment and halo-implant doping concentration are observed at parameters such as DIBL, ON current, OFF current and threshold voltage using the simulation tool on a lightly doped PMOS device.

4.8 DESIGN CONSIDERATIONS OF P-CHANNEL DEVICE BY VARYING THE GATE OXIDE THICKNESS

An increase in threshold voltage is observed with the rise in gate oxide thickness. The thickness of the gate material is originally 0.001 μm and increased to 0.002 μm. With this mild rise in the density of the gate oxide, the limit voltage is seen to improve by a better value. The threshold voltage differs from 0.264V to 0.553V as the gate oxide thickness varies from 1 nm to 2 nm [116]. Figure 4.59 demonstrates the graph between the limit voltages and the thickness of the gate oxide. As the gate oxide thickness increases, the threshold voltage increases as well.

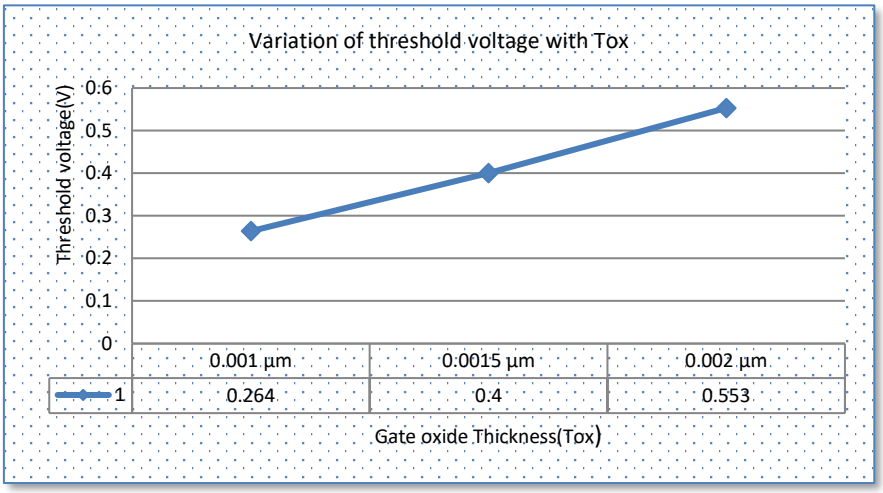


Figure 4.59 Threshold Voltages at Different Gate Oxide Thicknesses.

4.9 DESIGN CONSIDERATIONS OF P-CHANNEL DEVICE BY VARYING THE THRESHOLD VOLTAGE IMPLANT

As the concentration of the threshold adjust implant ranges from $1.5x10^{12}cm^{-3}$ to $3x10^{12}cm^{-3}$, the threshold voltage value varies from 0.246V to 0.309V. It can be observed that with an increase in Vt implant, threshold voltage also keeps on increasing without showing any irregularity or a dip in the graph.

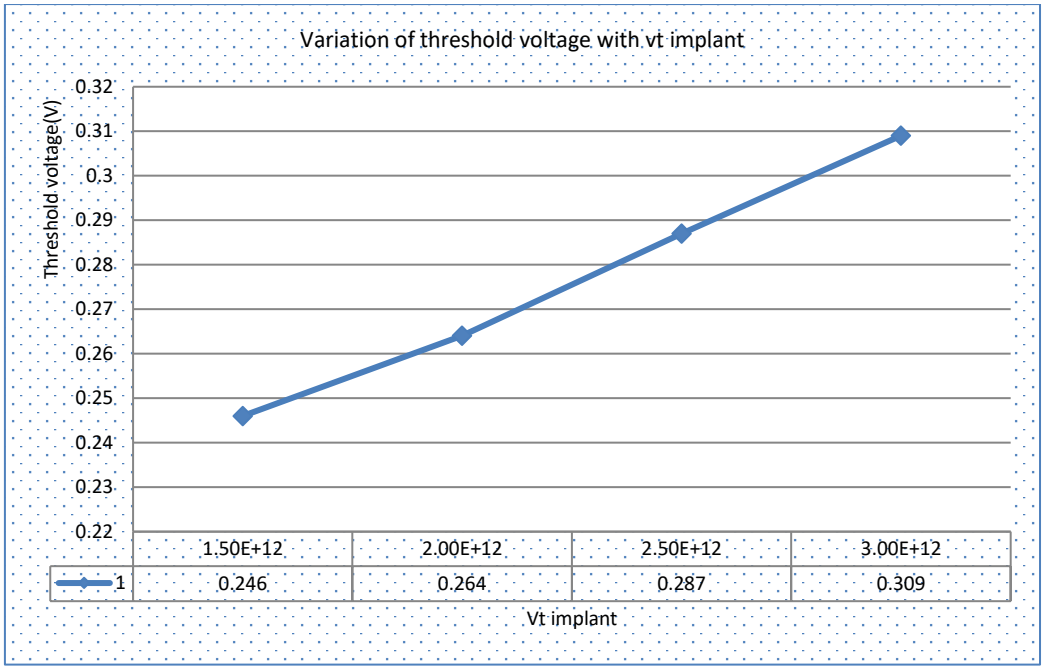


Figure 4.60 Variation of Threshold Voltage at different V_{th} Adjust Implantation

The relation between the threshold voltage and the V_{th} implant is as shown in Figure 4.60. V_{th} implant values are positioned on the horizontal axis, the threshold voltage is put on the vertical axis and a graph is plotted between the two to give a graphical understanding of the rising nature of threshold voltage with a rise in V_{th} implant. As we are increasing V_{th} implant voltage then the threshold voltage is increasing linearly. The ON and OFF currents are observed by varying the V_{th} implant. It can be concluded that with an increase in V_{th} implant, ON current and OFF current both show a decrease in their values. The value of ON current and OFF current varies from 8484µA. 18.88nA to 7401µA, 2.452nA respectively as the threshold implant concentration varies from $1.5x10^{12}$ cm^{-3} to $3x10^{12}$ cm^{-3}.

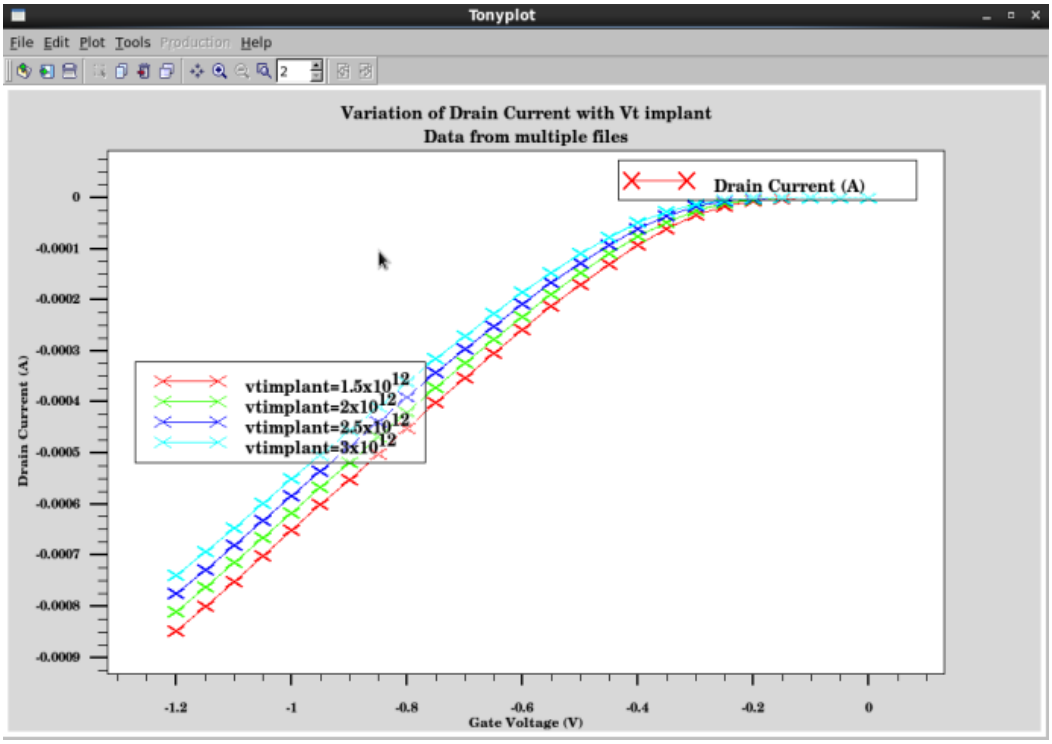


Figure 4.61 Variation of Drain Current with Vt Implant Data from multiple files

Figure 4.61 demonstrates the distinctive graph of drain current versus gate voltage where the gate current is positioned on the vertical axis and the gate voltage on the horizontal axis is positioned. The graphical representation of all the curves from multiple files shows an increasing nature with a higher slope for lower values. After a certain increase in the voltage of the gate, these curves are seen to reach a saturation point and thus the slope of the curve decreases slowly until saturation [60]. Figure 4.62 shown below plots a graph between substrate current vs gate voltage via data from multiple files. The different curves represent the behavior for different values of V_{th} implant concentrations. The graph that attains the maximum substrate current is for the minimum V_{th} implant concentrations, while one that achieves minimum substrate current among the considered cases belong to the maximum V_{th} implant concentration.

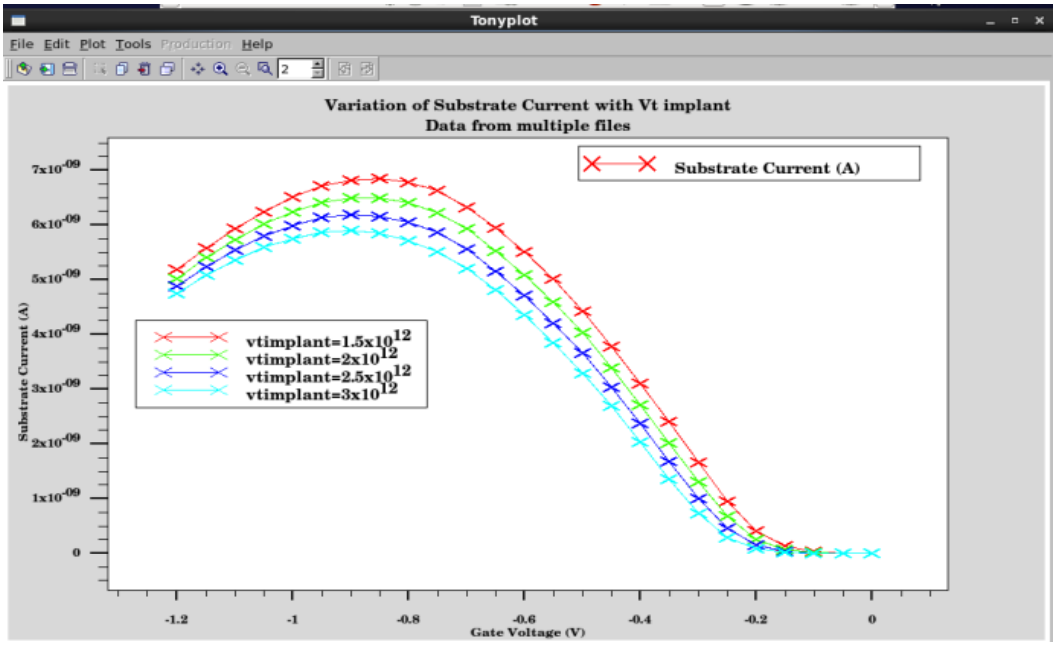


Figure 4.62: Variation of substrate Current with V_{th} implant Data from multiple files

From the graph it can be observed that with an increase in gate voltage the substrate current initially increases with an increasing slope. The slope of the curve begins to decrease and reaches the maximum. After attaining the maximum possible value for Substrate concentration, the curve now begins to decline with an increase in gate voltage i.e. after attaining the maxima a negative slope is observed. After increasing Gate voltage to a certain limit all the curves of different V_{th} concentrations attain saturation, substrate concentration reaches a minimum value before the gate voltage reaches the lower level.

4.10 DESIGN CONSIDERATIONS OF P-CHANNEL DEVICE BY VARYING THE HALO IMPLANT

The variations in halo implant from $3x10^{13}$ cm^{-3} to $6x10^{13}$ cm^{-3} results in variation in threshold voltage from 0.214V to 0.370V respectively. Figure 4.63 shows relationship between threshold voltage and the halo implant. Halo implant concentrations are placed on the horizontal axis while the threshold voltages are placed on the vertical axis. As the concentration of the halo implant is increasing the threshold voltage is increased.

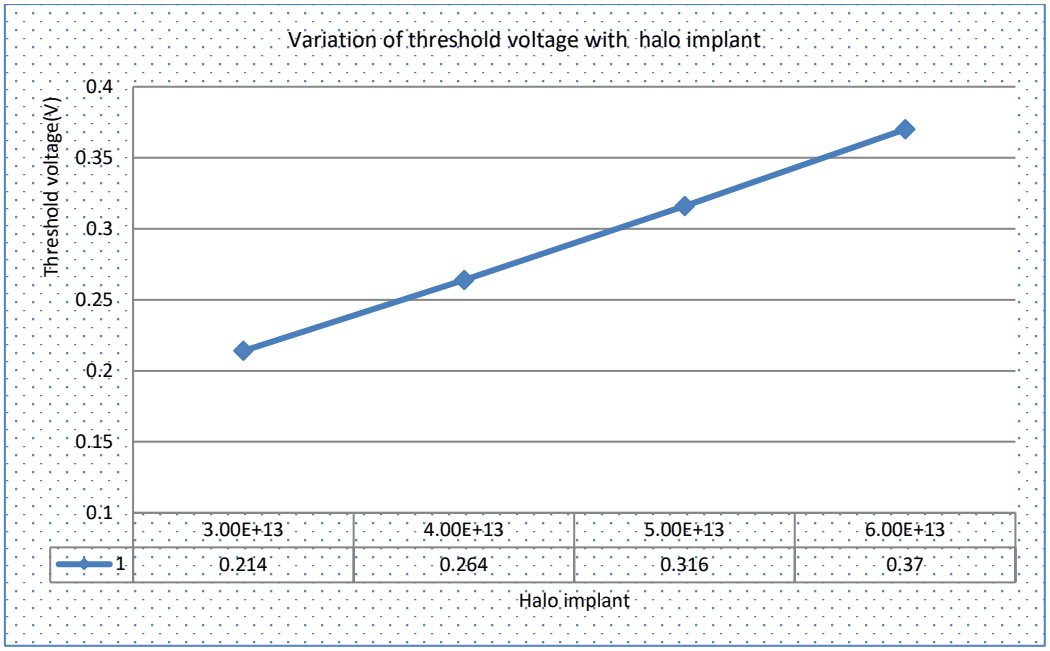


Figure 4.63: Variation of Threshold Voltage at Different Halo Implant Concentrations

The SILVACO software is used to vary the halo implant concentrations and then observe its effects on ON current and OFF current. With the increase in halo implant concentration ON current and OFF current both are seen to be decreasing. ON current is measured in a scale of micrometers while the OFF current is measured in a scale of nanometres. The variation in halo implant from $3x10^{13}$ cm^{-3} to $6x10^{13}$ cm^{-3} results in variation in ON current and OFF current from 9103µA, 56.22nA to 6340µA, 0.258nA respectively. Figure 4.64 below is a plot on the horizontal axis between the drain current along the vertical axis and the gate voltage. Different plots represent various concentrations of halo implants as shown in Figure 4.64 and Figure 4.65. Regardless of the concentrations of halo-implants, after a certain value of Gate voltage, the curves are seen to reach a saturation level beyond which there is no further increase in drain current.

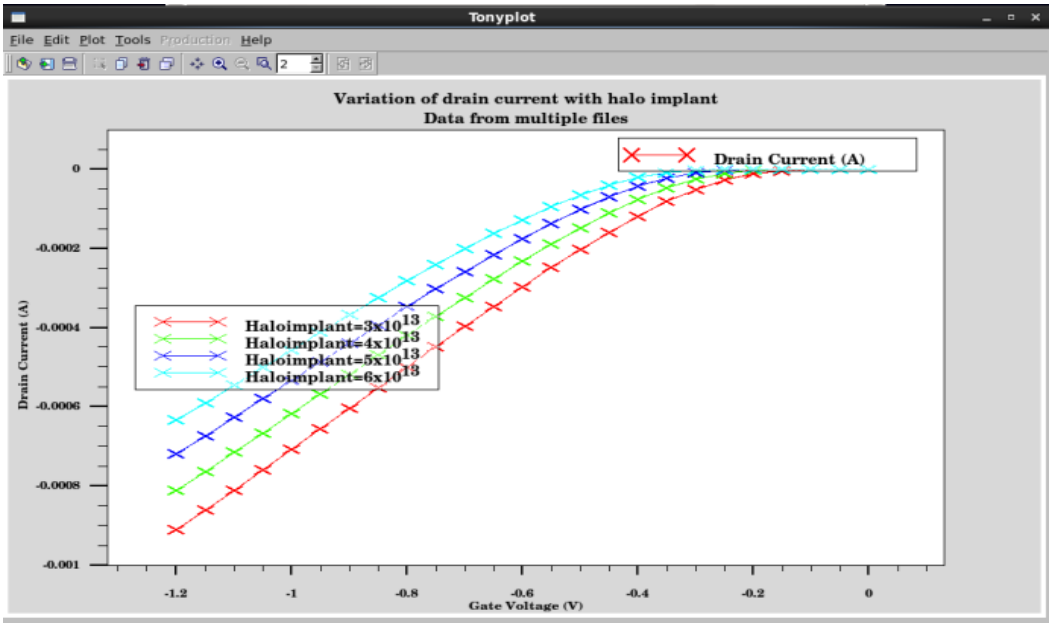


Figure 4.64 Variation of Drain Current with Halo Implant Data from Multiple Files

It has been observed that the value of the drain current is lower for the higher value of the halo implant concentration and a specific gate voltage below the saturation point. The plot below in Figure 4.65 shows that the higher the halo implant concentration for a particular gate voltage before the saturation point, the higher the substrate current. Initially, the curve has a positive slope that continues to decrease until the maximum is reached after reaching the maximum value of the substrate current, the curve reaches negative slope and decreases until it reaches lower substrate current [117].

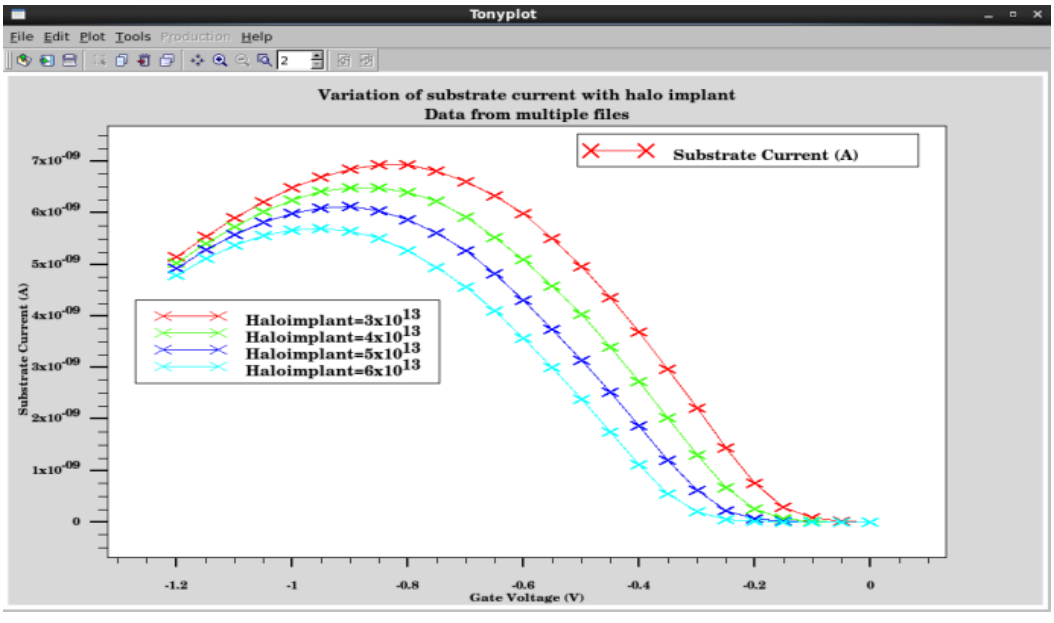


Figure 4.65 Variation of Substrate Current with a Halo Implant

4.10.1 Impact of Threshold Implant, Halo Implant and Gate Oxide Thickness on DIBL

Unintentional electrostatic interactions between the source and the drain called Drain Induced Barrier Lowering (DIBL) may occur when the channel length of the MOSFETs are not properly scaled and the source/drain junctions are extremely deep or due to low channel doping [45]. This also results in a punch-through effect or breakdown between source and drain which further results in gate control loss. The result is a different I_D-V_G curve after applying the different values of drain voltage to the source. The simulation will use the existing Athena simulation structure file.

Table 4.2 Effect of tox, Vt adjust and Halo implant on DIBL

Tox	Vt implant	Halo implant	DIBL
1nm	2e12	4e13	0.07574
1.5nm	2e12	4e13	0.111704
2nm	2e12	4e13	0.141089
1nm	1.5e12	4e13	0.077307
1nm	2e12	4e13	0.07574
1nm	2.5e12	4e13	0.072918
1nm	3e12	4e13	0.071846
1nm	2e12	3e13	0.079274
1nm	2e12	4e13	0.07574
1nm	2e12	5e13	0.07272
1nm	2e12	6e13	0.06943

The values of t_{ox}, V_{th} implant concentration and halo implant concentration are varied and the effects are observed on DIBL in Table 4.1. As t_{ox} is increased the value of DIBL is also increased, along with that, with a decrease in Halo implant concentration a decrease in DIBL is observed. Thus we can say that t_{ox} and Halo implant concentration is directly proportional, while it is observed that an increase in $V_{th,}$ DIBL is decreased [18]. Hence, inverse proportionality is observed between V_{th} implant and DIBL. The CMOS inverter can be designed using the above designed NMOS and PMOS devices using the mixed mode of SILVACO [118-122].

4.13 CONCLUSION

Different parameters are varied in this research work to control the different MOSFET factors. This chapter concludes that the analysis of variation of different parameters with work-function shows that the off-state leakage current of the device for lightly doped substrates decreases as a desirable factor for low-power applications. In addition, the DIBL and sub-threshold slope are also improving, but the device's drain current is dropping. In between the drain current and the subthreshold current, there is a trade-off. The lightly doped and heavily doped MOS devices are virtually fabricated and their characteristics are analyzed for drain current, substrate current, threshold voltage and off current. The lightly doped substrate provides better ON current equal to 2973μA, better threshold voltage equal to 0.22V, better off current equal to 2.580nA, better substrate current equal to 8.277e-07A, better sub-threshold slope equal to 72mV/dec even at low t_{ox} compared to the heavily doped substrate. This chapter also concludes that the halo implant is varied during fabrication in order to obtain optimized OFF-state leakage current of 9.422nA, 0.22V threshold voltage, 72.45mV/decade substrate current and 48mV/V DIBL at 1 nm gate oxide thickness. Halo implant's best value is $5x10^{13}cm^{-3}$.This also improves the ON / OFF ratio, which means that the device has a higher current drive and lower off-state leakage current. For best performance device, the best value of Polysilicon doping and concentration of Source / Drain doping appears to be $1.5x10^{13}cm^{-3}$ and $3.5x10^{15}cm^{-3}$respectively.It also concludes the design, virtual fabrication, simulation and analysis of a 40 nm gate length 45 nm NMOS device. The comparison of doping profiles in both Gaussian and Pearson is based on simulation results. Pearson Doping Profile has less OFF-state leakage current equal to 6.92924nA and high threshold voltage, Gaussian Doping profile has less substrate current equal to $9.47x10^{7}$ A and lower threshold voltage. The drain current is more equal to 2973μA in Gaussian Doping Profile. NMOS device is simulated with different thicknesses of the gate oxide. In the last, PMOS device was designed using the Gaussian Doping Profile and Halo Implant Variation, gate oxide thickness and threshold implant that affects the device threshold voltage, drain current, leakage current and substrate current. The estimated threshold voltage is -0.264V and a leakage current of 9.349nA are achieved for the 45 nm PMOS device in line with the guideline for the International Semiconductor Technology Roadmap (ITRS).

CHAPTER 5

PERFORMANCE ANALYSIS OF SOI-MOSFET

Over the last 25 years, silicon technology has emerged as the dominant technology in the microelectronics field because of the need for high integration density and high-performance digital circuits [123]. The continuous scaling of MOSFET dimensions deteriorates the performance of the device and enables different innovations such as Silicon-on-Insulator (SOI) to be developed by emerging technology. Two types of SOIs are available: PDSOI (Partially depleted SOI) and FDSOI (Fully depleted SOI). Due to its stronger subthreshold slope along with small parasitic capacitance, FDSOI MOSFET is preferable [124]. SOI MOSFETs have reduced leakage current, high speed due to very low capacitance and lower power dissipation as compared to traditional MOSFETs. The thickness of buried oxide can be varied to get a high-performance device. SILVACO TCAD tool is used to evaluate the dual material SOI MOSFET behavior. To decrease the leakage current of the device which is the necessary parameter in MOSFETs presently, the channel is doped with halo implants. The threshold voltage of the device can be adjusted by increasing or decreasing the doping concentration of the channel [85]. The leakage current of the MOSFET is a crucial metric for determining the capability of the device.

5.1 Dual Material SOI MOSFET

Due to the increased electric field on the drain side of the MOSFETs, various short channel effects occur which further reduce the device performance of the device. By proposing the improvement in the structure of the Gate, Gate material engineering is used to resolve these short channel effects and to reduce the strong electric field on the drain side. To improve the electric field at the source region, the Dual Material gate is proposed here to increase the efficiency of channel carriers [125] [82]. In the DMG MOSFET, the metal work-function of Gate1 (M_1) is higher than that of Gate2 (M_2) and the threshold voltage corresponding to M_1(Vt_1) is also higher than that corresponding to M_2 (Vt_2). It has the implied benefit of increasing gate transport efficiency by changing the electric field profile across the channel [122]. Due to the distinct work functions of two gates, the surface potential profile which is a step function validates a

decrease in the short-channel effects and the screening of the channel region under the M_1 from the variations of the drain potential.

5.1.1 Dual Material Gate Structure

The structure of fully depleted Dual-Material SOI MOSFET with two metal gates M_1 and M_2 of lengths L_1 and L_2 respectively is shown in Figure 5.1

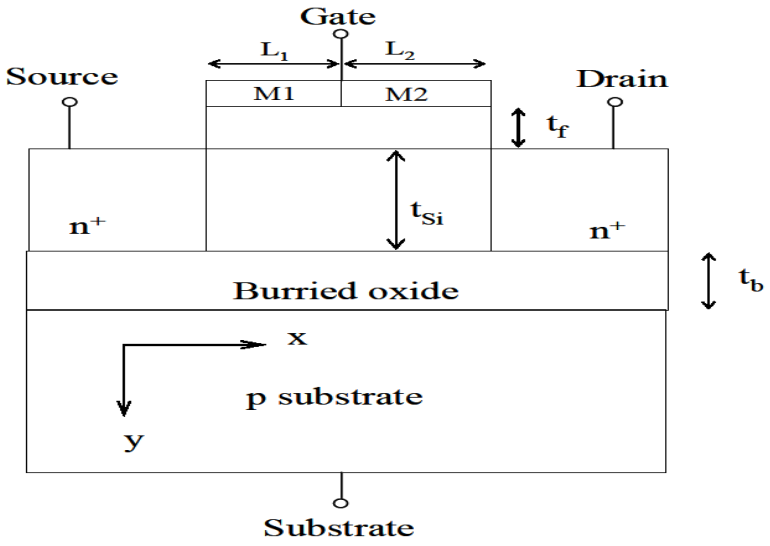


Figure 5.1 Structure of Dual material FD-SOI MOSFET

The source/drain regions of the device are doped uniformly at $9x10^{18}cm^{-3}$ and the channel is doped at $1x10^{15}cm^{-3}$. The buried oxide thickness, silicon channel thickness and front gate oxide thickness are 41nm, 9nm and 0.5nm respectively. The Source/Drain extension and channel length L_C (L_1+L_2) are considered 10nm and 15nm respectively. The work-function of M_1 and M_2 are considered 4.6 and 4.1 respectively. In this device, a high-dielectric constant (K=16) material is used i.e. Hafnium oxide (HfO_2) to enhance the electrostatic control of the gate over the channel and to increase the I_{ON}/I_{OFF} ratio [70] [126]. The device simulations are carried out using different models. For the electron generation/recombination consideration, SRH and auger models are used. To calibrate the theoretical values with the simulated values, these models are enabled in the simulator [127][119].

5.1.2 Mathematical Modeling

This section describes the mathematical model of the fully depleted Dual Material MOSFET. As the channel region is doped uniformly so that it is also possible to ignore the effects of fixed charge carriers to model the potential distribution:

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{Si}} \quad for\ 0 \le x \le L\ , 0 \le y \le t_{Si} \tag{5.1}$$

where t_{si} is the thickness of the silicon film, L is the length of the channel, N_A is the concentration of silicon film doping and silicon permittivity is ε_{si}. For the Fully Depleted DM SOI MOSFET, parabola function can be expressed as

$$\phi(x,y) = \phi_s(x) + c_1(x)y + c_2(x)y^2 \tag{5.2}$$

where the surface potential is φ(x) and c_1(x) and c_2(x) are the constants that are a function of x only to measure the vertical direction potential i.e. y-direction. The gate is divided into two sections in the Dual Material Gate structure i.e. Metal1 (M_1) and Metal2 (M_2) and the potential under M_1 and M_2 can be written as

$$\phi_1(x,y) = \phi_{s1}(x) + c_{11}(x)y + c_{12}(x)y^2 \quad for\ 0 \le x \le L_1\ , 0 \le y \le t_{Si} \tag{5.3}$$

$$\phi_2(x,y) = \phi_{s2}(x) + c_{21}(x)y + c_{22}(x)y^2 \quad for\ \ L_1 \le x \le L_1 + L_2\ , 0 \le y \le t_{Si} \tag{5.4}$$

For both Gate regions with boundary conditions, the potential profile is separately determined:

I. At the interface of the two distinct metals, the continuous surface potential is

$$\phi_1(L_1, 0) = \phi_2(L_1, 0) \tag{5.5}$$

II. At the interface of the two distinct metals, continuous electric flux is

$$\left.\frac{d\,\phi_1(x,y)}{dx}\right|_{x=L_1} = \left.\frac{d\,\phi_2(x,y)}{dx}\right|_{x=L_1} \tag{5.6}$$

III. The electric flux at the gate/front-oxide interface is constant for both Metal Gates.

$$\left.\frac{d\,\phi_1(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\,\frac{\phi_{S1}(x) - V'_{GS1}}{t_{ox}} \quad \text{for Metal1} \tag{5.7}$$

$$\left.\frac{d\,\phi_2(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\,\frac{\phi_{S2}(x) - V'_{GS2}}{t_{ox}} \quad \text{for Metal2} \tag{5.8}$$

Where t_{ox} is the gate oxide thickness, $V_{FB1,f}$ and $V_{FB2,f}$ are the flat band voltages of the front gate of M_1 and M_2 respectively.

$$V'_{GS1} = V_{GS} - V_{FB1,f} \text{ and } \qquad V'_{GS2} = V_{GS} - V_{FB2,f}$$

IV. The potential at the source end is given by:

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi} \tag{5.9}$$

V. The potential at the drain end is given by:

$$\phi_2(L_1 + L_2, 0) = \phi_{s2}(L_1 + L_2) = V_{bi} + V_{DS} \tag{5.10}$$

Where $V_{bi} = {}^{E_g}/_{2} + V_T ln\, {}^{N_A}/_{n_i}$ is the built-in potential, n_i is the intrinsic concentration, N_A is the doping concentration.

VI. Electric flux is constant for both the metal gates at the interface of buried oxide and the back-channel.

$$\left.\frac{d\,\phi_1(x,y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{SUB} - \phi_B(x)}{t_b} \quad \text{for Metal1} \tag{5.11}$$

$$\left.\frac{d\,\phi_2(x,y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{SUB} - \phi_B(x)}{t_b} \quad \text{for Metal2} \tag{5.12}$$

Region under Metal1

The further relations of potential can be obtained from equations 5.3, 5.7 and 5.11 for the region under Metal 1:

$$\phi_{S1}(x) + c_{11}(x)t_{Si} + c_{12}(x)t_{Si}^2 = \phi_B(x) \tag{5.13}$$

$$c_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi_{S1}(x) - V'_{GS1}}{t_f} = C_f \left(\frac{\phi_{S1}(x) - V'_{GS1}}{\varepsilon_{Si}}\right) \text{where} C_f = \frac{\varepsilon_{ox}}{t_f} \tag{5.14}$$

$$c_{11}(x) + 2c_{12}(x)t_{Si} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{SUB} - \phi_B(x)}{t_b} = C_b \left(\frac{V'_{SUB} - \phi_B(x)}{t_b}\right) \text{where} C_b = \frac{\varepsilon_{ox}}{t_b} \tag{5.15}$$

By solving the equations 5.12, 5.13 and 5.14, we get

$$c_{12}(x) = \frac{V'_{SUB} + V'_{GS1}\left(\frac{C_f}{C_b} + \frac{C_f}{C_{Si}}\right) - \phi_{S1}(x)\left(1 + \frac{C_f}{C_b} + \frac{C_f}{C_{Si}}\right)}{\left(1 + 2\frac{C_{Si}}{C_b}\right)} \tag{5.16}$$

Where $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$

By substituting the values of c_{11}(x) from equation 5.14 and c_{12}(x) from equation 5.16 to 5.3 equation, the potential distribution is given as:

$$\frac{d^2\phi_{Si}(x)}{dx^2} - \alpha\phi_{S1}(x) = \beta_1 \tag{5.17}$$

Where $\alpha = \frac{2(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}})}{t_{Si}^2(1+\frac{2C_{Si}}{C_b})}$

$$\beta_1 = \frac{qN_A}{\varepsilon_{Si}} - 2V'_{GS1}\left(\frac{\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}\right) - 2V'_{SUB}\left(\frac{1}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}\right)$$

By solving the second-order non-homogenous differential equation 5.17, Potential distribution can be described as:

$$\phi_{S1}(x) = Aexp(\lambda_1 x) + Bexp(\lambda_2) - \frac{\beta_1}{\alpha} \quad (5.18)$$

$$A + B - \frac{\beta_1}{\alpha} = V_{bi} \quad (5.19)$$

Region under Metal2

Similarly, for the region under Metal2 relations obtained from equations 5.4, 5.8 and 5.12:

$$\phi_{S2}(x) + c_{21}(x)t_{Si} \; + c_{22}(x)t_{Si}^2 = \; \phi_B(x) \quad (5.20)$$

$$c_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi_{S2}(x)-V'_{GS2}}{t_f} \; = \; C_f\left(\frac{\phi_{S2}(x)-V'_{GS2}}{\varepsilon_{Si}}\right) \text{where} C_f = \frac{\varepsilon_{ox}}{t_f} \quad (5.21)$$

$$c_{21}(x) + 2c_{22}(x)t_{Si} \; = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{SUB}-\phi_B(x)}{t_b} \; = \; C_b\left(\frac{V'_{SUB}-\phi_B(x)}{t_b}\right) \text{where} C_b = \frac{\varepsilon_{ox}}{t_b} \quad (5.22)$$

By solving the equations 5.16, 5.17 and 5.18, we get

$$c_{22}(x) = \frac{V'_{SUB}+V'_{GS2}\left(\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)-\phi_{S2}(x)\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_b}\right)} \quad (5.23)$$

By substituting the values of c_{21}(x) from equation 5.21 and c_{22}(x) from equation 5.23 to 5.4 equation, the potential distribution is given as:

$$\frac{d^2\phi_{S2}(x)}{dx^2} - \alpha\phi_{S2}(x) = \beta_2 \quad (5.24)$$

where

$$\beta_2 = \frac{qN_A}{\varepsilon_{Si}} - 2V'_{GS2}\left(\frac{\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}\right) - 2V'_{SUB}\left(\frac{1}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}\right)$$

By solving the second-order non-homogenous differential equation 4.24, Potential Distribution can be described as:

$$\phi_{S2}(x) = Cexp(\lambda_1(x - L_1)) + Dexp(\lambda_2(x - L_1)) - \frac{\beta_1}{\alpha} \quad (5.25)$$

5.1.3 Results and Discussion

The analytical model of the dual material SOI MOSFET is estimated in the above section. The simulations are also performed in the ATLAS simulator with the same boundary conditions to validate the proposed analytical model with the simulated results [37]. The device is initially developed and simulated in compliance with ITRS guidelines. The length of the channel ($L_G=L_1+L_2$) is 15 nm, the thickness of oxide (t_{ox}) is 0.5 nm and the thickness of silicon is 9 nm. Due to the decrease in gate oxide thickness, the gate leakage current flows through the thin layer of oxide along with other short channel effects [68]. Gate work-function engineering with two distinct work-functions is proposed to minimize the short channel effects. Also, the low k oxide layer is substituted with high k oxide layer to reduce the tunneling effect [128]. HfO_2, which is a material with high permittivity is taken for gate oxide material [129]. To minimize the sub-threshold leakage current of the device, a dual work-function technique is used i.e. Φ_1(Mo)=4.6eV at the source end and Φ_2(Mn)=4.1eV at the drain side along with high k material. By employing Molybdenum (Mo) for the M_1 gate and Manganese (Mn) for the M_2 gate as Gate material, the dual metal is formed [130] [73]. The electric field is higher at the source end as compared to the drain end due to the high work-function of the Metal M_1 at the source region. The simulated structure is shown in Figure 5.2 below following the simulations carried out in the simulator.

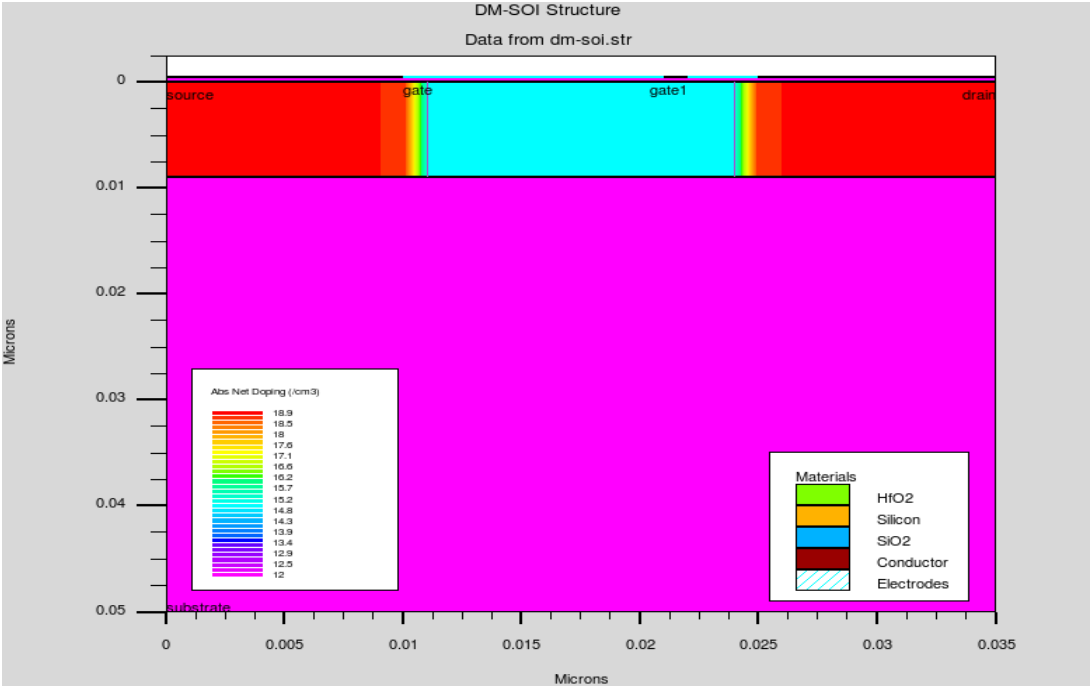


Figure 5.2 Simulated Structure of DM-SOI MOSFET

The surface potential of DM-SOI MOSFET has been analytically calculated and simulated at different drain voltages as shown in Figure 5.3.

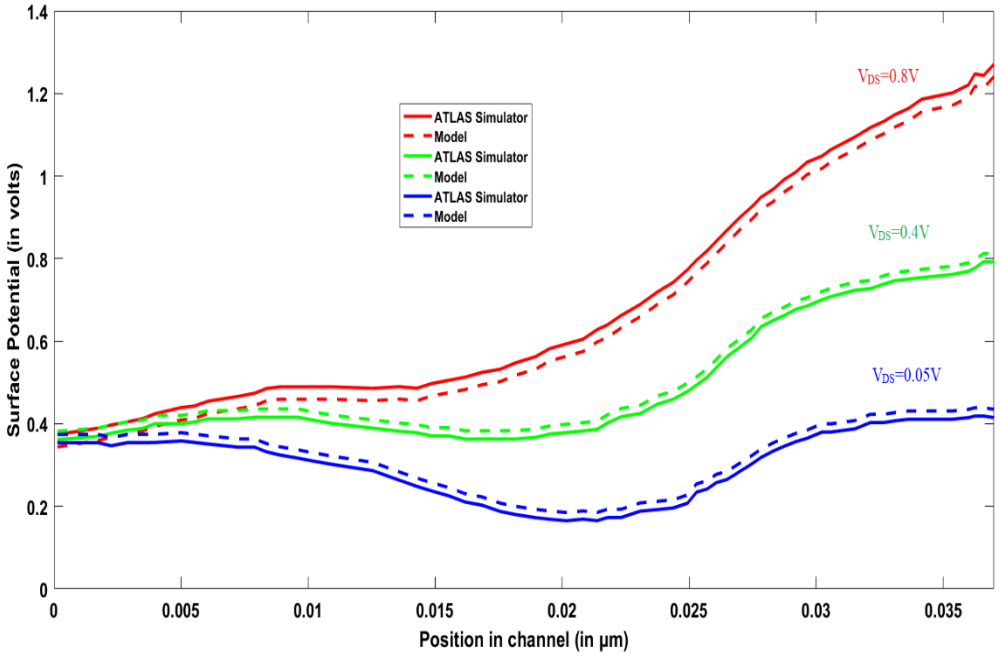


Figure 5.3 Potential distribution Graph of DM-SOI MOSFET

The estimated and simulated surface potential values at various drain bias voltages are plotted against the horizontal distance x for L=0.035 μm in Figure 5.3. The simulation results are validating the derived analytical model of the device. There is no substantial

improvement in the potential under gate M_1 due to the presence of a dual-material gate, even though the drain bias is increased. Therefore, the drain voltage has a much lower influence on the drain current and decreases drain conductance [91]. The drain current of the DM-SOI has been measured at different drain voltages as shown in Figure 5.4. It has been observed that the drain current increases as the drain voltage of the MOSFET increases. The sub-threshold current varies linearly with the gate to the source bias. However, an exponential rise is observed with an increase in the drain to source bias due to the barrier lowering induced by the drain. The increase in drain-source voltage boosts the minimum surface potential position which again exponentially increases the subthreshold current. So, for the shorter channel length devices, this exponential correlation becomes significant. For longer channel length devices, the leakage current is ignored but its influence cannot be ignored at smaller channel lengths. A higher leakage current results in higher energy consumption. It must also be taken into account at smaller lengths since it can result in low power consumption.

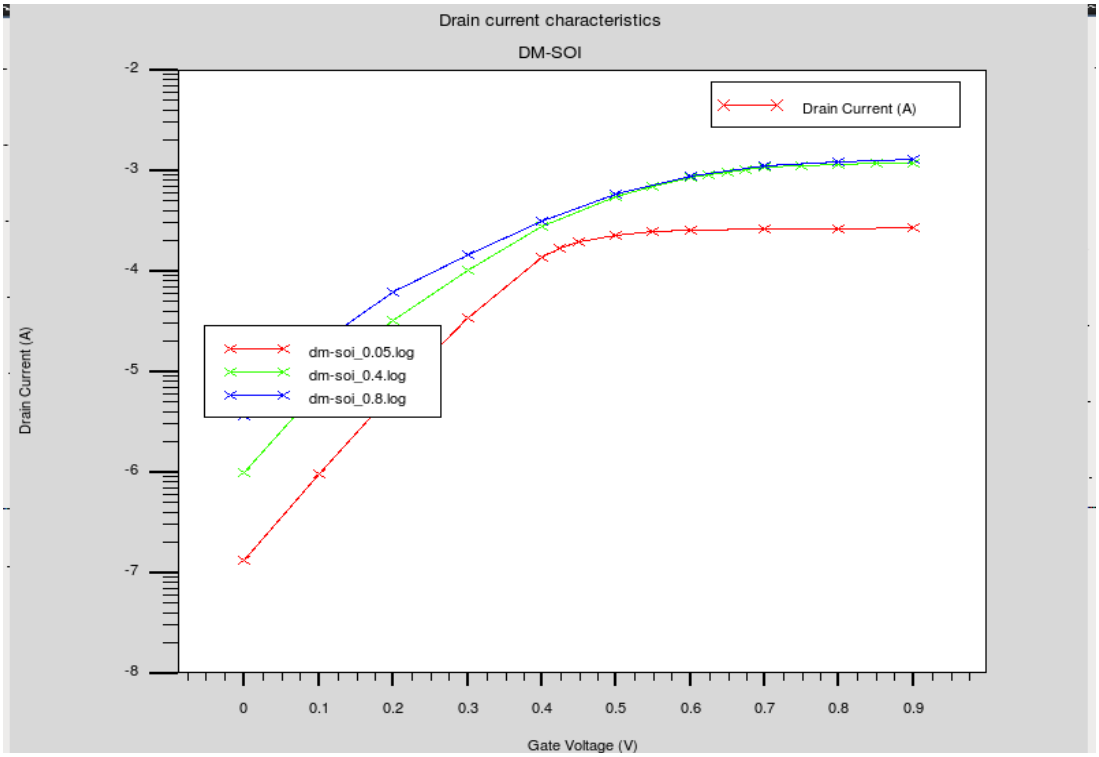


Figure 5.4 I_{DS}-V_{GS} characteristics at different V_{DS}

The MOSFET is simulated with distinct work functions, i.e. Φ_1= 4.6eV and Φ_2= 5.1eV as shown in Figure 5.5 respectively. It has been shown that as the work-function of the gate increases, the off-state leakage current decreases.

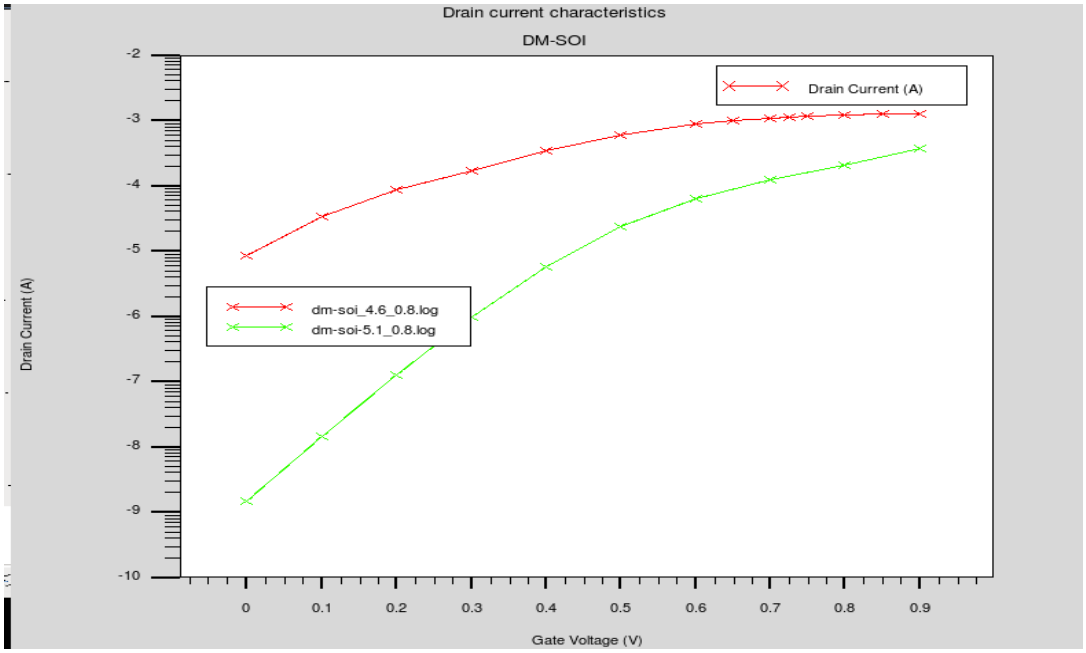


Figure 5.5 I_{DS}-V_{GS} characteristics at different work-functions

When the thin-film thickness is decreased, the front-gate controllability over the surface of the channel is increased as compared to the impact exerted by the source/drain. For distinct silicon film thicknesses i.e. t_{si}=9 nm and t_{si}=10 nm, the off-state leakage current is also calculated. For t_{si}=10nm, the leakage current is found to be lowered and increases with the rise in the thickness of silicon as shown in Figure 5.6 below.

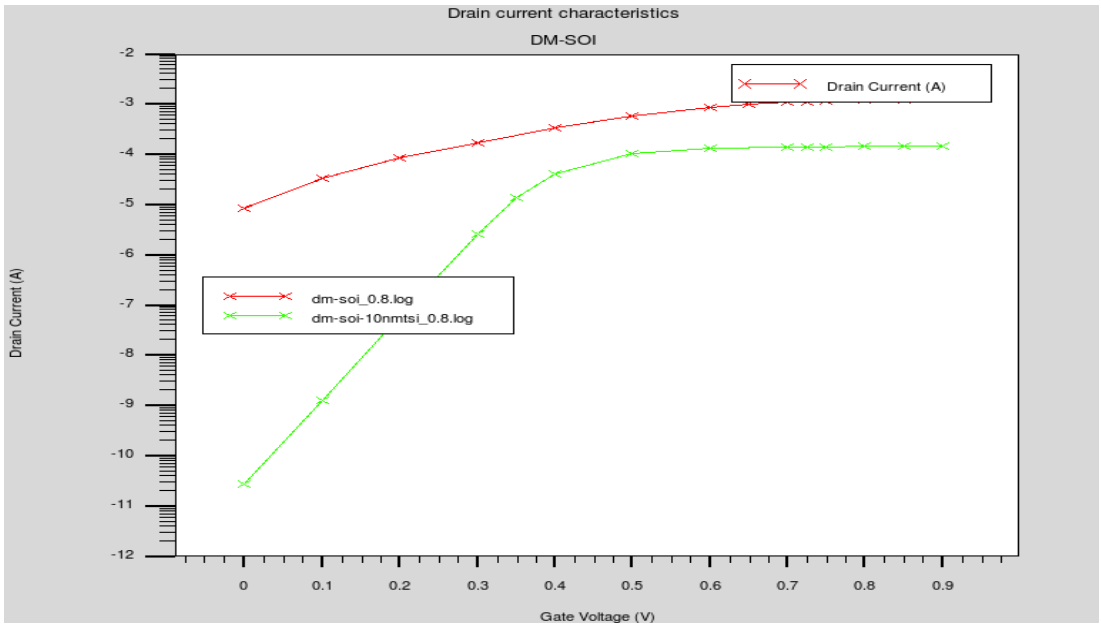


Figure 5.6 I_{DS}-V_{GS} characteristics at different silicon thickness

The performance characteristics of the Dual material Gate (DMG) and Single material Gate (SMG) SOI devices are compared for the channel length L=15nm. The work function of the gate material is selected as 4.1 eV for SMG SOI. The channel doping of

SMG SOI device is therefore taken as N_A=1x 10^{15} cm^{-3} which produces the same threshold voltage, V_{th} =0.21 V for both the DMG and SMG MOSFETs. The comparison of Single & Dual material gate devices is done on the basis of leakage current. It has been found that DM-SOI has less leakage current compared to SM-SOI MOSFET as shown in Figure 5.7.

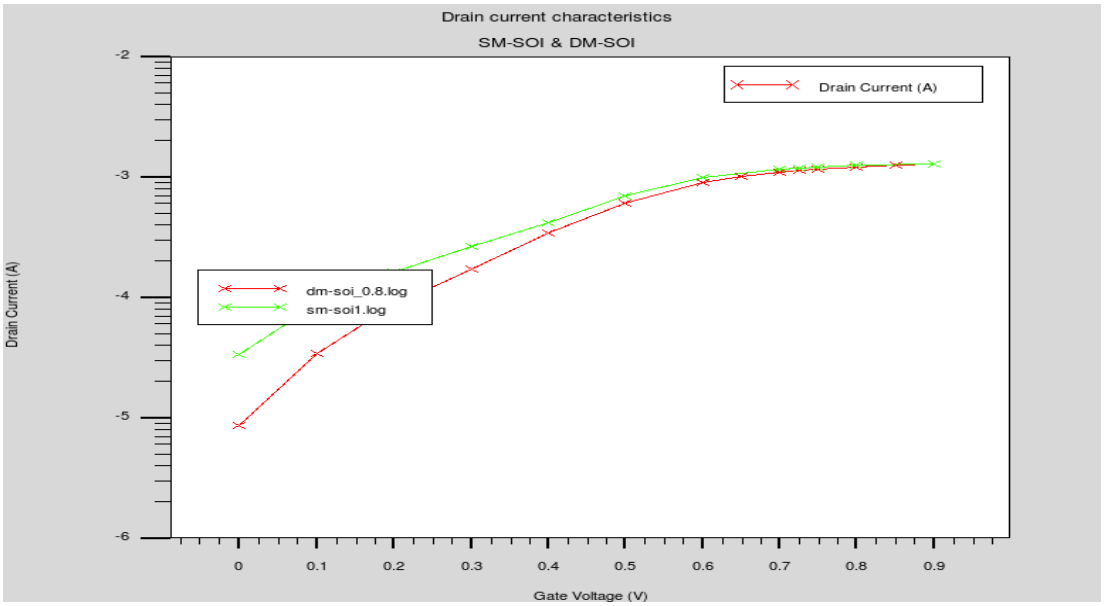


Figure 5.7 Comparison graph of SM-SOI & DM-SOI MOSFET

A two-dimensional analytical model of surface potential is generated for a fully depleted dual-material gate (DMG) SOI MOSFET by solving the 2-D Poisson equation with appropriate boundary conditions. The influence of various MOS parameters i.e silicon film thickness, work-function, applied drain voltages and effect of single & dual material gate on the leakage current has been studied. In comparison with 2-D TCAD simulations, the results estimated by the model are validated. Another degree of freedom for the design of the SOI transistor is the combination of Gate material engineering and Channel engineering, a good outcome discussed by this formulation. [125].

5.2 Dual Halo Dual material SOI MOSFET

The dual-material SOI structure developed in the above section does not offer good results in terms of leakage current. The idea of halo doping comes into the frame, either single or double to enhance the performance of the device. The doping is performed on one side of the channel in single halo dual material SOI MOSFET (SHDM-SOI) MOSFET [131] to improve the efficiency of the device. The halo doping is performed on both sides of the channel in the Dual Halo Dual Material SOI device so that the best

leakage current value can be obtained for low power applications. The Channel Engineering approach such as the Single-Halo (SH) also known as the lateral asymmetric channel or Dual-Halo (DH) implants are utilized to minimize the short channel effects. Channel Engineering and Gate Engineering approaches are combined to create a novel device structure, such as the Dual Halo Dual Material Gate (DHDMG) MOSFETs. [132]. Due to pocket implantation, the reverse short-channel effect (RSCE) is triggered by introducing impurity from both the source and drain regions. The overall concentration of pocket doping is progressively decreased linearly with a pocket length from both the source and drain regions towards the substrate concentration.

5.2.1 TCAD Simulation Results

Figure 5.8 shows the structure of the Dual Halo Dual material SOI MOSFET material with dual halo doping on both sides of the channel.

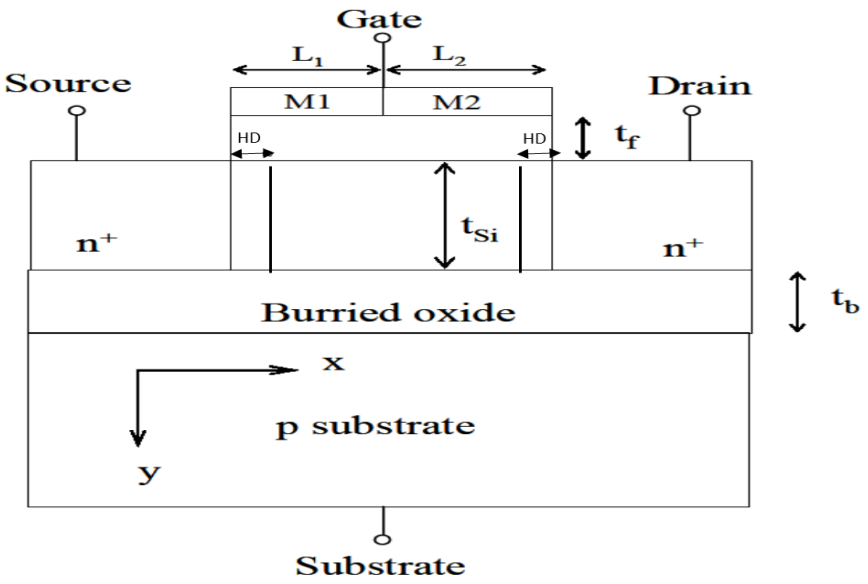


Figure 5.8 DHDM-SOI MOSFET Structure

The simulations are performed using TCAD software and the drain current characteristics are plotted in Figure 5.9. The device is designed with a single halo doping and a dual halo doping in the channel region and their characteristics have been compared. The optimized halo doping facilitated the device to be used in low power applications [38]. The velocity of the electrons in the form of impurity scattering along the channel was reduced by the use of doping engineering in this optimized device resulting in less collision between electrons and atoms in the DHDM-SOI device.

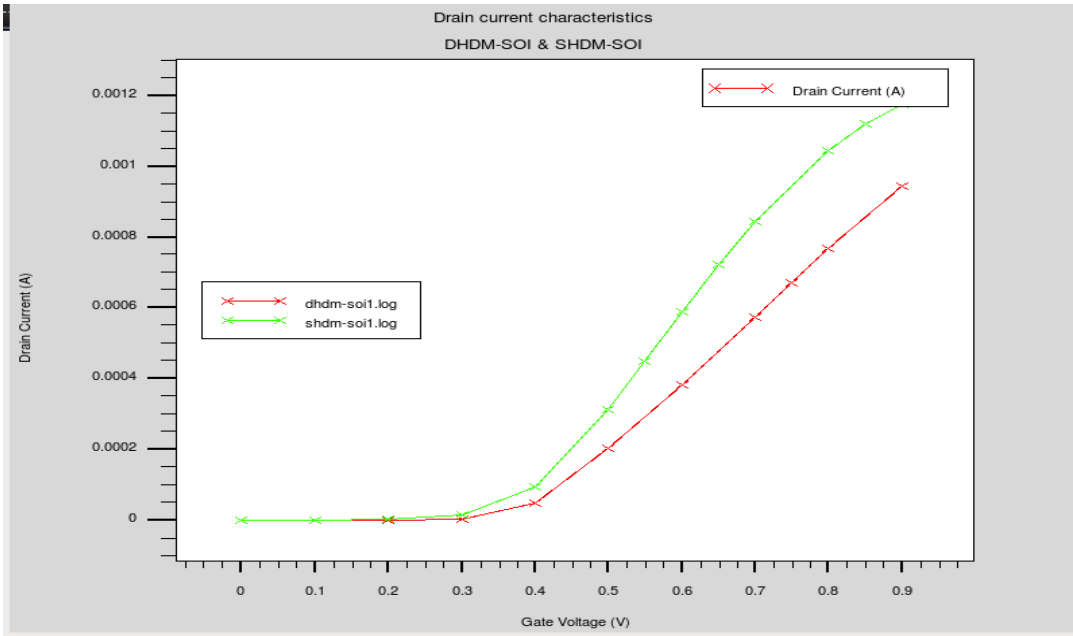


Figure 5.9 Drain current characteristics of SHDM-SOI & DHDM-SOI

The comparison of drain current with single halo doping and dual halo doping in the channel has been observed in Figure 5.9. DHDM-SOI is having less ON current and less OFF-state current as shown in Figure 5.9 and Figure 5.10 respectively.

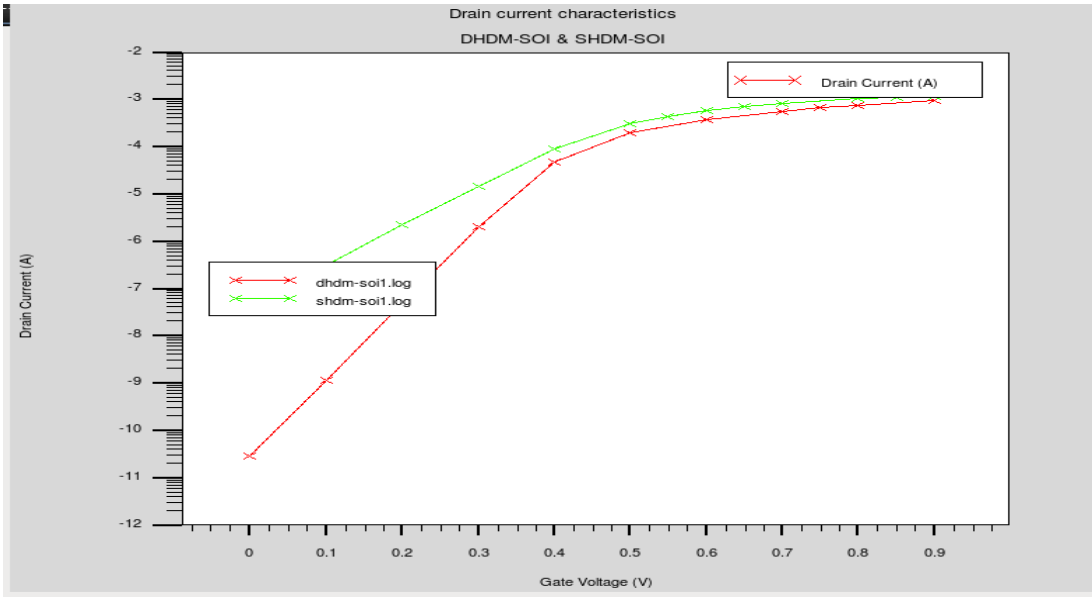


Figure 5.10 Comparison graph of SHDM-SOI & DHDM-SOI MOSFET

Figure 5.11 below shows the drain current characteristics of the dual material SOI (DM-SOI) MOSFET, single halo dual-material (SHDM-SOI) MOSFET and dual halo dual-material (DHDM-SOI) MOSFET.

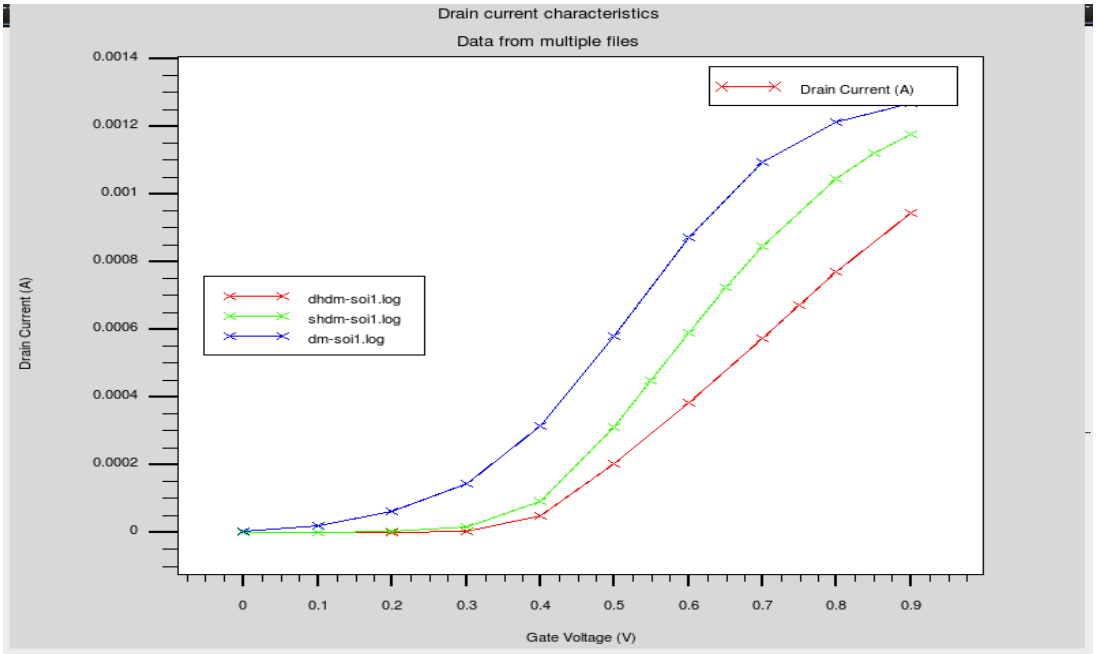


Figure 5.11 Drain current characteristics of DM-SOI, SHDM-SOI & DHDM-SOI

It has been observed that Dual material (DM–SOI) MOSFET is the best device in those terms of drain current and Dual Halo Dual Material (DHDM–SOI) MOSFET is best in the terms of sub-threshold leakage current as observed in Figure 5.12. Table 5.1 shows the comparison of simulated device data with the previous work done.

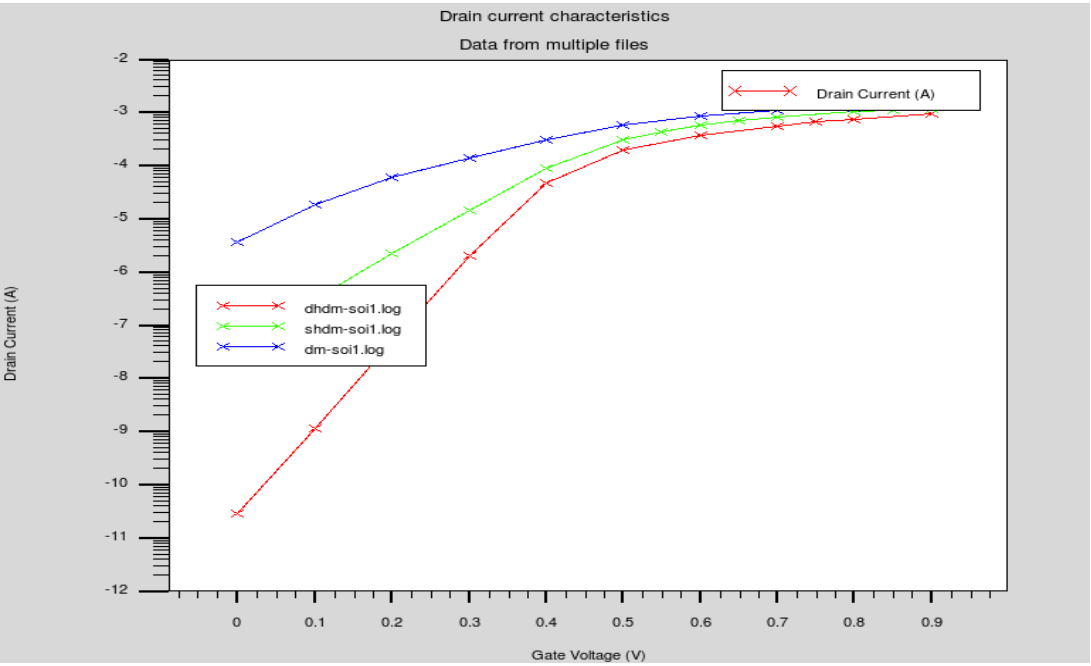


Figure 5.12 Comparison graph of DM-SOI, DMSH-SOI & DMDH-SOI MOSFET

Table 5.1 Comparison of Simulated SOI Device Results with Literature

S.No.	Parameter	Karbalaei et al [131]	Simulated Data
1.	Sub-threshold current	0.44 e-9 A	2.89 e-11 A
2.	Drain Current	0.23 mA	0.94 mA
3.	Ion/Ioff Ratio	53 e+4	32.6e+06
4.	SS (mV/dec)	74	61.5

5.3 Conclusion

Dual material SOI (DM-SOI), Single Halo Dual material (SHDM –SOI) MOSFET and Dual Halo Dual material (DHDM –SOI) devices has been designed in this chapter. The surface potential is analytically estimated, simulated using TCAD tools and compared with each other. The drain current and off-state leakage current have been estimated for all these devices. It has been observed that DHDM-SOI MOSFET gives the best value of leakage current equals to 2.89×10^{-11}A and DM-SOI MOSFET gives the best value of drain current equals to 1.26mA. The effect on the subthreshold characteristics of the device is also seen with variations in silicon film thickness, work-function and drain bias. It has been concluded that when the length of the control gate increases as compared to two screen gates, the device has enhanced stability.

CHAPTER 6

CHARACTERIZATION OF G-SOI MOSFET

This chapter is focused on the design, virtual fabrication, simulation and analysis of Graphene-Silicon on Insulator (G-SOI) using TCAD software. The entire virtual fabrication process, design and simulation are done in the ATLAS device simulator. Several materials are utilized to enrich the performance of the device. Silicon field-effect transistor is the leading pretender in the tremendous semiconductor world. The two-dimensional materials like graphene are seizing the market day by day. Graphene-Silicon on Insulator (G-SOI) is a majestic device that is very much appraised by electronic industries these days because of its higher mobility and ON current. G-SOI is presented here with various substrates and different oxide materials to acquire the reduced leakage current, saturation slope and Drain Induced Barrier Lowering (DIBL) with enhanced drain current. The performance of the device depends upon various parameters i.e. contact doping, gate insulator dielectric constant, graphene film thickness, oxide thickness, etc. The choice of a suitable gate dielectric constant is important in determining device performance. The comparative analysis after computational simulations results showed that G-SOI provides times more I_{ON}/I_{OFF} ratio than other devices like conventional SOI devices [58] [133]. It is a viable option for low power digital applications in Nano-electronics. After analysing the simulation outcomes, it has been found that G-SOI with hexagonal Boron Nitride as substrate and Lanthanum Gadolinium oxide as a gate oxide gives higher trans-conductance, lower Sub-threshold Swing, lower OFF-state current (I_{OFF}), and better drain current to OFF-state current ratio (I_{ON}/I_{OFF}). Graphene is a single-atomic-thick material with extremely high mobility and thermal conductivity. Due to the ultra-high electron mobility of more than 200,000 cm^2/V sec calculated in ejected graphene, it is considered one of the most promising channel materials for fast transistors. It can be used in wireless communication circuits and RF applications in the future [134] [78].

6.1 ULTRA-THIN BODY SILICON ON INSULATOR (UTB-SOI) DEVICE

Silicon on Insulator (SOI) technology arose in the picture after scaling of various parameters which results in the short channel effects [72]. When the channel length of MOSFET decreases, the ability to control the gate reduces. As a result, the threshold voltage of the MOS reduces which further results in Drain-induced barrier lowering (DIBL).

An SOI is a semiconductor device where a silicon or germanium semiconductor layer is created on an insulating layer that is a buried oxide (BOX) layer created on a silicon substrate. Two kinds of SOIs are available: Fully Depleted SOI (FDSOI) and Partially Depleted SOI (PDSOI). In n-type Partially Depleted SOI, the p-type film is inserted between the gate oxide layer and buried oxide layer so that the depletion region cannot shield the entire p-type region [135]. Thus, this form of SOI works like bulk MOSFET to some extent. The film in FDSOI MOSFET is very narrow so that the depletion region includes the entire film. PDSOI operates at a high velocity compared to bulk MOSFETs. It is least preferred because of its floating body effect. The silicon thickness has been decreased to decrease the floating body effect which innovative a new tool called FDSOI. Further study on ultra-thin body (UTB) SOI results in FDSOI [136].

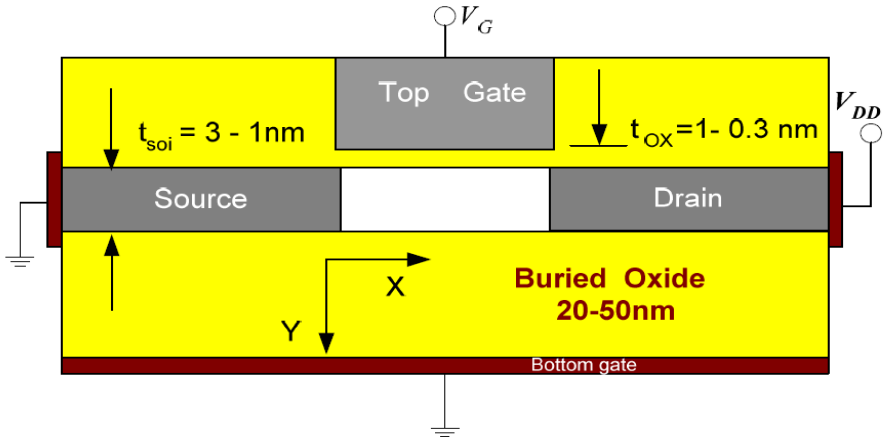


Figure 6.1 UTB-SOI Structure according to ITRS

The primary distinction between FDSOI and UTB-SOI is the thickness of the silicon layer. Usually, the thickness of the silicon layer for UTB-SOI transistors is less than 10 nm. UTB-SOI comprises dual gates: the top and bottom gate. Both the gates can be used to control together to get a higher I_{ON}/I_{OFF} ratio. According to ITRS guidelines [137], the

thickness of oxide can be taken from 0.3 nm to 1nm, the thickness of silicon can be taken from 1nm to 3nm and thickness of buried oxide can be taken from 20-50nm. The basic structure of UTB-SOI is as shown in Figure 6.1. According to ITRS guidelines, the scaling in MOSFET is as shown in Table 6.1. It shows the technology is scaling down from 90nm to 22nm [120] as the years are passing on for MOSFETs according to ITRS. The effective channel length is also scaled down from 37nm to 9nm. Similarly, the thickness of silicon and thickness of buried oxide are also scaled down according to the length defined [42].

Table 6.1 ITRS Technology map

Year	2004	2007	2010	2013	2016
Node of Technology	90	65	45	32	22
Lg	37	25	18	13	9
ITRS'03(Initial-$t_{silicon}$)	21-39	18-33	15-19	14-16	13-14
ITRS'01(Final-$t_{silicon}$)	(11-19)	(8-13)	(5-9)	(4-7)	(3-5)
ITRS'03(Initial-tbox)	56-94	42-70	26-44	18-32	14-22
ITRS'01(Final-tbox)	(28-46)	(19-31)	(14-23)	(10-16)	(7-11)

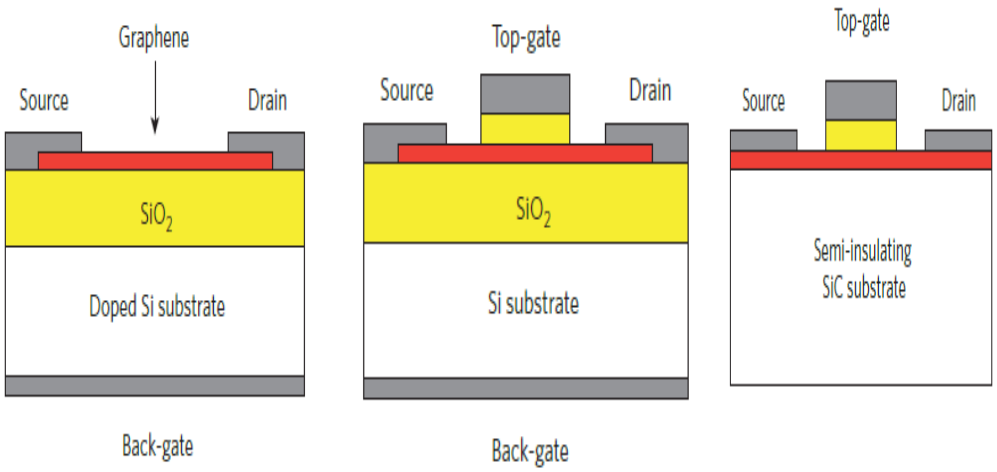
Table 6.2 ITRS Technology specifications

L_e [nm]	15		12.5		10		7.5		5	
Thickness scaled[nm]	$t_{silicon}$	t_{oxide}	$t_{silicon}$	t_{oxide}	$t_{silicon}$	t_{oxide}	$t_{silicon}$	t_{oxide}	$t_{silicon}$	t_{oxide}
Non-Scaled	3	1	3	1	3	1	3	1	3	1
t_{oxide}: linearly scaled	3	1	3	0.8	3	0.7	3	0.5	3	
$t_{silicon}$: constant										
t_{oxide}: constant	3	1	2.5	1	2	1	1.5	1	1	1
$t_{silicon}$: linearly scaled										
t_{oxide}: linearly scaled	3	3	2.5	0.8	2	0.7	1.5	0.5	1	0.3
$t_{silicon}$: linearly scaled										
t_{oxide}: linearly scaled	3	1			**2.5**	**0.7**			2	0.3
$t_{silicon}$: Sub-linearly scaled										

Table 6.2 shows the scaling down of channel length for SOI devices from 15nm to 5nm according to ITRS. Initially, the device is designed using these specifications given in the above table. The device having 10nm channel length, 2.5nm gate oxide thickness (t_{ox}), 0.7nm silicon thickness has been designed, virtually fabricated and simulated.

6.2 GRAPHENE SILICON ON INSULATOR (G-SOI)

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are the main design block of semiconductor technology in Very-Large-Scale Integration (VLSI) chips. The design of VLSI chips increases the desire of shrinking the dimensions by shrinking the channel length of the device. The device offers greater speed and dynamic power consumption efficiency. Investigations are being carried out to improve the performance of VLSI Chips. After the evolution of Single gate MOSFETs, the technology Silicon on Insulator (SOI) came. There were some problems of increased tunneling current which is reduced by using double-gate MOSFETs. Due to high sub-threshold current, reduced ON current and decreased Ion/Ioff ratio reduces the use of double-gate MOSFETs in the market. Researchers found a new promising material to be used in MOSFETs to boost the performance of the device. Graphene is a relatively new material with distinctive characteristics for electronic applications [31] [127]. The Silicon MOSFETs with 22nm channel length are fabricated till now. As stated by the International Technology Roadmap for Semiconductors (ITRS) there is a requirement of 10-nm MOSFETs in 2020 and further. Silicon MOSFETs cannot be scaled further because of short channel effects which degrades the performance of the device. To control the short channel effects, the device's structure is further modified with some new materials to enrich the performance of the device. Graphene with its high mobility is a promising material to achieve the high ON the current of the MOSFETs. The available structures of G-SOI are given below:



(a) Back-gated G-SOI (b) Top-gated G-SOI (c) SiC substrate G-SOI

Figure 6.2 various structures of G-SOI

Figure 6.2 shows the different available structures of G-SOI. Figure 6.2 (a) shows G-SOI having silicon substrate, graphene channel, and back-gate. Figure 6.2 (b) shows G-SOI having silicon substrate, graphene channel, top gate and back-gate. Figure 6.2 (c) shows G-SOI having Silicon carbide (SiC) substrate [81], graphene channel and top-gate [79].

The narrow channel region can suppress short-channel effects by scaling theory and therefore allow MOSFETs to be assessed in very short channel lengths. Graphene's two-dimensional aspects imply the thinnest channel possible. Hence, MOSFETs should be more feasible than their competing products [80]. The recent ITRS roadmap highly proposes enhanced graphene research and even includes carbon-based Nano-electronics research and development. The race is still open and at least as promising as those for alternative ideas are the prospects for graphene devices. GNR MOSFET was previously developed with 50 nm gate-length and a work-function equivalent to the GNR electron affinity with a distance from origin and gate-drain of 50 nm. [77].

Graphene can be used as an oxide material or as a channel material in MOSFETs. Here the double-gate transistor with a graphene channel is modeled. This type of G-SOI has two gates: Top gate and Back gate. Both the gates are connected electrically so the graphene channel conductivity can be effectively modified by both the top and bottom gates [138]. This material gives its best properties whenever used in different places. The substrate can be replaced by other materials also like H-BN [139], SiC and the low k gate oxide material can be replaced by high k. SOI devices were designed after double gate

MOSFETs to get efficient circuit/device performance. The design of G-SOI gets motivation from SOI devices with improved performance [140]. Then the silicon is replaced by graphene material following high k material to give low leakage, high on/off ratio and high trans-conductance device.

6.3 DEVICE MODELLING

There are various modeling approaches of graphene transistors viz. ab initio, atomistic modeling, semi-classical device modeling and analytical modeling. With the tradeoff between accuracy and computational cost, these approaches utilize different methods to model the graphene transistors. The main objective is to accurately define the ad hoc level hierarchies and information exchange interfaces between the multistage systems.

To model large-scale graphene devices, a semi-classical modeling approach with numerical solutions is needed for providing information for device parameters and geometry optimization. These analytical models can be directly imported into commercial software such as circuit analysis. The potential distributions are computed by solving 2-D Poisson Equation at any plane section of the G-SOI [141]. 2-D Poisson Equation is given by equation given below:

$$-\varepsilon_0\varepsilon_r\left[\frac{\partial^2 V(x,y)}{\partial x^2}+\frac{\partial^2 V(x,y)}{\partial y^2}=\rho_{dep}\right] \tag{6.1}$$

whereas ε_0 is the free space's electrical permittivity, ε_r is the relative permittivity, ρdep is the density of the depletion charge

$$\rho_{dep}=qN_D \tag{6.2}$$

Wave function distributions are estimated at any cross-section of the G-SOI channel by solving the 2-D Schrödinger Equation [141]. The 2D Schrödinger Equation is given by:

$$-\frac{\hbar^2}{2m_{yi}^*}\frac{d^2}{dy^2}\varphi_{ij}(y,z)-\frac{\hbar^2}{2m_{zi}^*}\frac{d^2}{dz^2}\varphi_{ij}(y,z)+c(y,z)\varphi_{ij}(y,z)=E_{ij}\varphi_{ij}(y,z) \tag{6.3}$$

where $c(y,z)$ is the conduction band profile, E_{ij} is the Eigen energy, $\varphi_{ij}(y,z)$ is the wave function distribution, m_{yi}^* and m_{zi}^* are the effective masses.

The drain current is calculated by 2-D Poisson- Schrödinger Equation:

$$I_D = W.\left[\frac{q}{\hbar^2}\sqrt{\frac{m_c}{2}}.\left(\frac{k_BT}{\pi}\right)^{\frac{3}{2}}\right]\left\{\frac{\mathcal{F}_1}{2}\left[\frac{(E_F-E_i)}{k_BT}\right]-\frac{\mathcal{F}_1}{2}\left[\frac{(E_F-E_i-qV_D)}{k_BT}\right]\right\} \quad (6.4)$$

where m_c is the conductive effective mass, E_i is the sub-band energy and $\frac{\mathcal{F}_1}{2}$ is the Fermi-Dirac integral. The surface potential of G-SOI has been analytically calculated and simulated in TCAD device simulator. The comparative results are shown in Figure 6.3.

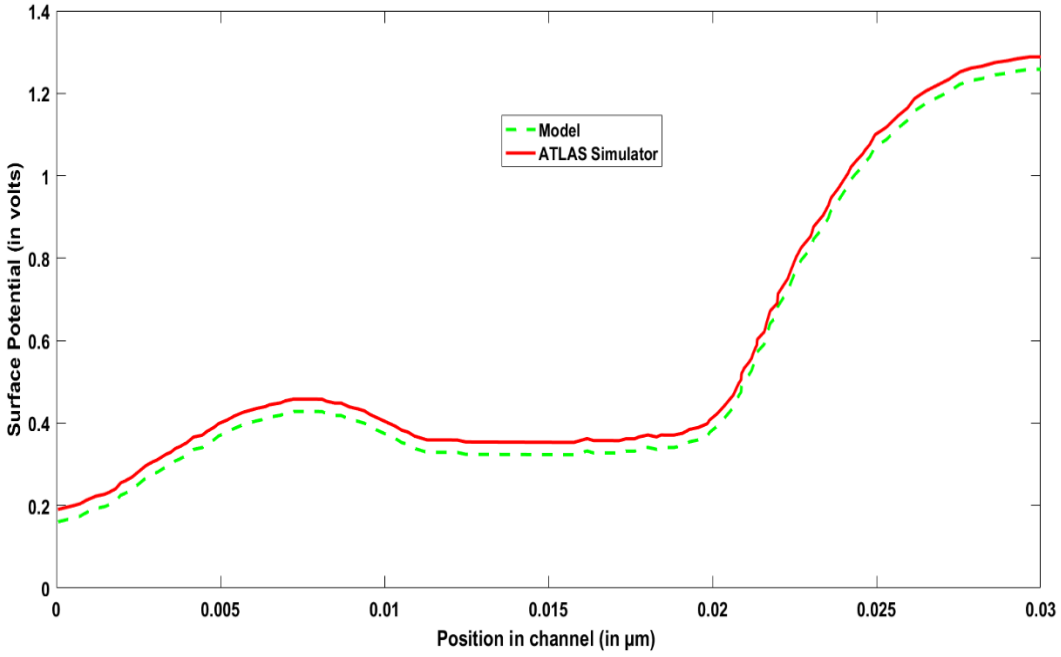


Figure 6.3 Potential distribution graph of G-SOI

The estimated and simulated surface potential values at a particular drain bias voltage is plotted against the horizontal distance x for L=0.03 μm. The simulation results are validating the derived analytical model of the device. The conduction band and valence band profiles are as shown in Figures 6.4 and Figure 6.5

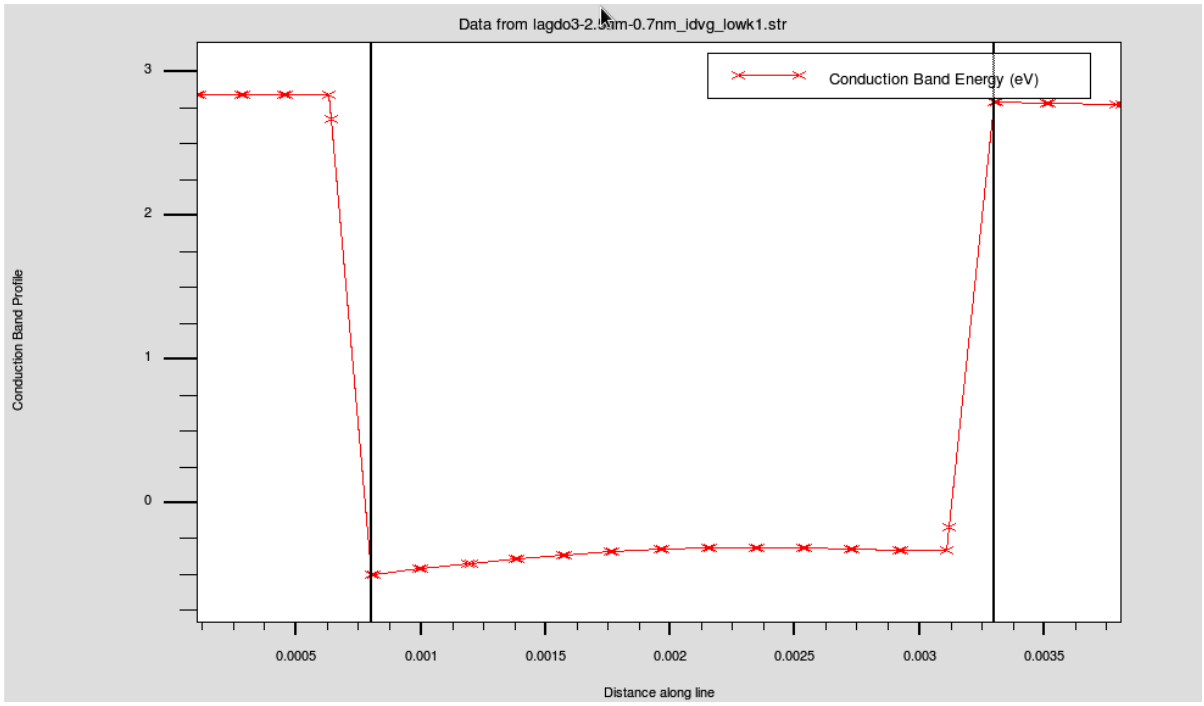


Figure 6.4 G-SOI Conduction Band Profile

Figure 6.4 above demonstrates G-SOI's conductive band profile. A cutline is being taken through the source and drain to get the band properties.

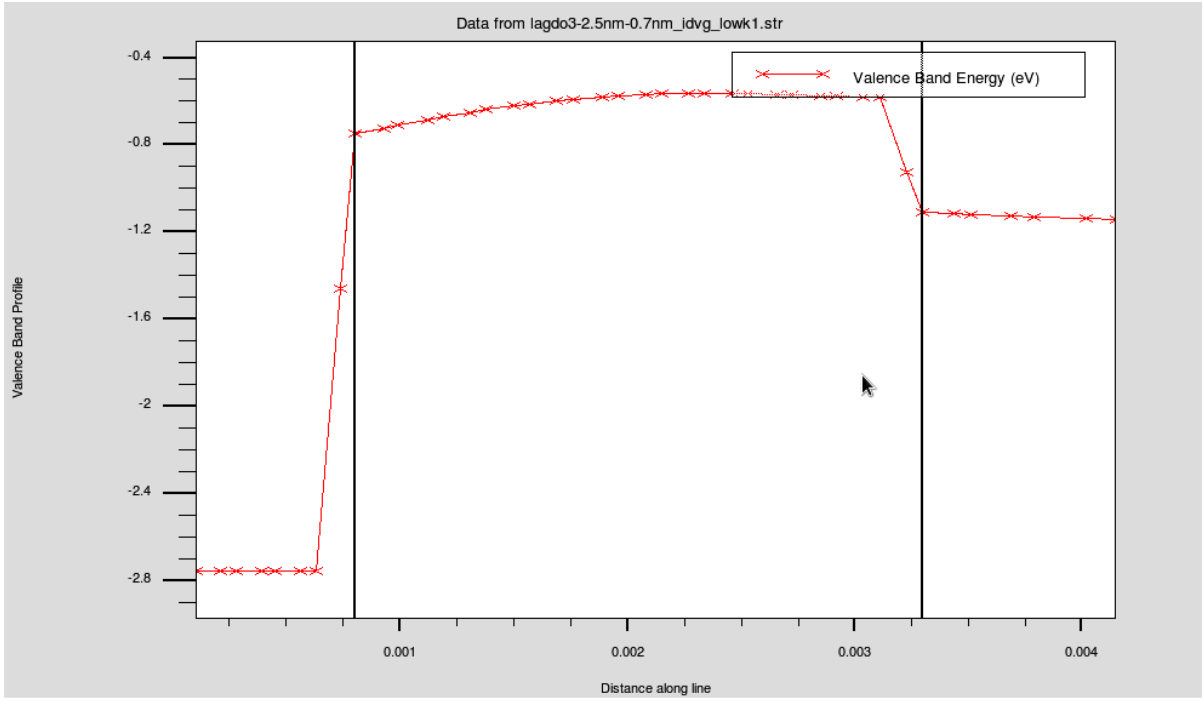


Figure 6.5 Valence band profile of G-SOI

The above Figure 6.5 shows the valence band profile of G-SOI. A cutline is being taken through the source and drain to get the valence band graph. In order to achieve the distinct Eigen states (i.e. sub-bands), 2-D Schrödinger equation is solved for the respective conductive band profile. Figure 6.6 also predicts the wave function distributions analogous to the distinct sub-bands.

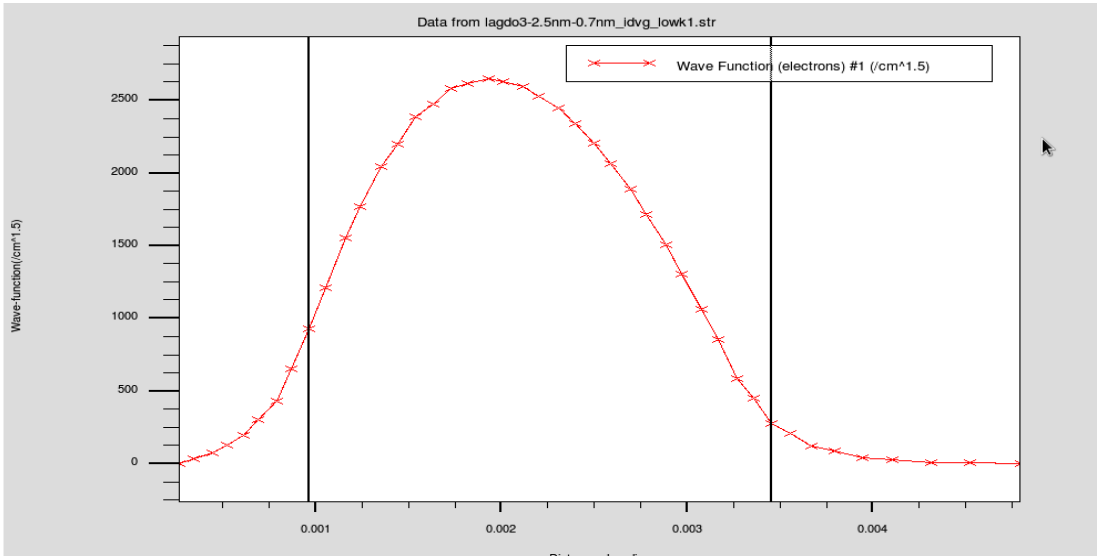


Figure 6.6 Wave function distribution graph

The drain current is calculated by Equation 6.3 after solving the 2-D Poisson-Schrödinger Equation and the results are shown in Figure 6.7

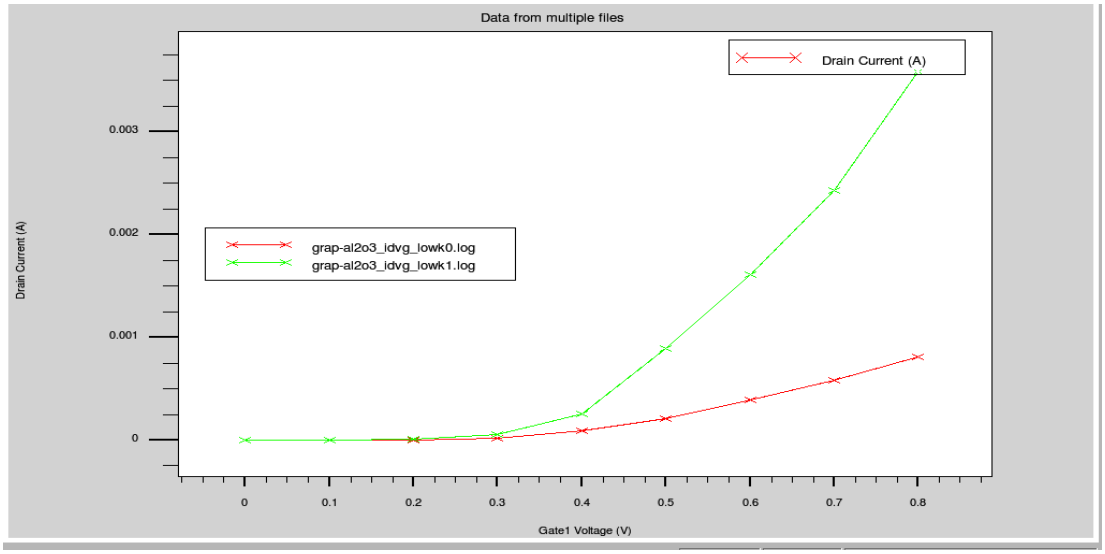


Figure 6.7 I_D-V_{GS} Plot of G-SOI at V_{DS}=0.8V

Graphene was verified as the products valued for upholding Moore's Law as silicon approached its boundaries. The incredible electronic characteristics of high mobility graphene-like increased saturation velocity, etc. became a golden shoot for graphene-based electronics [142]. This chapter is focused on the study of graphene FETs using NEGF formalism in the sub-micro-meter regime. The most demanding approach used to model carrier transport in nanoscale FETs is non-equilibrium Green's Function approach (NEGF) which is based on solving Schrödinger Equation under non-equilibrium conditions. NEGF formalism has been successfully applied to study quantum transport in conventional silicon MOSFETs, carbon nanotubes (CNTs) etc [16]. The device is designed with 2D [29] graphene material as a channel material and h-BN material as substrate material having following specifications as shown in the Table 6.3 below

Table 6.3 Material Design Specifications

Material	2D-Graphene	Hexagonal Boron Nitride (h-BN)
Energy Band gap (eV)	0	3.9
Electron affinity (eV)	4.24	1.11
Permittivity	4.22	4.2

6.4 DEVICE FABRICATION AND SIMULATION

Since the last ten years, the device scales into the deep sub-micron lengths, transistors have been overwhelmed by short channel effects. In specific, Drain Induced Barrier Lowering (DIBL) is associated with a failure of electrostatic gate control loss over the channel potential in short channel devices resulting in a dramatic rise in leakage currents and in the worst scenario, inhibiting the turn-off device [24]. Strategies to improve gate control have led to the development of ultra-thin-body SOI, FinFET and gate-all-around MOSFET technologies, targeting to reduce the cross-section and surface-to-volume ratio of the channel material with respect to the gate. Graphene, as a two-dimensional material would represent the ultimate surface-to-volume scaling and allow for excellent electrostatic gate control.

The device is initially designed and simulated using ATLAS SILVACO. The design specifications are considered according to ITRS guidelines. The channel length, L_G is

taken 10nm oxide thickness, t_{ox} equals 0.7nm and silicon thickness t_{si} equals 2.5nm. The gate oxide material is taken Al_2O_3 which is a high permittivity material. Generally, Silicon is taken as a channel material in MOSFETs but here the device is designed using a new 2-D material known as Graphene. The silicon material in the channel region is replaced by Graphene material. The simulated structure of G-SOI is given below in Figure 6.8

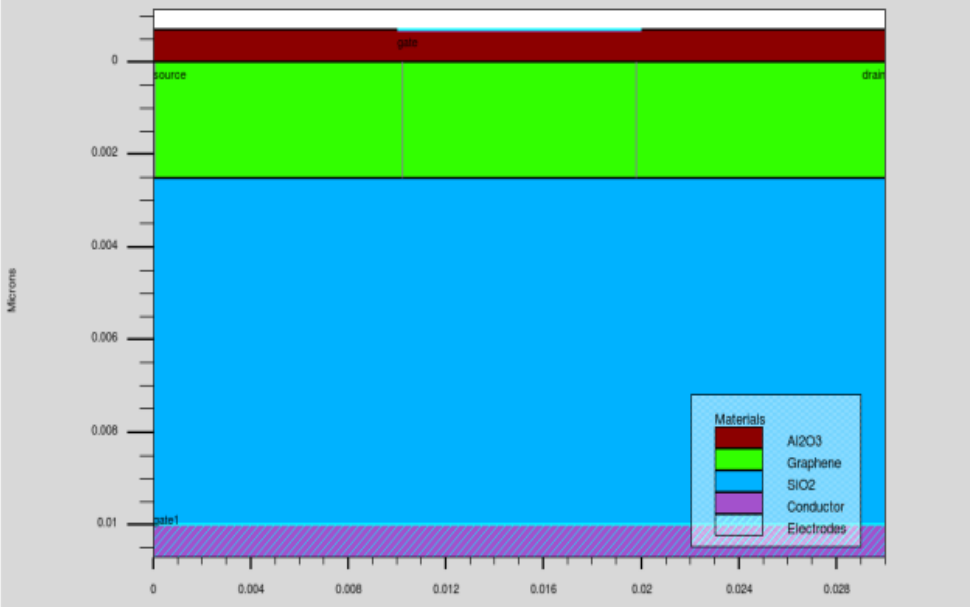


Figure: 6.8 Simulated Structure of G-SOI

The simulation is performed using the Non-Equilibrium Green (NEGF) model to obtain the device's performance metrics [74]. In G-SOIs, Graphene material is incorporated as a channel material instead of silicon building a difference between FET and G-SOI [143]. The device is designed and virtually fabricated in ATLAS of SILVACO TCAD tools. It is initially designed using silicon dioxide, SiO_2 as buried oxide, Graphene as channel material and Aluminium oxide, Al_2O_3 as gate oxide material.

Al_2O_3 is replaced by hexagonal boron nitride, h-BN material which is employed to increase the band-gap of zero band-gap graphene material. To study and simulate the behavior of the G-SOI device, Non-equilibrium Green's Function (NEGF) method is used. The method is implemented on a device using the SILVACO ATLAS tool. The channel is lightly doped, the main innovative research to design this device [144]. The graphene is a metalloid and gapless material whereas h-BN is a semiconductor material with a huge band-gap [145]. Due to its atomically soft surface, the h-BN material is used

as a substrate with graphene channel devices and a large lattice constant than graphene, free of destructive bonds, atomically smooth, comparatively chemically inert having a low-density stimulating impurity. Various substrates are used with graphene channel devices like SiC, SiO_2 but h-BN substrates are giving the best performance among all. Additionally, High k gate oxides are used to enrich the performance of the device. The combination of graphene and h-BN gives a higher ON/OFF ratio, reduced leakage current, and DIBL. The gate oxide material, Al_2O_3 is replaced by Hafnium Oxide, HfO_2 having permittivity 22, electron band offset~2.57eV and hole band offset of ~1.91eV. The analysis of the device is done. After that HfO_2 is replaced by Lanthanum Gadolinium Oxide ($LaGdO_3$) having dielectric constant (k) of ~ 22, a large bandgap of ~5.6eV, electron band offset~2.57eV and hole band offset of ~1.91eV. The analysis of the proposed device with HfO_2 gate oxide and improved device with $LaGdO_3$ has been done. It has been observed that the improved G-SOI with $LaGdO_3$ is providing a better Ion/Ioff ratio [146][147], better leakage current and improved DIBL than other devices.

6.5 PARAMETER EXTRACTION AND COMPARATIVE ANALYSIS

After the design and fabrication of the device, various processes and device factors are extracted to analyse the behavior of the device. Utilization of high-k materials is required to improve the performance of the device. The threshold voltage and sub-threshold slope after simulation of the device are extracted 0.30V and 65mV/decade respectively [148]. The comparative analysis is performed with various thin oxides and the gate oxide thickness is also varied step-by-step to analyse the thickness variation effect of the device.

6.5.1 Device with Different Gate Oxide Materials and Substrates

The device is simulated with different gate oxides and substrates. The drain current of all three devices is extracted and compared. It has been observed that G-SOI with the h-BN substrate and amorphous high k Lanthanum Gadolinium Oxide ($LaGdO_3$) [75] gate oxide has the highest drain current equals to 4.55 mA. Lanthanum Gadolinium Oxide ($LaGdO_3$) has a dielectric constant (k) of ~ 22, a large energy band gap of ~5.6eV, electron band offset~2.57eV and hole band offset of ~1.91eV. The CMOS logic circuits and memory chips were constructed from this recent innovated two-dimensional material nowadays [149-151]. The combination of Lanthanum and Gadolinium Oxide gives excellent performance devices. This gate oxide material has a higher electron band-gap and hole band offset than hafnium oxide used earlier. The channel doping and work-function [82]

is taken $1x10^{15}cm^{-3}$ (lightly doped) and 4.55eV respectively. The comparative analysis of drain currents with different gate oxides is as shown in Figure 6.9.

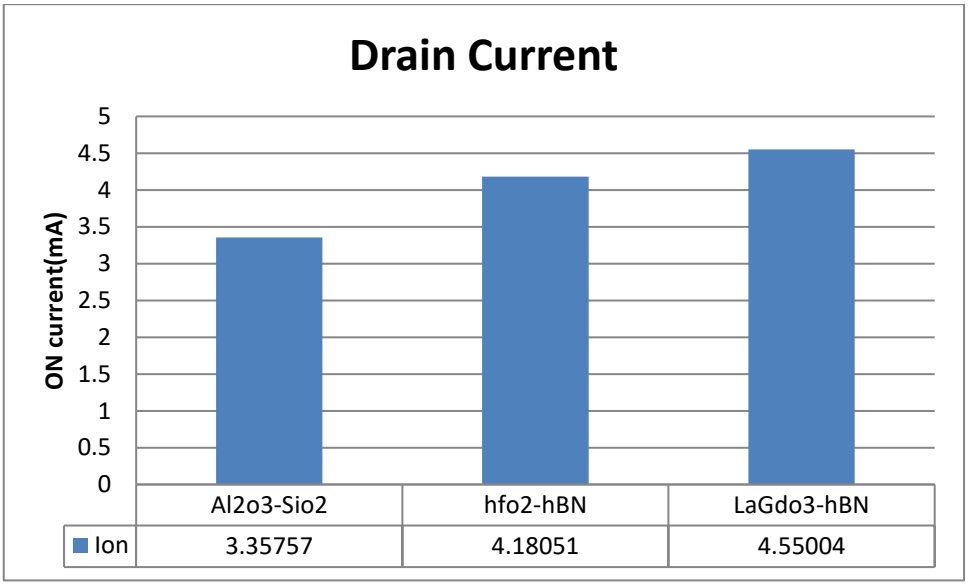


Figure 6.9 Drain Current Characteristics with Different Gate Oxide Materials

The existing sub-threshold is the undesirable current of leakage produced by MOSFETs owing to second-order effects. As per the extracted values, the proposed device has the lowest leakage current as shown in Figure 6.10

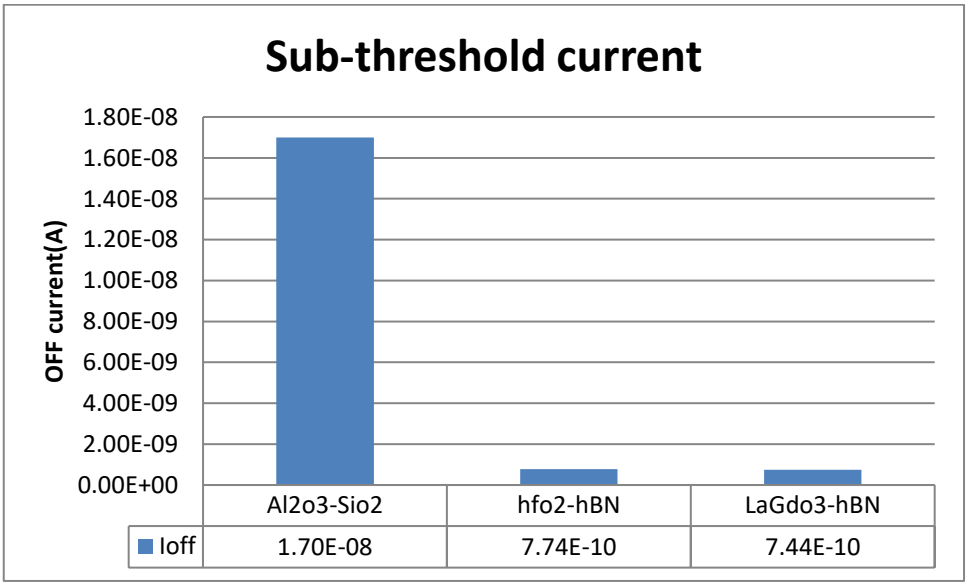


Figure 6.10 Sub-threshold current with Different Gate Oxide Materials

The high ON/OFF ratio is achieved by using an h-BN substrate with the Graphene channel and $LaGdO_3$ high k gate oxide as shown in Figure 6.11.

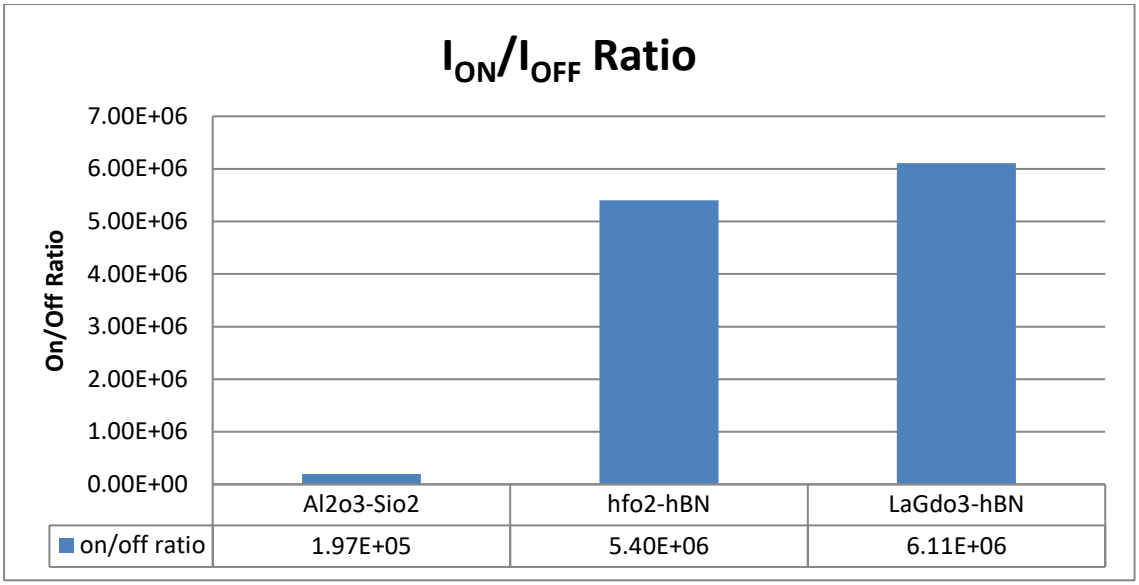


Figure 6.11 ON/OFF ratio Comparison with Different Gate Oxide Materials

DIBL is another type of leakage current that is least required to get a high-performance device. The proposed device has very little DIBL equals to 69.6mV/V as shown in Figure 6.12.

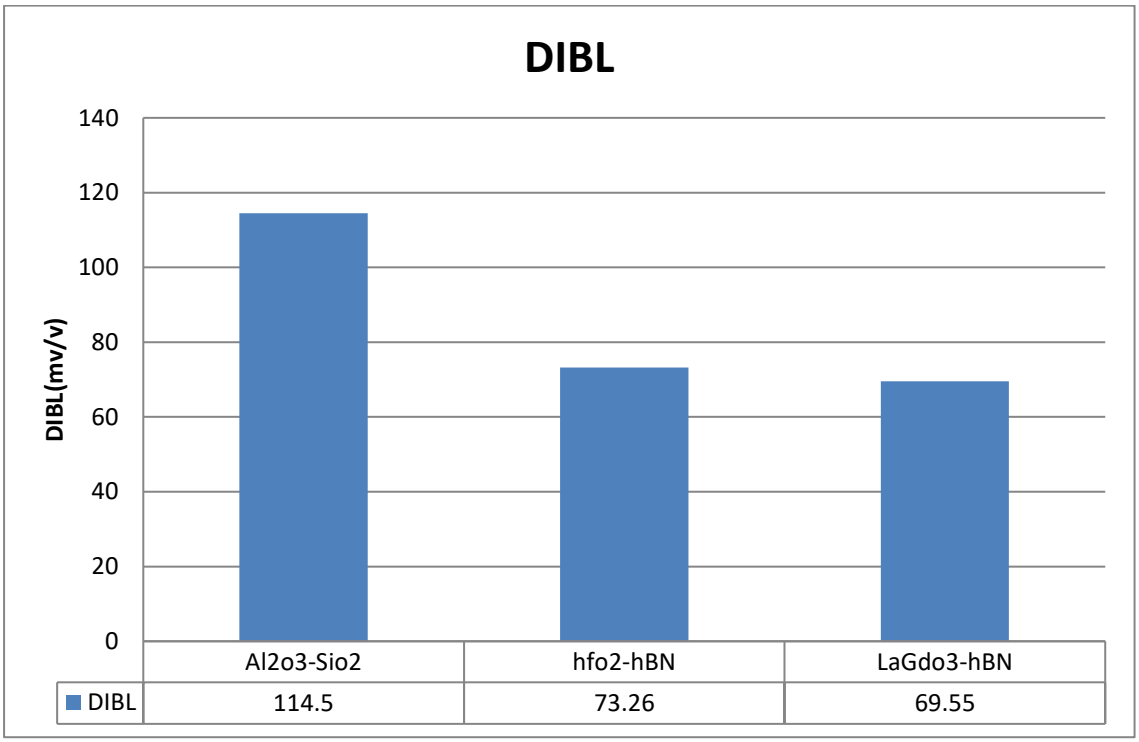


Figure 6.12 DIBL with Different Gate Oxide Materials

The conduction band and valence band comparison of all the three devices is shown in the simulated structure below in Figure 6.13. A cutline is being taken to plot the band characteristics of the device.

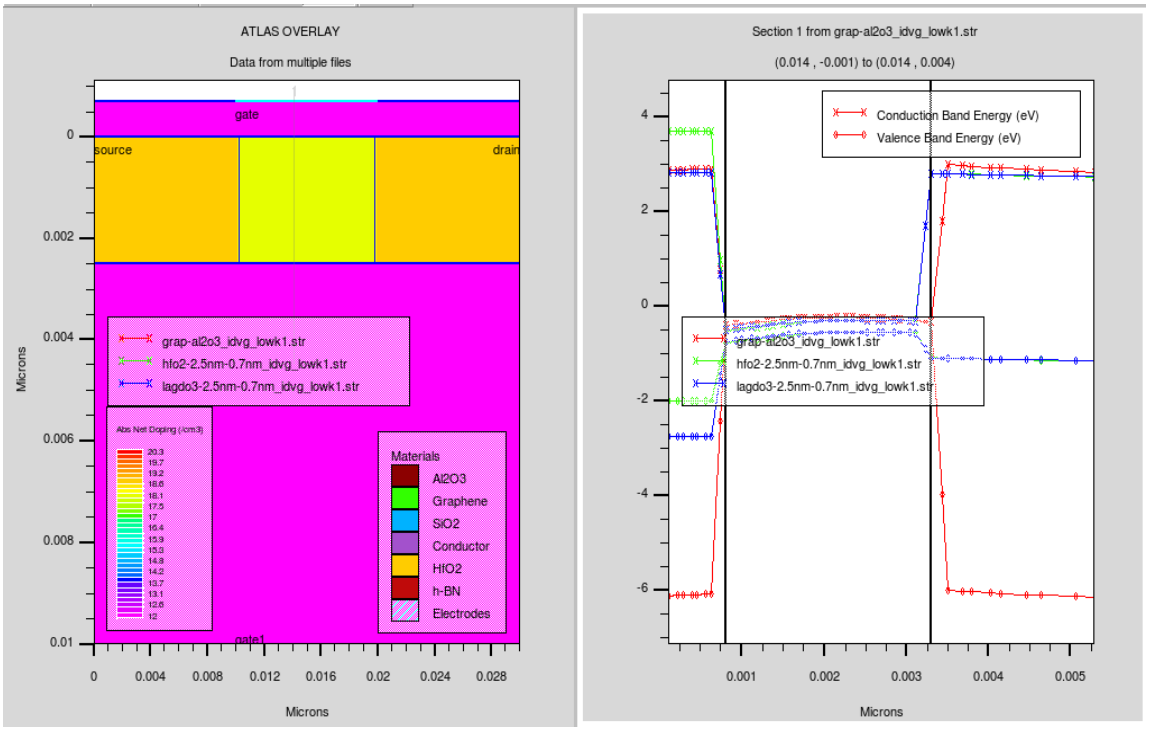


Figure 6.13 Comparison Curves of Band Structure with Different Oxide Materials

The current density is the amount of charge per unit time flowing from a selected cross-section per unit area. The Ohm's law states that the current density is proportional to the electric field. The electron current density of all three devices is as shown in Figure 6.14. It has been shown that high permittivity materials (HfO_2, $LaGdO_3$) have high electron density as compared to low permittivity devices (Al_2O_3).

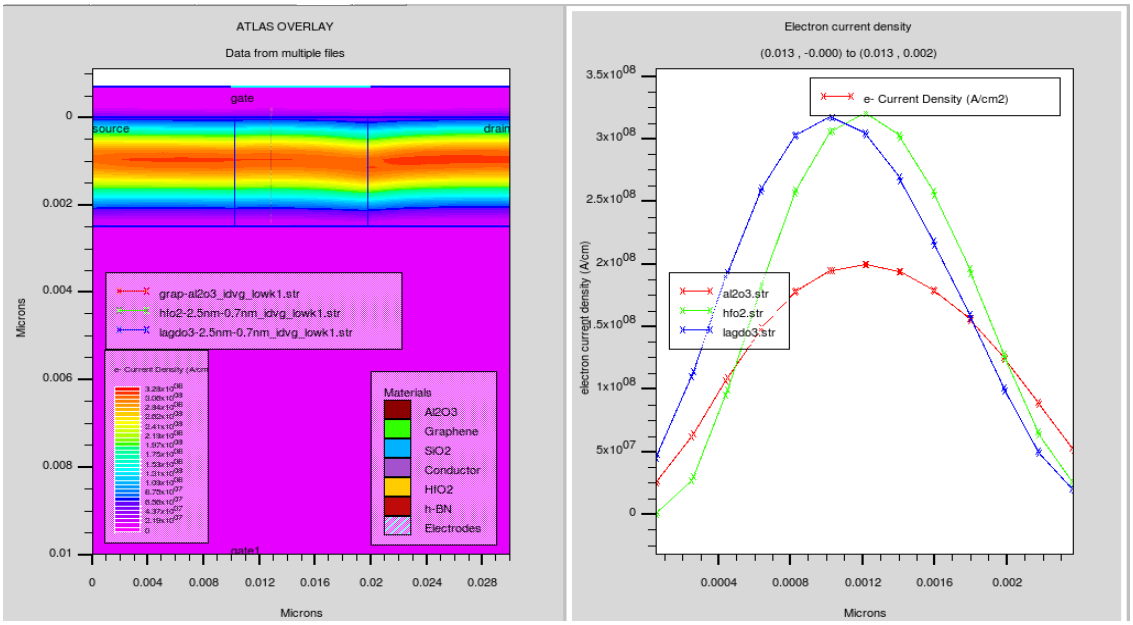


Figure 6.14 Comparison curves of Electron Density with Different Gate Oxide Materials

6.5.2 Device with Different Oxide Thickness

The gate oxide thickness may be varied to analyse the device's conduct [152-154]. Here, the thickness of the gate oxide can vary from 0.7 nm to 2.5 nm. The maximum current ~ 4.55mA, OFF current ~$7.44x10^{-10}$A and I_{ON}/I_{OFF} current ratio ~ $6.11x10^{+06}$ is obtained with a gate oxide thickness of 0.7 nm as shown in Figure 6.15, Figure 6.16 and Figure 6.17 respectively.

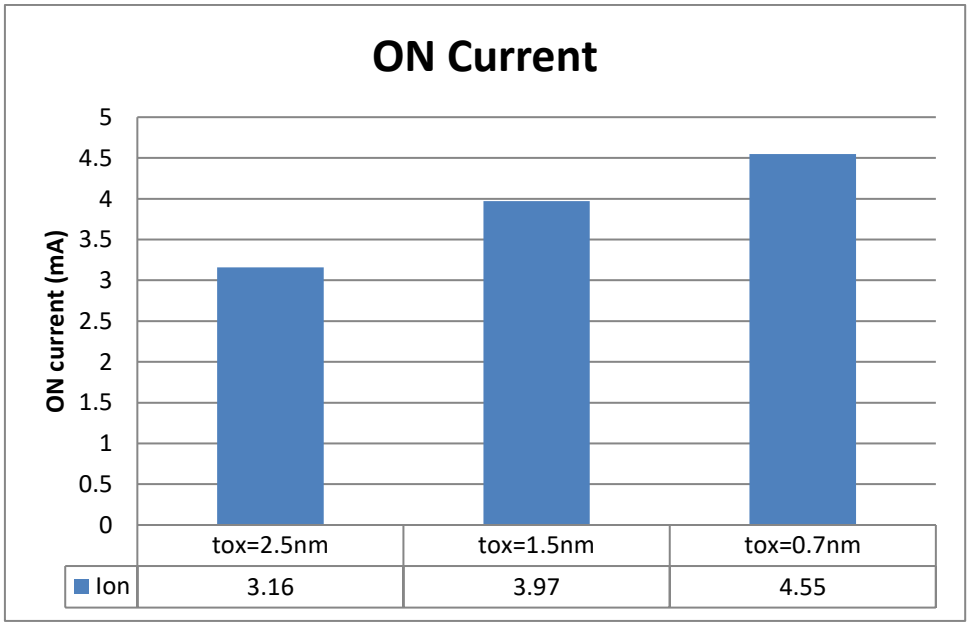


Figure 6.15 Drain Current Characteristics with Different Gate Oxide Thickness

With a gate oxide of 0.7 nm, the lowest off-state leakage current is obtained.

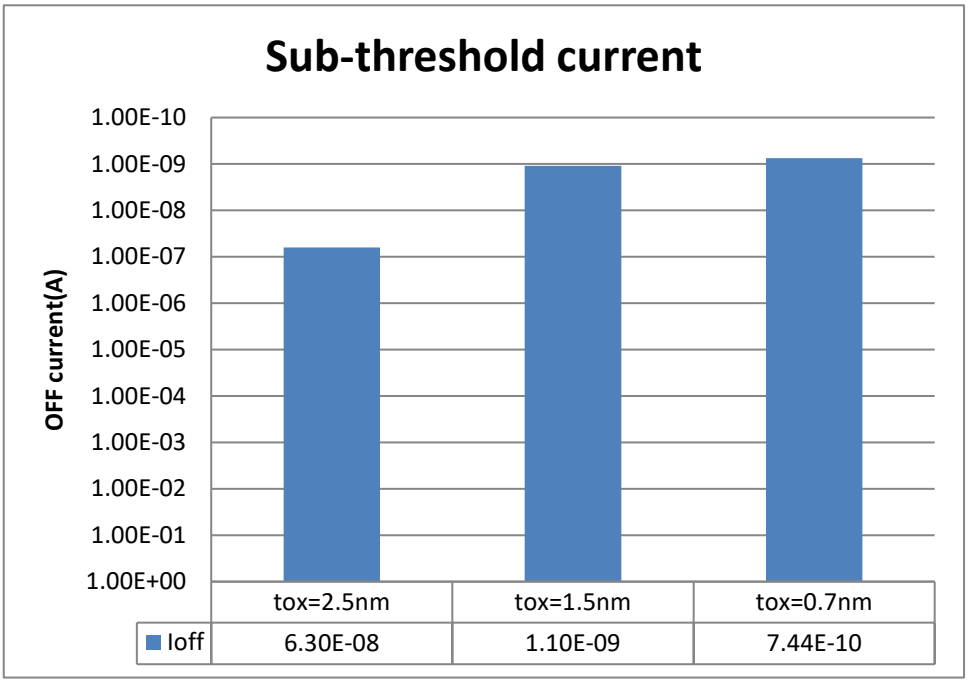


Figure 6.16 Sub-threshold current characteristics with different gate oxide thickness

The highest I_{ON}/I_{OFF} ratio is achieved with a gate oxide thickness of 0.7nm.

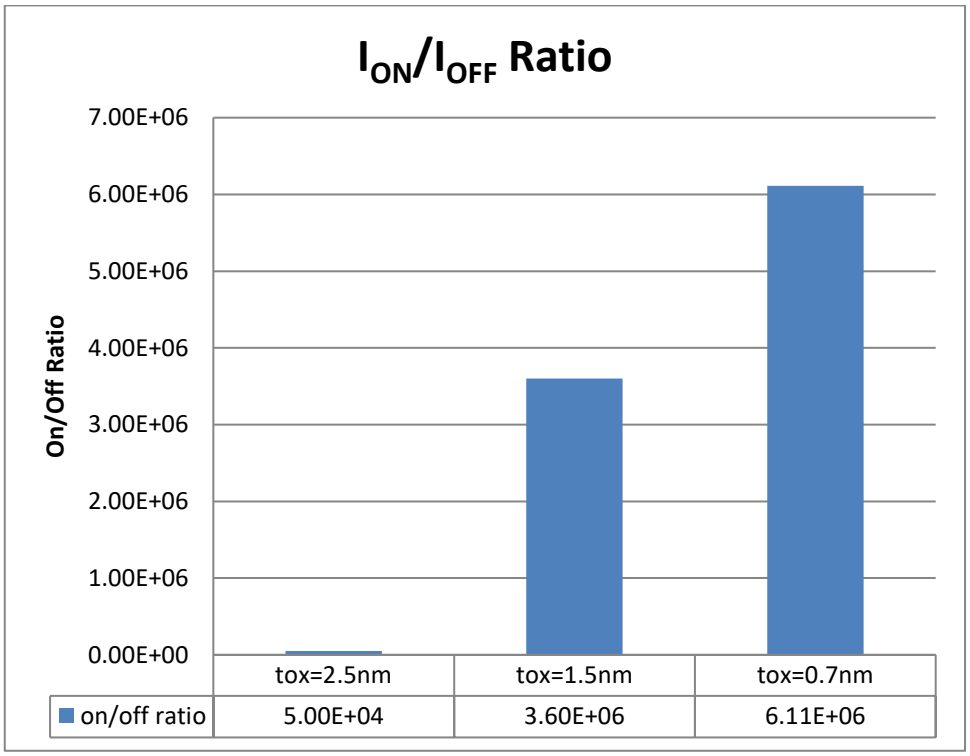


Figure 6.17 I_{ON}/I_{OFF} Ratios with Different Gate Oxide Thickness

The lowest DIBL noted at gate oxide thickness of 0.7nm.

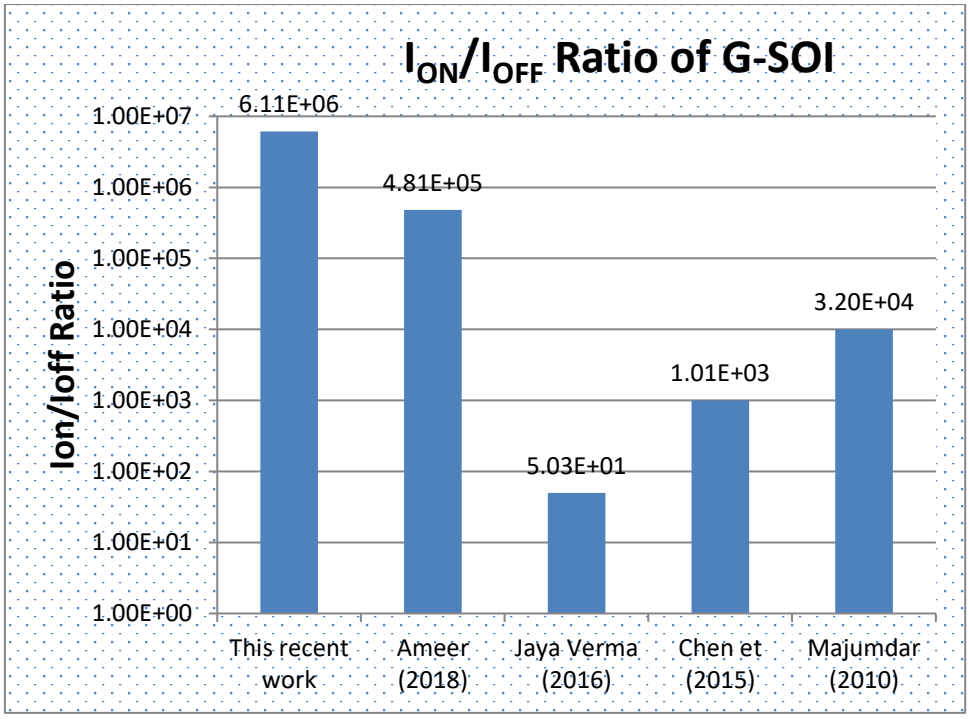


Figure 6.18 I_{ON}/I_{OFF} ratio comparisons with existing research work

Figure 6.18 shows the comparison of research work done here with previous research works [146]. The research work provides the optimized current ratio of I_{ON}/I_{OFF} equals to $6.11x10^{+06}$, which is the primary goal for attaining G-SOI design and simulation. To obtain the greater I_{ON}/I_{OFF} ratio, the process parameters can be modified. Using Graphene as a FET channel material ultimately dominates Si MOSFET which is one of the most important concerns in the latest years [155-158]. Off-state leakage has become feasible to enhance. Non-equilibrium Green's (NEGF) method is used to study G-SOI's transport behavior. The absence of an OFF state was the main obstacle to the digital circuit application of graphene-based transistors [159]. A feasible alternative is to open a bandgap in graphene, for instance by using bilayer graphene, nanoribbons, quantum [160] dots derivatives, high k materials and by having substrates of different materials other than silicon and SiC without degrading the electronic performance of graphene [161]. Minimum DIBL is obtained at selected specifications of the device taken shown in Figure 6.19. Table 6.4 shows the comparison of simulated device data with the previous works done.

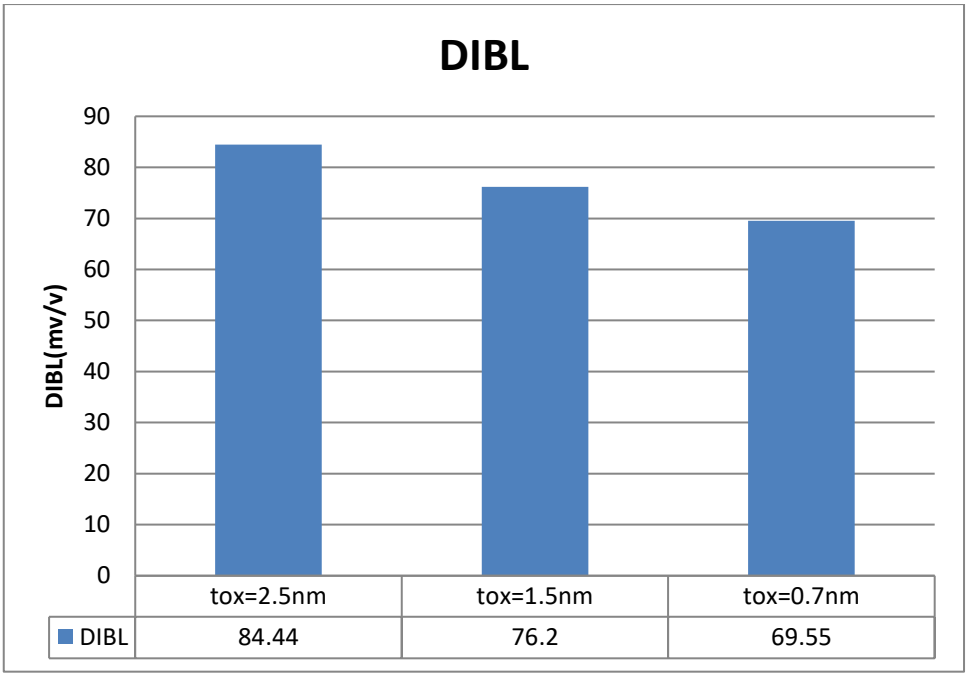


Figure 6.19 DIBL with different gate oxide thickness

Table 6.4 Comparison of Simulated G-SOI Device Results with Literature

S.No.	Parameter	Simulated Data	Heidari et al [140] Roslan et al [146]
1.	ON/OFF ratio	6.11e+06	4.81e+05 [146] 4.3 e+06 [140]
2.	Sub-threshold current	7.44e-10 A	5.401e-10 [146] 1.2 e-9 A [140]
3.	DIBL	69.55 mV/V	87 mV/V [140]

6.6 CV CHARACTERISTICS

The MOS capacitance is dependent on the input voltage connected to the gate electrode. When the gate voltage is applied, the C-V characteristics changes in three different regions of action: Accumulation region, Depletion region, and Inversion. Depending on the extraction techniques, there are three kinds of curves of CV: a theoretical curve of CV, a curve of low-frequency CV, and a curve of high-frequency CV. The MOS capacitance is measured at low-frequency by resolving normalized band bending y for each value of gate voltage which is given by:

$$y(V_G) = \frac{q}{kT}\left(V_G + \frac{Q_s}{C_{ox}}\right) \tag{6.5}$$

where y is the difference between normalized surface potential,υ_s and normalized bulk potential, υ_B, q is the electron charge, k is the Boltzman's constant, T is temperature, V_{GS} is the gate voltage applied, Q_s is the surface charge and C_{ox} is the oxide capacitance which is equal to $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.

$$y = \upsilon_s - \upsilon_B$$

$$\text{where } \upsilon_s = \phi_s \frac{q}{KT} \ , \upsilon_B = \phi_B \frac{q}{KT}$$

$$\text{and } \phi_B = \ln \frac{n_i}{N_A} \text{ for p-type substrates}$$

The capacitance-voltage curve for the device simulated is given in Figure 6.20.

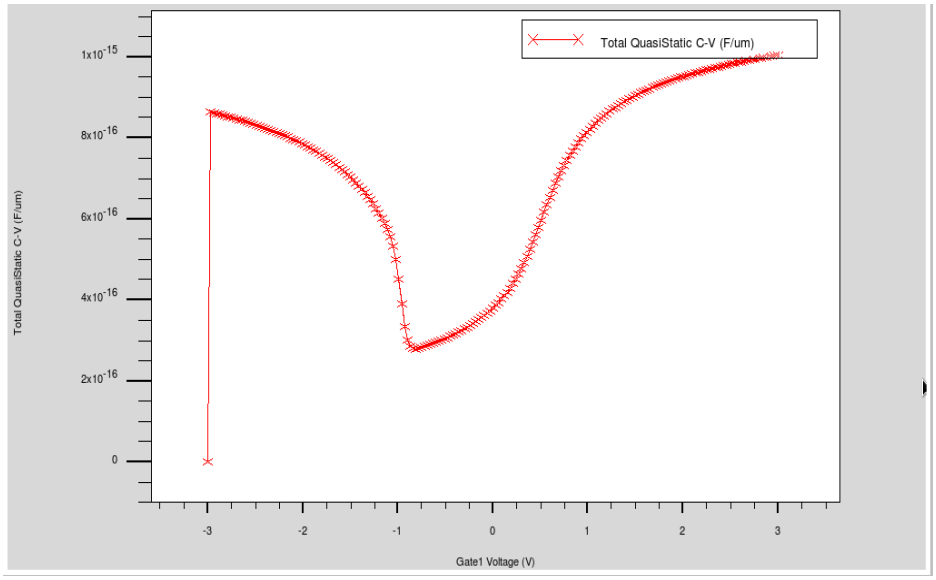


Figure 6.20 CV Characteristics of G-SOI with Al_2O_3 material

The Capacitance versus gate voltage characteristics showed in Figure 6.20 and Figure 6.21 show that the maximum capacitance is achieved by using high permittivity material i.e Al_2O_3 and Lanthanum Gadolinium Oxide ($LaGdO_3$) respectively. The total Quasistatic Capacitance achieved is $6x10^{-15}$F/µm.

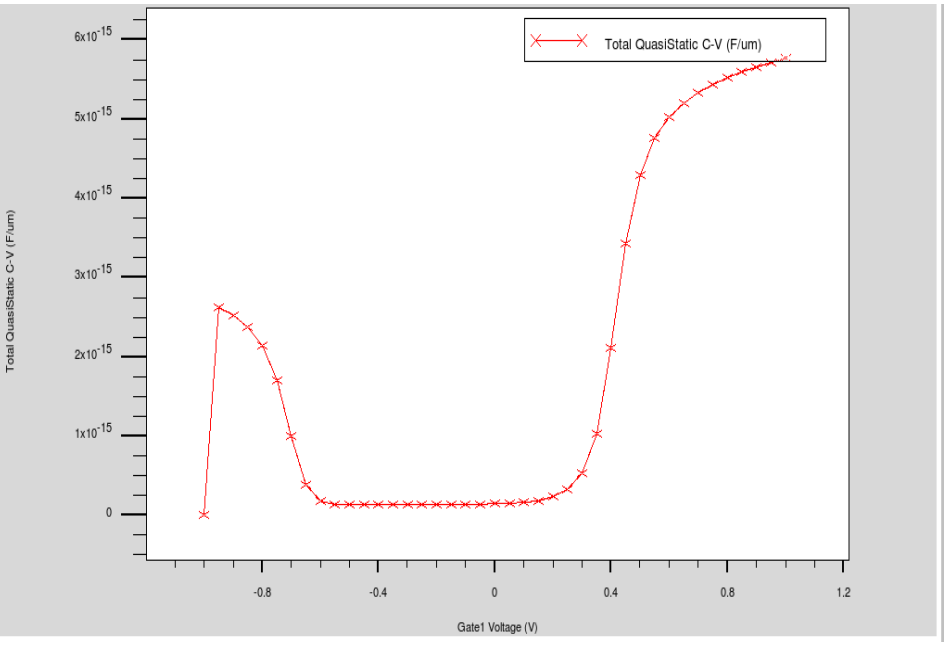


Figure 6.21 CV Characteristics of G-SOI with $LaGdO_3$ material

6.6 CONCLUSION

A Graphene-Silicon on insulator (G-SOI) is designed and simulated with graphene as a channel material in this research work. It is a majestic device that is highly appreciated in recent years by the electronic industry due to its high mobility and ON current. The simulations performed in the software are focused on the NEGF method to better analyse the device's different parameters. From the results of the simulation, it was observed that the G-SOI with hexagonal Boron Nitride as a substrate and $LaGdO_3$ as a gate oxide give higher trans-conductance, lower sub-threshold swing, lower off-current (Ioff) and higher off-current (I_{ON}/I_{OFF}) ratio. It also concludes that the improved device performs excellently in the context of ON/OFF current ratio, sub-threshold current and DIBL $6.11x10^{06}$, $7.44x10^{-10}$ A and 69mV/V respectively. This design's main motive is to achieve maximum ON/OFF ratio, lower sub-threshold current and DIBL for the best performance device.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSIONS

The main objective of this research work is to model and optimize a Silicon MOSFET suitable for low-power applications. The design and optimization depend strongly on the appropriate simulation of the physical behavior and electrical characteristics of the device. By analysing the characteristics of semiconductor devices using CMOS Technology Computer-Aided Design (TCAD) process, evaluation and enhancement of their essential parameters are performed. This research is aimed to explore the problems created by scaling of MOSFET dimensions and by using alternative techniques to deal with them. Different architectures and channel materials are listed in order to fix the problems in existing devices. Different methods to decrease the leakage current of the system are explored. Additional modifications are demonstrated in existing MOS structures such as halo doping, threshold voltage implant and work-function engineering to control leakage current of the MOSFET. Various channel materials such as Graphene are used to achieve a higher I_{ON}/I_{OFF} ratio. The major contributions of this research are as following:

- The constant scaling of the chip dimensions deteriorates the output of the MOSFET devices to different types of leakage currents and short channel effects (SCEs). In this research work, various techniques have been developed to minimize these short channel problems resulting from the downscaling of the device dimensions. An NMOS device is designed and fabricated using TCAD software having effective channel length and extractions of parameters are carried out to optimize the performance of the device.
- It has been observed that less sub-threshold leakage current, high ON/OFF ratio, less DIBL and less sub-threshold leakage is optimized by increasing the work-function of the gate electrode.
- The key element in this research work is to improve the performance of the MOS device by adjusting the device and process parameters i.e. gate oxide thickness, halo doping, threshold implant doping, Source/Drain doping, substrate doping, poly doping and work function. After the analysis, it has been observed that short

channel effects decreases and the characteristics of the device have been improved by increasing the threshold voltage.

- Lightly doped substrates are the best solution for enhancing the noise immunity of substrates and devices developed on lightly doped substrates have better drain characteristics than heavily doped substrates. In the case of the highly doped substrates, the substrate current is more prominent making it less appropriate for the device level design. For lightly doped devices off-state leakage current can also be minimized by increasing the work-function of the gate electrode. Such methods showed good results in reducing threshold voltage variance. The model reliability can be calculated from the performance characteristics of the device. The lightly doped substrate has improved characteristics such as ON current, threshold voltage, off-state current, substrate current, and sub-threshold slope compared to the highly doped substrates even at low gate oxide thickness.
- The best value of Polysilicon doping and Source/Drain doping concentration considered for the best performance device is $1.5x10^{15}$ cm^{-3} and $3.5x10^{15}cm^{-3}$ respectively. Based on extracted values, a comparison of Gaussian and Pearson is performed to analyze the best doping profile for MOS devices. It has been observed less OFF-state leakage current and high threshold voltage has been obtained in the Pearson Doping Profile as compared to Gaussian Doping Profile. But the drain current is more in the doping profile of Gaussian Doping Profile as compared to Pearson Doping Profile. NMOS device is modeled with different gate oxide thicknesses.
- PMOS device is designed and fabricated with the Gaussian Doping Profile. Halo-Implant Variation, Gate Oxide Thickness and Threshold Implant are varied to analyse the effect on parameters such as threshold voltage, drain current, leakage current and substrate current of the device.
- Low k materials are replaced with high k gate dielectrics having high permittivity to boost the performance of MOSFETs. A dual material SOI devices with single and dual halo doping are designed and simulated to obtain the best value of off-state leakage current. After the analysis, it concludes that the best performance is obtained by a combination of HfO_2 (high k material), metal gate and dual halo dual material device.

- A device called Graphene-Silicon on Insulator (G-SOI) is developed to mitigate these short channel effects arising from downscaling of chip dimensions. The high ON/OFF ratio and high ON current are achieved by using high mobility Graphene material. Graphene-Silicon on Insulator (G-SOI) is a glorious device that is highly appreciated in recent years by the electronic industry due to its high flexibility, mobility and ON current. G-SOI is presented in this research with different substrates and different oxide materials to achieve reduced leakage current, saturation slope and drain-induced barrier lowering (DIBL) with increased drain current. From the simulation results, it has been observed that the G-SOI with hexagonal Boron Nitride as a substrate and $LaGdO_3$ as a gate oxide gives higher ON current, lower sub-threshold current and higher I_{ON}/I_{OFF} ratio. The main motive of this design is to achieve maximum ON/OFF ratio, lower sub-threshold current and less DIBL for best performance device which is achieved by having such type of device.

7.2 SCOPE OF FUTURE WORK

The research work performed in this thesis has demonstrated the ability to reduce short channel effects and enhance device quality in Analog/RF applications and low power applications by choosing correct device dimensions with appropriate materials. It also describes the effect of working and high-k dielectric gate work-function on different device parameters. It is now possible to use the same framework to enhance the understanding of existing structures and to develop new structures for high-performance, low-power and high-speed applications that may be of interest to certain applications. It is hoped that the findings presented will provide opportunities for further research. The research can further be expanded:

- By the inclusion of other SCEs that are not considered such as GIDL, hot carrier effect and deterioration of mobility.
- By detailed optimization of device which can be used in communication applications.
- By fabrication of different device structures, Graphene can be a future material for multi-gate devices and Interconnects
- By further developing different techniques to increase the graphene material bandgap so that it can be used effectively in low-power circuits.

BRIEF PROFILE OF THE RESEARCH SCHOLAR

Nitin Sachdeva (nsymca81@gmail.com) received an M.Tech Degree in VLSI Design & CAD from Thapar Institute of Engineering & Technology, Patiala (Punjab) and B.Tech in Electronics and Communication Engineering from PTU, Jalandhar in 2005 and 2003 respectively. She is working as Assistant Professor in Electronics Engineering Department at J.C Bose University of Science & Technology, YMCA Faridabad from January 2007. She has supervised several M.Tech Thesis and Projects. She has also published many papers in various National & International Conferences/Journals. Her research interest is in the field of VLSI Design and also pursuing her Ph.D. in the field of VLSI Design.

LIST OF PUBLICATIONS

List of Published Papers

Sr. No.	Title of the Paper along with Volume, Issue No., Year of Publication	Publisher	Whether peer reviewed Yes/No	Whether Refereed Yes/No	Whether any amount paid for publication Yes/No	Indexed in
1.	Performance Investigation of dual-halo dual-dielectric Triple material Surrounding Gate MOSFET with high-k dielectrics for low power applications, Journal of Semi-conductor Technology and Science, Volume 20, No.3, pp. 297-304, ISSN No. 2233-4866, June 2020	IEIE, Korea	YES	YES	NO	SCIE
2.	Effect of variation of gate work-Function on electrical characteristics of lightly doped PMOSFET, International Journal of Future Generation Communication and Networking, Volume 12, No.4, pp.17-26, ISSN No. 2207-9645, 2019	Nadia Journal Publications	YES	YES	NO	ESCI
3.	Analytical Modeling & Simulation of off-state Leakage current for lightly doped MOSFETs, Journal of Nano- and electronic physics, Volume 9, No.6, pp.06009-(1-4), ISSN No. 2306-4277, 2017	Sumy State University (Sumy, Ukraine)	YES	YES	YES	SCOPUS

4.	Analytical 2D Modeling of Surface Potential and threshold voltage for Lightly doped substrate NMOS, International Journal of Recent Technology and Engineering, Volume 8, Issue 4, pp 12108-121111, ISSN No. 2277-3878, November 2019	Blue Eyes Intelligence Engineering and Sciences Publication	YES	YES	NO	SCOPUS
5.	Effect of Gate Work-function on Gate Induced Drain Leakage of MOSFETs, International Journal of Computational Engineering & Management, Volume 21, Issue 1, pp 11-16, ISSN No. 2230-7893, January 2018	IJCEM research foundation trust	YES	YES	NO	UGC APPROVED
6.	The Impact of Substrate Doping Concentration on Electrical Characteristics of 45nm NMOS device, Journal on Electronics Engineering, Volume 8, No.2, pp.20-26, ISSN no. 2249-0760, February 2018	i-manager Publications	YES	YES	NO	UGC APPROVED
7.	Effect of halo implant and threshold implant on sub-threshold current and substrate Current of MOSFET, Journal on Embedded Systems, Volume 6, No.1, pp.23-29, ISSN No. 2320-2335, 2017	i-manager Publications	YES	YES	NO	UGC APPROVED
8.	Reduction of Short Channel Effects with the Variation of Poly Doping and Source/Drain Doping, Journal of Semi-conductor Devices and Circuits, Volume 4, Issue 3, ISSN No. 2455-3379, pp-35-42, 2017	STM	YES	YES	NO	UGC APPROVED

9.	Effect of Various Parameters on Threshold Voltage of Virtually Fabricated Lightly Doped PMOS Device, Journal of VLSI Design Tools & Technology, Volume 7, Issue 3, pp-13-20, ISSN No. 2321–6492, 2017	STM	YES	YES	NO	UGC APPROVED
10.	Impact of various doping Distributions on N-MOSFET Performance, International Journal of Technology, Volume 8, Issue 1, pp.1-10, ISSN No. 2231-3915,2018	Knowledge and research publishers	YES	YES	NO	UGC APPROVED
11.	Analyzing the threshold voltage and sub-threshold slope of bulk and SOI MOSFET in SILVACO, Journal on Embedded Systems, i-manager Publications, Volume 5, No.4, pp.11-16, ISSN No. 2320-2335, 2017	i-manager Publications	YES	YES	NO	UGC APPROVED
12.	Design, Simulation &Optimization of 45nm NMOS Transistor, International Journal of Advanced Research in Computer and Comm. Engineering, Volume 5, Issue 1, pp.272-274, ISSN No. 2278-1021, 2016	IJARCCE	YES	YES	YES	GOOGLE SCHOLAR
13.	Impact of Various Parameters on Power Consumption of CMOS Logic Circuits, International Journal of Signal Processing, Image Processing and Pattern Recognition, Volume 10, No. 9, pp.31-42, 2207-970X, 2017	Nadia Journal Publications	YES	YES	NO	GOOGLE SCHOLAR

14.	Study the characteristics of 130nm NMOS transistor using SILVACO TCAD Tool, 2016	National Conference, RSTTMI, YMCAUST, Faridabad				
15.	NMOS Fabrication At 180nm Node and Study the Effect of Various Parameters on Threshold Voltage Using SILVACO TCAD Tool, 2016	National Conference, RSTTMI, YMCAUST, Faridabad				
16.	Optimization in fabricating 65nm NMOS Transistor using SILVACO Tool, 2016	International Conference, SDREM, YMCAUST, Faridabad				

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SUMMARY OF THESIS

on

MODELING, ESTIMATION AND REDUCTION OF TOTAL LEAKAGE IN SCALED CMOS LOGIC CIRCUITS

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CONTENTS

1. INTRODUCTION

Over the last few years, semiconductor manufacturing has done notable progress and primarily leading to fast advancement in integration techniques as well as the design of large-scale devices. As the integration level of the chip improves, there is more complication in manufacturing. The transistor size is switched from micrometer to nanometer. In 1947, the first transistor was invented at Bell Labs and the electronics sector is switched from electron tubes to solid-state electronic devices [28]. The development in solid-state electronics research in particular and semiconductor-based electronics trade began with the growth of bipolar transistors, which is found to be one of the most significant innovations in 20th century. This innovation of bipolar devices had an extraordinary effect on the growth of the science and technology of semiconductors at that time. The bipolar junction transistors (BJTs) are replaced by MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) in Digital Electronic Circuits [29]. MOSFET is a semiconductor device widely used for switching and amplifying electronic signals in electronic systems. MOSFET is a core of an integrated circuit that can be designed and produced in one chip due to its very tiny size. CMOS (Complementary Metal Oxide Field Effect Transistor) is a major component of digital and analog integration [24]. CMOS technology is the chosen technology for the construction of various integrated circuits i.e. microprocessors, microcontrollers, memory chips, sensors, data converters and various communication applications. The size of the device must be reduced to accommodate more number of transistors on a single chip. The scaling down of dimensions of the transistor results in different unexpected issues that degrade the efficiency of the device. The various short channel effects, leakage current issues and threshold voltage variation etc. occur due to the scaling issues [13].

Miniaturization with Very Large Scale Integration (VLSI) in the areas of multimedia communication, image processing and many broadband applications has been increasing at a very fast speed. It is a system of integration on a single silicon chip with millions of MOS transistors. When complexity increases exponentially, this contributes to ultra-large-scale (ULSI) implementation [31]. In 1965, Intel's co-founder, Gordon Moore reported that several transistors on a chip were doubled after every two years. [4]. He expected this trend of an increasing number of transistors to continue in the future also.

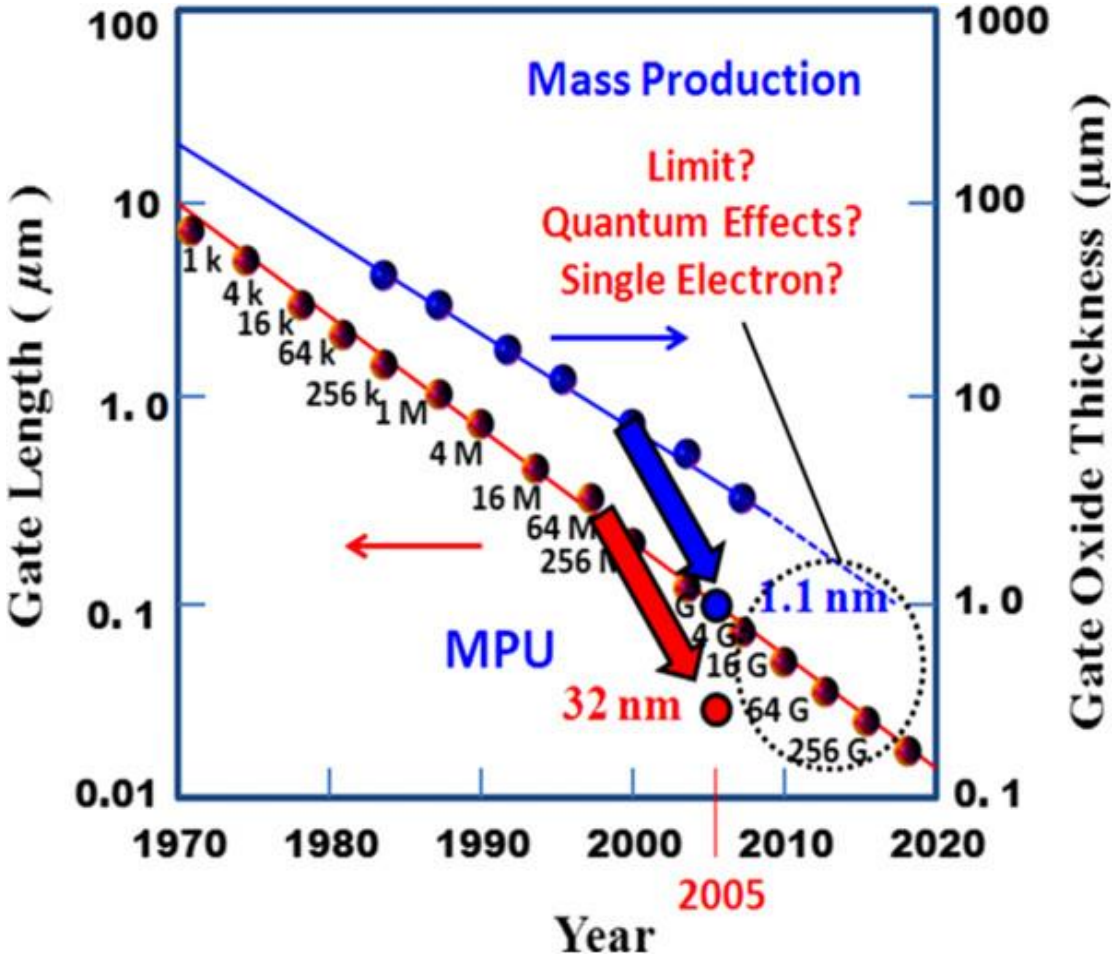

Figure 1 Technology Progress

Microelectronics production, automation, data sharing and signals processing over the past thirty years has been heavily dependent on the Very Large-Scale Integrated Circuit (VLSI) market. VLSI technology is credited with high-speed, ultra-small, low-power semiconductor chips, sensors and advanced materials. In 1960, Kahng and Atilla conducted the first practical exhibition on MOSFETs based on Silicon. MOSFET is a semiconductor device broadly used in electronic devices for switching and amplifying electronic signals. It is a component of an integrated circuit which can be built and assembled in one chip due to its short dimensions.

Scaling is defined as a managed change in physical and electrical properties resulting in a decreased chip area while maintaining the characteristics of the device. It is often referred to as reducing the size i.e. MOSFET dimensions. MOS transistor scaling requires the systematic decrease of the overall dimensions of the device as allowed by the existing

technology while maintaining the geometric ratios found in the larger devices. The scaling results in varying device parameters such as threshold voltage, gate oxide thickness, channel size and width [27].

Fabricating MOSFETs with much shorter channel lengths is a major issue nowadays and the problems of manufacturing semiconductor devices are always a notification sign in developing integrated circuit production. Over the past few years, the small dimensions of the MOSFET have developed operational disorders under a few tens of nanometers. The gate oxide thickness must be decreased to preserve the supply voltage and threshold voltage resulting in gate leakage current. Due to the scaling of MOS devices, many short channel effects such as Drain Induced Barrier Lowering (DIBL), Sub-threshold Leakage, Punch-Through, Hot-Electron Effect and Dielectric Breakdown occurs. The aim of this research is to investigate the issues caused by scaling the dimensions of MOSFET and applying alternative methods to manage them. Various architectures, channel materials and modified structures are suggested to solve the issues in existing devices. Different techniques are explored to reduce the leakage current of the device. Additional changes in the existing MOS structures such as Halo doping, threshold voltage implant and work-function engineering [30] are illustrated to control the sub-threshold leakage current and DIBL. Various channel materials such as Graphene is utilized during virtual fabrication of the device to get a higher I_{ON}/I_{OFF} ratio.

2. LITERATURE REVIEW

Moore's Law and the ITRS have been complimenting each other since the first edition of the roadmap in the early 90s. High leakage current in deep-sub-micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced. The Closed-form 2D Modeling of MOSFETs deep-submicron and sub-100 nm is explored using a conformal mapping method where the 2D Poisson Equation is partitioned into a 1D long-channel situation and 2D Laplace Equation in the depletion regions [2]. One of the issues with the scaling of classical MOSFETs to the sub-100 nm range is that the density of the substrate doping must be increased to 10^{18} cm^{-3} in order to include the source and drain depletion layers. However, high doping has several negative effects on the MOSFET properties such

as channel mobility degradation and excessive threshold voltages. One alternative is to use a much lower doping substrate and instead ion implants a higher doping concentration under the surface. A thin layer of lower concentration of doping persists on the surface after annealing usually at a depth of less than 100nm. The much higher doping required avoiding extreme short-channel effects and punch-through extends into the substrate for another 100nm or so. This approach applies to both Classical and Non-Classical MOSFETs. The electrical features of the submicron system were investigated. The following parameters have been applied for constant field scaling: active channel size, ion implantation threshold voltage (V_{th}) and gate oxide thickness (t_{ox}). Other approaches used in submicron systems to avoid short channel effects included shallow trench isolation (STI), deposition of sidewall spacers, implantation of lightly doped drain (LDD), and well-implantation retrograde. The findings indicate that well retrograde implantation permitted the highest density of the dopant to drop below the surface of the substrate [3]. A lightly doped region was formed with the implementation of sidewall spacer and LDD implantation beyond the n^+ drain/source junction. Drain Current (I_D) has also risen as the metallization layers rise. The effects of variable channel size, gate insulator thickness (SiO_2), gate insulator content and temperature were analysed using computational simulations. Clearly, these simulation findings show that the carbon Nano-tube MOSFETs is the best candidate for use in high-speed switching applications for optimum system parameters than the MOSFET [8].

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was the cornerstone of the development of Nano-electronics technology [15]. The scaling down of planar bulk MOSFET implied by Moore's Law was saturated due to short channel effects and DIBL. Due to this alternative approach, problem-solving was considered with reduced node technology [32]. SOI technology has contributed to a revolution in the scaling of transistors and more volumes of packaging in the same space. The invariability of early voltage and intrinsic gain from drain-bulk connected NMOS and PMOS transistors was controlled in weak inversion [16]. It has been shown in a wide range of geometry and bias conditions for both measured and TCAD simulated systems. Early voltage and undeniable increase are given in weak-moderate inversion, which shows that these quantities are dominated by the impact of the substrate and are insensitive to bias and geometry. Several issues and

approaches have also addressed the issue of quantum mechanical effects in MOSFET modeling. Therefore, it can be found that in all areas of its operation there is a powerful need for an analytical model that correctly describes the nanometer-sized MOSFET behavior. The electrical properties studied were the threshold voltage (V_{th}) and the current level (I_{max}). The investigation approach was performed by measuring the concentration of boron doping in polysilicon doping, adjusting impurities in polysilicon doping and also increasing the concentration of arsenic doping in source/drain annealing [18]. The doping concentration was correctly varied to obtain the ideal property of the transistor. SILVACO TCAD tools were used to obtain electrical characteristics of the NMOS device. A 90 nm NMOS has been designed and manufactured to test its electrical performance. SILVACO's ATHENA and ATLAS modules were the tools used to visualize the NMOS transistor electrical characteristics. The primary parameter analysed was the value of threshold voltage (V_{th}) which defines whether or not a transistor is operating [19].

The ATLAS simulator simulates the electrical characterization of the 65 nm NMOS transistor structure and then compares it with the reported observational results. The simulated threshold voltage was found to be 0.2V, which correlates well to the experimental value. Furthermore, there are various short channel effects such as punch-through, velocity saturation, and hot electron generation. The parameters include HALO implantation, S/D implantation, compensation implantation, SiO_2 thickness, V_{th} adjustment implant, poly-silicon thickness and silicon annealing time [21]. The experimental development of Taguchi Technique determined system parameters. Threshold voltage (V_{th}) is taken as marginal, the best effects of different variables on the S/N ratio and modification parameter Compensation Implant for NMOS threshold voltage (V_{th}) are considered because this has a large effect on the mean threshold voltage (V_{th}) but almost no effect on threshold voltage deviation (V_{th}). This study demonstrates that Taguchi Analysis can be used efficiently in the development of CMOS devices to find the ideal approach. To find a functioning transistor with threshold voltage and leakage current within the estimation of International Technology Roadmap for Semiconductors (ITRS) at this technology stage in the process. The key finding in this work is that "V_{th} adjust Implant" cannot surprisingly be used as a V_{th} modification parameter but "Compensation implant" can be used to adjust V_{th} to its target value of 0.110 V [22]. Device-level noise in the

development of a sub-micron can cause serious problems with circuit incorporation. With lightly and heavily doped substrates, MOS devices are virtually developed and the substrate current is accessed for these devices. Lightly doped substrates increase noise tolerance compared to heavily doped substrates. With the aid of ATLAS, simulation of the substrate conduct is undertaken at 45 nm engineering node device for PMOS and NMOS. Substrate current is calculated for PMOS and NMOS applications for heavily or lightly doped substrates. In the case of highly doped substrates, the substrate current is more intense making it less appropriate at the stage of the device. The substrate current in lightly doped substrate devices is less as compared to heavily doped devices. The lightly doped substrate devices, therefore, have greater resistance to substrate noise and devices built on lightly doped substrates have better drain properties than heavily doped substrate devices. Basically, a comparison of heavily doped and lightly doped substrates is done here [25]. To extract threshold voltage of MOSFET based on the widely used Constant Current Method for calculating, defining and observing the threshold voltage. Using predictive models, the threshold voltage is evaluated and simulated. This approach allows for faster development of reliable analog circuits in state-of-the-art CMOS technologies where voltage ranges are significantly small and only predictive models are active during design. In view of the necessarily limited gate overdrives in low-voltage analog architecture and the widespread use of predictive models for faster time on the market [26][17].

Silicide was used on the interface of the poly-Si gate to reduce the resistance of the electrode gate. NMOS device was basically manufactured using the ATHENA module. By using the ATLAS module, the electrical characterization of the device was implemented [22] [27]. The resistance of the poly-silicon layer should also be maintained as small as possible to improve the system speed by reducing the time for a transistor to turn on to accumulate charge in the channel Taguchi method is used to predict the optimal solution to achieve the desired transistor efficiently. This high-k material has been developed as a forthcoming high-k candidate by examining the temperature and frequency-dependent dielectric structures. Analysis of extremely-thin sheet-based $LaGdO_3$ planar condenser structures demonstrated the validity of this new material for next-generation radio frequency, analog/mixed-signal and adaptive random access memory systems. In conclusion, this detailed work indicates that $LaGdO_3$ poses the best solution high-k

material constraints, so this latest, high-potential material for digital devices has been shown as a dielectric gate [35].

3. MOTIVATION OF RESEARCH

Integrated circuits (IC) technology has undergone immense technical and economic progress. The main engine powering the electronics journey is "miniaturization." It is becoming a massive challenge in increasing speed and density in the semiconductors industry since the invention of the first calculation devices. Optimizing MOSFETs is a challenging job for digital and analog circuits due to contradictory device performance needs. In logic applications where trade-off is governed by the I_{ON} / I_{OFF} ratio, the task is to minimize OFF current while reducing intrinsic delay and maintaining high ON current. Cutting speed, intrinsic gain, linearity, noise and device mismatches are the performance metric for RF and analog circuits. The gate length was one of the most critical parameters directly related to CMOS scaling. When MOSFET devices are miniaturized, several complications results. As the length of the channel decreases, several effects alter the quality of MOSFET devices. The short channel effects like mobility degradation, DIBL, hot carrier effect, velocity saturation, channel length modulation, Punch-through and reduction of threshold voltage occurs due to scaling process. The presence of these effects in existing devices due to scaling in MOSFETs is the motivating factor to do research work to reduce these types of effects so that performance due to miniaturization is not degraded. The motive of this research work is to develop various techniques to enhance the performance of the device.

4. OBJECTIVES

The following are objectives of the research work:

- To study and perform the virtual fabrication of Nano-Scale devices.
- To analyse the impact of various design parameters such as gate oxide thickness, halo doping, threshold implant concentration, substrate doping, source/drain doping on the performance of the device.
- To analyse the extraction of various parameters such as Sub-threshold leakage current, drain current, Substrate current, ON current, ON/OFF ratio, device capacitance, etc. of MOSFET using various doping profiles.
- To investigate the effect of the work-function of gate material on device performance.
- To design and simulate an SOI device with high k oxide material and metal gate.
- To design & simulate Graphene-based Transistor

The whole proposed work related to modeling, analysis & simulation has been done using SILVACO TCAD & various other tools.

5. REMEDIES TO SCALING PROBLEMS

The remedies to scaling problems are:

- The scaling of gate oxide thickness along with channel length of MOS transistors gives rise to an increase in undesired gate leakage current [23]. To avoid this type of leakage high-k materials are recommended to replace low k materials as a gate oxide material. High-k dielectric gate thickness affects threshold voltage (V_{th}) and off-state leakage current (I_{OFF}).A device with high drive current (I_{ON}) and low I_{OFF} results in a high ON-OFF current ratio (I_{ON}/I_{OFF}) resulting in faster switching speeds for the N-type Metal Oxide Semiconductor Field Effect Transistor (NMOS).
- For devices in the nanometer scale, the metal gate electrodes are chosen over poly-silicon. The benefits of metal gate electrode over poly-silicon gates are reduced gate resistance and desirable function setting. For compatibility with standard high-temperature CMOS processing, thermally stable metal electrodes are needed.
- Integrated circuit chips have different fabrication steps from crystal growth to metallization of the device. Different patterns are created and different layers are

placed upon each other having insulating layers between them. Every layer is deposited or diffused on the surface of the wafer having defined temperature, time and doping concentration [18]. There are various parameters at different steps that can be altered during fabrication to enhance the performance of the device. Various implants i.e halo implant, threshold voltage implant, Source/Drain implant, substrate doping can be incorporated into the device to reduce short channel effects.

- Changes in processing techniques and the introduction of new materials and device architectures have resolved many of the difficulties in the device concentrations. Silicon on Insulator (SOI) is one of those architectures that IBM launched [9]. It is predicted that by decreasing power consumption and enhancing the device's transient response, the substrate current can be reduced [10].SOI is further used as a base device for multi-gate transistors and Graphene based transistors to reduce the short channel effects. Scaling of conventional bulk MOSFETs has been done continuously until 2018 to endure Moore's Law. Due to the scaling of conventional transistors, several short channel effects arise resulting in degradation of the device's performance. It is very necessary to find out an alternative to reduce short channel effects for enhancement of the device. According to ITRS, 2004 first consideration is transport enhanced FETs which improves the carrier mobility and current drive. The second consideration is to have ultra-thin body SOI (UTB SOI) FETs. The third consideration is source/drain engineering FETs and the last consideration is multiple gate FETs. The research of ultra-thin body (UTB) SOI MOSFETs [7] has increased the chance of replacing the conventional MOSFETs at 45 nm technology node and beyond. UTB SOI is the extension of FDSOI. In addition, the halo doping in the channel region of the SOI device provides tremendous device performance. Graphene material is preferred nowadays to be used as a channel material [6]. A Graphene-Silicon on Insulator (G-SOI) is a device that has lightly doped graphene channel between source and drain. It is a majestic device that is very much appraised by electronic industries these days because of its higher mobility and ON current. Here the G-SOI is presented with various substrates and different oxide materials to acquire the reduced leakage current, saturation slope and Drain Induced Barrier Lowering (DIBL) with enhanced drain

current. The performance of the device depends upon various parameters i.e. contact doping, gate insulator dielectric constant, graphene film thickness, oxide thickness, etc. The most demanding approach used to model carrier transport in nanoscale FETs is non-equilibrium Green's Function approach (NEGF) which is based on solving Schrödinger Equation under non-equilibrium conditions [33] [34]. The choice of a suitable gate dielectric constant is important in determining device performance. The comparative analysis after computational simulations results showed that G-SOI provides much better I_{ON}/I_{OFF} ratio than conventional SOI devices [20] [5]. There can be millions of transistors on a tiny piece of silicon in a modern-day IC. Of course, without computer aids, the manufacture and design of these ICs cannot be performed. Electronic Design Automation (EDA) tools involve both the manufacture and design of these ICs. Highly accurate software tools are needed to analyze and simulate embedded circuit design and manufacturing. Lots of research have been performed on these problems and are still going on [11]. The whole work is done to accomplish this research work is performed in SILVACO TCAD Tool. ATHENA offers a platform for the simulation of ion implantation, diffusion, etching, deposition, lithography, and oxidation of semiconductor materials ATLAS simulates semiconductor electrical, optical and thermal behavior [12].

6. RESEARCH METHODOLOGY

The purposed work is done by using ATHENA and ATLAS SILVACO software as shown in the flow diagram given below. The Design, fabrication and comparative analysis of various devices have been done to improve the performance metrics of the device.

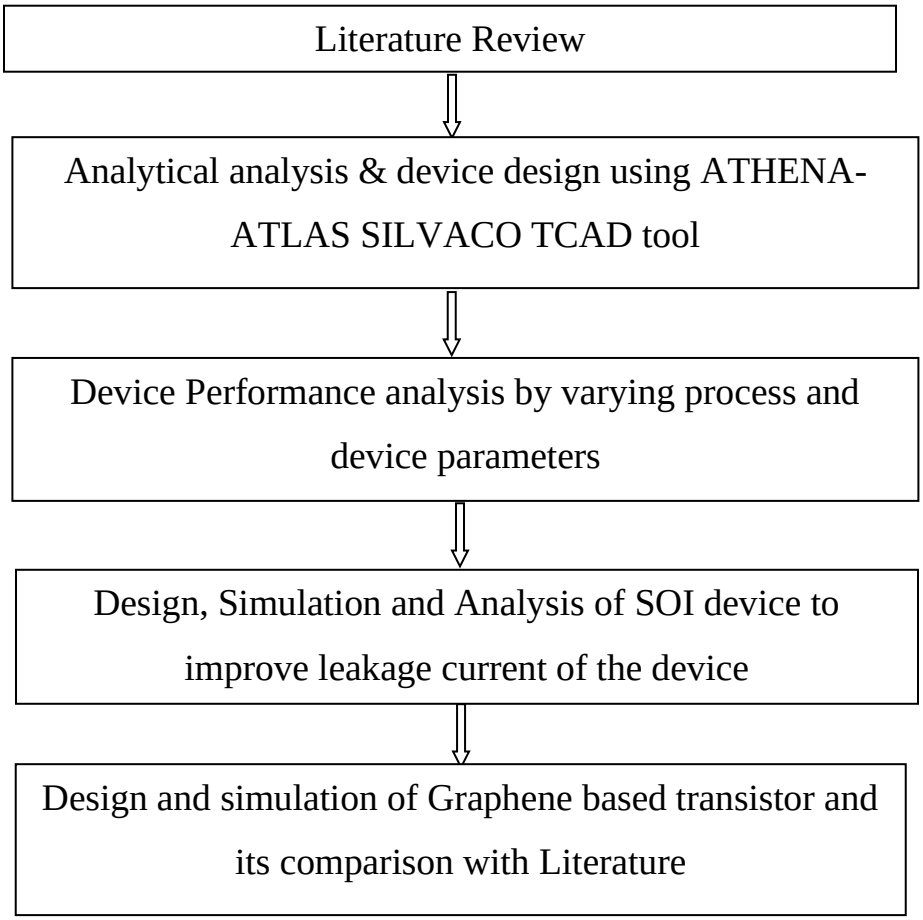

Figure 2. Flow diagram for Research Methodology adopted

7. THESIS ORGANIZATION

This thesis is organized into seven chapters. The detailed view of all the chapters is given below:

Chapter 1 Introduction

A detailed review of existing devices on various technologies and their related parameters is presented. The solutions to various problems beyond the 50nm channel lengths are explored. The main motive is to formulate the problem in existing devices concentrating on drain current, off-state leakage current, sub-threshold slope and substrate current of the device. In this chapter, the objectives of the thesis are also discussed.

Chapter 2 Literature Review

This Chapter provides a survey of existing MOSFET scaling and short-channel effects research and present problems. This chapter along with the scaling theory also describes the physics behind the issue. The main sources of variation will then be discussed outlining their impacts on device and circuit efficiency. It presents the conventional existing MOSFET structures, enhancement techniques and recent trends to enhance the performance of the device.

Chapter 3 Modeling and Simulation Methodology

Running real experiments in semiconductor fabrication Labs is both time-consuming and expensive. The use of TCAD tools reduce the development cost and shorten the development time. It is often more cost-effective and time-efficient to substitute simulated experiments for some of the real-world experiments. The device is initially designed and virtually fabricated using SILVACO ATHENA and ATLAS tools. The mathematical expression of surface potential and the threshold voltage is also being derived.

Chapter 4 Electrical Characteristics of Novel Silicon MOSFET

This chapter describes the design, simulation and analysis of NMOS and PMOS devices based on various extracted or simulated parameters. Initially, NMOS and PMOS devices have been designed, virtually fabricated and simulated. Various device design parameters

(threshold voltage, drain current, sub-threshold current, substrate current, linear threshold voltage, and DIBL) have been extracted and reported in this chapter. Further, the device with the variation in substrate doping is designed. Two devices have been designed with lightly doped and heavily doped substrates and the comparison of both the devices has been done. The analysis of the device with Gaussian and Pearson Doping Profiles has been reported in this chapter.

Chapter 5 Performance Analysis of the SOI MOSFET

The persistent scaling of MOSFET dimensions worsens the performance of the device and allows the innovation of new devices such as Silicon-on-Insulator (SOI) with modified structures. In this chapter, the surface potential of dual material SOI MOSFET is analytical estimated and compared with the simulated results. Also, the dual-material single halo and dual-material dual halo structures are being designed & simulated to reduce the device's leakage current.

Chapter 6 Characterization of G-SOI MOSFET

An NMOS device with a channel length equals to 10nm has been designed. Initially, 10nm G-SOI was designed using the silicon channel. Then the Silicon material in the channel is replaced with Graphene which gives a high ON current. Further, the SiO_2 substrate is replaced with h-BN material which gives high ON current as well as low leakage current as compared with other devices. Finally, a new high k material $LaGdO_3$ is introduced here to enhance the performance of the device.

Chapter 7 Conclusion and Future Scope

This chapter gives the conclusion and future scope of the work done

8. CONCLUSIONS

The main objective of this work is to model and optimize a Silicon MOSFET suitable for low-power applications. The design and optimization depend strongly on the appropriate simulation of the physical behavior and electrical characteristics of the device. By analyzing the characteristics of semiconductor devices using CMOS Technology Computer-Aided Design (TCAD) process, evaluation and enhancement of their essential parameters are performed. This research is aimed at exploring the problems created by scaling MOSFET sizes and using alternative techniques to deal with them. Different architectures and channel materials are listed in order to fix the problems in existing systems. Different methods to decrease the leakage current of the system are explored. The key element in this research work is to improve the performance of the MOS device by adjusting the device and process parameters i.e. gate oxide thickness, halo doping, threshold implant doping, Source/Drain doping, substrate doping, poly doping and work function etc. After the analysis, it has been observed that short channel effects decreases and the characteristics of the device have been improved by increasing the threshold voltage. The lightly doped substrate are preferred due to its improved characteristics such as ON current, threshold voltage, OFF-state current , substrate current, and sub-threshold slope compared to the highly doped substrates even at low gate oxide thickness. It has been observed less OFF-state leakage current and high threshold voltage has been obtained in the Pearson Doping Profile as compared to Gaussian Doping Profile. Low k materials are replaced with high k gate dielectrics with high permittivity to boost the performance of the device. A dual material SOI devices with single and dual halo doping are designed and simulated to obtain the best value of off-state leakage current. After the analysis, it concludes that the best performance is obtained by a combination of HfO2 (high k material), metal gate and dual halo dual material device. Various channel materials such as Graphene are used to achieve a higher Ion/Ioff ratio.

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10. LIST OF PUBLICATIONS

Sr. No.	Title of the Paper along with Volume, Issue No., Year of Publication	Publisher	Whether peer reviewed Yes/No	Whether Refereed Yes/No	Whether any amount paid for publication Yes/No	Indexed in
1.	Performance Investigation of dual-halo dual-dielectric Triple material Surrounding Gate MOSFET with high-k dielectrics for low power applications, Journal of Semi-conductor Technology and Science, Volume 20, No.3, pp. 297-304, ISSN No. 2233-4866, June 2020	IEIE, Korea	YES	YES	NO	SCIE
2.	Effect of variation of gate work-Function on electrical characteristics of lightly doped PMOSFET, International Journal of Future Generation Communication and Networking, Volume 12, No.4, pp.17-26, ISSN No. 2207-9645, 2019	Nadia Journal Publications	YES	YES	NO	ESCI
3.	Analytical Modeling & Simulation of off-state Leakage current for lightly doped MOSFETs, Journal of Nano- and electronic physics, Volume 9, No.6, pp.06009-(1-4), ISSN No. 2306-4277, 2017	Sumy State University (Sumy, Ukraine)	YES	YES	YES	SCOPUS

4.	Analytical 2D Modeling of Surface Potential and threshold voltage for Lightly doped substrate NMOS, International Journal of Recent Technology and Engineering, Volume 8, Issue 4, pp 12108-121111, ISSN No. 2277-3878, November 2019	*Blue Eyes Intelligence Engineering and Sciences Publication*	YES	YES	NO	SCOPUS
5.	Effect of Gate Work-function on Gate Induced Drain Leakage of MOSFETs, International Journal of Computational Engineering & Management, Volume 21, Issue 1, pp 11-16, ISSN No. 2230-7893, January 2018	IJCEM research foundation trust	YES	YES	NO	UGC APPROVED
6.	The Impact of Substrate Doping Concentration on Electrical Characteristics of 45nm NMOS device, Journal on Electronics Engineering, Volume 8, No.2, pp.20-26, ISSN no. 2249-0760, February 2018	i-manager Publications	YES	YES	NO	UGC APPROVED
7.	Effect of halo implant and threshold implant on sub-threshold current and substrate Current of MOSFET, Journal on Embedded Systems, Volume 6, No.1, pp.23-29, ISSN No. 2320-2335, 2017	i-manager Publications	YES	YES	NO	UGC APPROVED
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12.	Design, Simulation &Optimization of 45nm NMOS Transistor, International Journal of Advanced Research in Computer and Comm. Engineering, Volume 5, Issue	IJARCCE	YES	YES	YES	GOOGLE SCHOLAR

	1, pp.272-274, ISSN No. 2278-1021, 2016					
13.	Impact of Various Parameters on Power Consumption of CMOS Logic Circuits, International Journal of Signal Processing, Image Processing and Pattern Recognition, Volume 10, No. 9, pp.31-42, 2207-970X, 2017	Nadia Journal Publications	YES	YES	NO	GOOGLE SCHOLAR
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15.	NMOS Fabrication At 180nm Node and Study the Effect of Various Parameters on Threshold Voltage Using SILVACO TCAD Tool, 2016	National Conference, RSTTMI, YMCAUST, Faridabad				
16.	Optimization in fabricating 65nm NMOS Transistor using SILVACO Tool, 2016	International Conference, SDREM, YMCAUST, Faridabad				