Exam Roll No. _____

YMCA University of Science and Technology, Faridabad

M.Tech (ECE) III -Semester

Subject Name: Electronics System Design (Code: E16C-701)

Time: 03 Hrs M. Marks: 60

Note:- (i) Question No. 1 (Part-A) is Compulsory.
(ii) Answer any four questions from Part-B in detail.

	Part A (Compulsory Question) (2*10=20 Marks)	
Q1:	(a) Mention various applications of a multiplexer.	(2)
	(b) Compare in brief the features of MSI and LSI circuits.	(2)
	(c) What is the need of sequential circuits?	(2)
	(d) Mention the architectural differences between combinational and sequential circuits.	(2)
	(e) What do you understand by clock skew?	(2)
	(f) Mention various applications of PLAs.	(2)
	(g) What is the significance of asynchronous circuits?	(2)
	(h) What are the characteristics of essential hazards?	(2)
	(i) Draw the general structure of CPLD.	(2)
	(j) Compare the features of synchronous and asynchronous sequential circuits.	(2)
	Part B (4*10=40 Marks)	
Q2:	(a) With the help of block diagram and K-maps, present the design of a two-bit comparator. (b) With the help of relevant diagrams, design a 4-to-1 multiplexer.	(5) (5)
Q3:	(a) Describe in detail the schematic diagram for a Tristate buffer. (b) Design a clocked S-R flip flop as prescribed by its characteristic table.	(5) (5)
Q4:	(a) Convert S-R flip flop to a D-latch using conversion table and K-map. (b) Design a self –correcting 3-bit twisted ring counter using JK flip-flops (assume relevant values).	(5) (5)
Q5:	Explain in detail the following with reference to MDS diagram generation: (i) MDS Symbology (ii) MDS diagram constructs Also develop a seven state MDS diagram for the prototype pop machine system controller.	(10)
Q6:	Write detailed notes on the following: (a) FPGA (b) Hazards	(5) (5)
Q7:	(a) Explain in detail the block diagram model of a general asynchronous finite state machine. (b) Design a binary toggle circuit that changes state with each rising edge of the clock input (assume relevant parameters if required).	(5) (5)