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Total Pages : 4

**221301**

May 2019

M.Tech. (ECE) III Semester (Reappear)

**ELECTRONIC SYSTEM DESIGN**

**(E16C-701)**

Time : 3 Hours]

[Max. Marks : 75

*Instructions :*

- (i) *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
- (ii) *Answer any four questions from Part-B in detail.*
- (iii) *Different sub-parts of a question are to be attempted adjacent to each other.*

**PART-A**

1. (a) Simplify :  $X = (B + \bar{C})(\bar{B} + C) \overline{(\bar{A} + B + \bar{C})}$ . (1.5) CO1
- (b) What is priority encoder? (1.5) CO2
- (c) Mention any *two* differences between edge triggering and level triggering. (1.5) CO3

- (d) What are different types of Hazards? (1.5) CO5
- (e) What is a state table? (1.5) CO4
- (f) What are the advantages of static RAM and Dynamic RAM? (1.5) CO4
- (g) Design a full adder circuit using gates. (1.5) CO2
- (h) Realize a SR flip-flop using NAND gates. (1.5) CO1
- (i) Define a bus. (1.5) CO2
- (j) Define cycle and races. (1.5) CO5

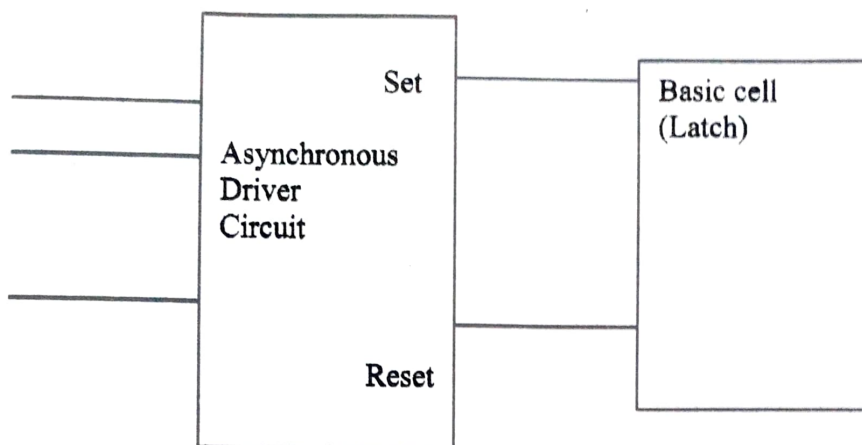
### PART-B

- 2. (a) Design a gray to binary code converter using PLA. (10) CO1
- (b) Convert a D FF to SR FF. (5) CO3
- 3. (a) If an eight stage ripple counter is to be designed using flip-flop with worst case transition times =  $25n$  sec, what is maximum input frequency at which this counter will operate. (5) CO3
- (b) Implement the following Boolean expression using 8 : 1 multiplexer.  

$$F(A, B, C, D) = \sum m(1, 3, 5, 10, 11, 13, 14) + d(0, 2).$$
(10) CO2

- 4. Design a system controller for 2's complement system which will start up and load a 74198 on the command (START), then successively shift these bits out and serially replace the original words with its 2's complement. When the process is completed, the DONE signal is to be asserted and held asserted until the next START is received and recognized, at which time it is to be deasserted. (15) CO4
- 5. (a) Explain in detail the wired logic and Bus oriented structures. (5) CO2
- (b) Explain the designing of system controller using Multiplexers. (10) CO4
- 6. (a) Design a circuit that is used to control the code on the outputs Z and W based on the position of control switch (CS). The control is prescribed as follows : when the switch is in UP position (CSUP(L) ASSERTED) the ZW code equals 00. When the circuit senses that switch has been moved to down position (CSUP(L) NOT-ASSERTED), the output is to sequence, with the rising edge of the CLK, from ZW= 00 to ZW = 01 to ZW = 11 to ZW = 10 and then stop and hold until the switch is moved back to the up position once more, at which time the ZW code reverts to ZW = 00. (10) CO3
- (b) Realize the EX-OR Gate with the help of four NAND gates only. (5) CO1

7. Design an edge-triggered D Flip-Flop based on the model shown in fig and SET/RESET operation of the basic cell.



(15) CO5

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