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May, 2019

M.Tech. (ECE) - II SEMESTER (Reappear)

VLSI Design (E16-C 608-A)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) Explain the role of transconductance in the operation of a MOS transistor. (1.5)

   (b) How does body effect influences the threshold voltage of a MOS transistor? (1.5)

   (c) Compare the sources of power dissipation between static CMOS and dynamic CMOS circuits. (1.5)

   (d) Give a tabular comparison between dry and wet etching. (1.5)

   (e) Why scaling is required and derive the scaling factor for gate capacitance. (1.5)

(f) Why is it necessary to have swing restoration logic in pass transistor logic circuits? (1.5)

(g) What are the various ways to reduce the delay time of a CMOS inverter? (1.5)

(h) Discuss the various architectural issues in VLSI. (1.5)

(i) In CMOS technology, why do we design the size of PMOS to be higher than that of NMOS? (1.5)

(j) Among energy and power dissipation of VLSI circuits, which one is more important for portable systems. (1.5)

PART–B

2. (a) Consider a MOS system with t_{OX} = 200 Å, ϕ_{GC} = – 0.85 V, $N_A = 2*10^{15}$ cm^{-3}, $Q_{OX} = q*2*10^{11}$ C/cm^3. Determine the threshold voltage under zero bias at room temperature. (7)

(b) Discuss the basic processes involved in fabricating CMOS using planar technology with the help of diagram. (8)

3. (a) Give the schematic diagram of a Bi-CMOS inverter. Explain its operation. Compare the switching characteristics of a Bi-CMOS inverter with respect to that for static CMOS for different fan out conditions. (10)

(b) Explain the accumulation, depletion and inversion conditions for a MOSFET with the help of energy band diagrams. (5)

4. (a) What is sheet resistance. Find out the expression of the resistance of rectangular sheet in terms of sheet resistance. (7)

(b) As you move to a new process technology with a scaling factor S = 1.4, how the drain current, power density, delay and energy requirement changes for the constant field scaling? (8)

5. (a) Design a stick diagram for $Y = \overline{A + \bar{B}C}$. (7)

(b) Design and implement a CMOS logic circuit that realizes the function of 2 bit comparator. (8)

6. (a) What is the latch up problem that arises in bulk CMOS technology? How it can overcome? (8)

(b) Explain the various sources of leakage current. (7)

7. Compare the area, in terms of the number of transistors, for the three different implementations of a full adder using (i) static CMOS, (ii) domino CMOS, and (iii) complementary pass transistor logic (CPL). (15)