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December, 2019

M.Tech. (Power Systems)-I SEMESTER

Pulse Width Modulation for PE Converters (MPS 110A)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Assume any missing data.*

PART - A

1. (a) What is pulse width modulation control of converters? (1.5)

   (b) What is modulation index? (1.5)

   (c) What is sinusoidal PWM? (1.5)

   (d) How is the output voltage of a sinusoidal PWM control converter varied? (1.5)

(e) What is a four quadrant converter? (1.5)

(f) What is the effect of chopping frequency on the load ripple current? (1.5)

(g) What is the purpose of overmodulation? (1.5)

(h) What is third-harmonic PWM? (1.5)

(i) What are the reasons for adding a filter on the inverter output? (1.5)

(j) What are the types of multilevel inverters? (1.5)

PART - B

2. (a) Explain the principle of pulse width modulation with the help of waveforms. (8)

(b) Comment on the harmonics in three-phase PWM inverters. (7)

3. (a) The three-phase, six step inverter has a star connected load with R = 8Ω and L = 2 mH. The inverter frequency is 50 Hz and the dc input voltage E is 200 V. (i) Derive the expression for i(t) as a Fourier series. (ii) Determine the RMS phase voltage at fundamental frequency and RMS line current. (10)

(b) What are the advantages and disadvantages of PWM Inverters? (5)

4. (a) Compare and contrast the features of square wave and sine wave PWMs. (7)

(b) Explain the technique of reduction of low order harmonics using PWM. (8)

5. (a) Explain how the voltage control of a three phase VSI is achieved (i) by controlling the dc link voltage (ii) by using multiple inverters, and (iii) by using pulse width modulation. (10)

(b) How is constant torque operation achieved with a PWM inverter? (5)

6. (a) How many SPDT switches are needed for a three and four level inverter? Explain. (6)

(b) The holding current of thyristors in the single phase full converter is I_H = 500 mA and the delay time is t_d = 1.5 μs. The converter is supplied from a 120 V, 60 Hz supply and has a load of L = 10 mH and R = 10. The converter is operated with a delay angle of $\alpha = 30°$. Determine the minimum value of gate pulse width t_G. (9)

7. Discuss any *two* of the following :

(i) Zero space vector placement modulation strategies.

(ii) PWM for multilevel inverters.

(iii) PWM for voltage unbalance. (15)