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322204

May, 2019
M.Tech. - II SEMESTER
ASIC's & FPGA (MVLE-210)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Assume suitable data wherever not provided.*

PART–A

1. (a) What are the features of full custom ASIC? (1.5)

(b) Differentiate between board level testing and system level testing. (1.5)

(c) Indicate the design flow technology using FPGA. (1.5)

(d) Compare behavioral and data flow modelling in VHDL. (1.5)

(e) Write the syntax of inertial delay model in VHDL. (1.5)

(f) Differentiate between floor planning and placement in integrated circuits. (1.5)

(g) Implement one bit comparator using PAL. (1.5)

(h) What is the difference between null and unaffected statements? (1.5)

(i) Name various commercially available FPGA. (1.5)

(j) Define yield. Which factors improves the yield of integrated circuits. (1.5)

PART–B

2. (a) What is meant by synthesis? List and explain steps involved in synthesis? How it is different from simulation. (7.5)

(b) Model full adder circuit in structure modelling using half adder as package. (7.5)

3. (a) Explain different types of ASICs. Describe ASIC design flow in details. (7.5)

(b) Explain the process to carry out serial scan test and parallel scan test with neat sketches. (7.5)

4. (a) What is floor planning? How it is different from placement? Describe K-L algorithm using a suitable example. (7.5)

(b) Write the behavioral model of DFF in VHDL. (7.5)

5. What is FPGA? Using neat sketches differentiate between various classes of FPGA. Explain various types of programming technology used for the implementation of architecture in different FPGA using clear schematic. (15)

6. Design a FSM having input I and output Z, the machine is a sequence detector that produces Z = '1', when the previous two values of I were "00" and "11" else Z = '0'. Model this FSM using VHDL. (15)

7. (a) What is BIST, explain in details. (5)

(b) Compare FPGA, ASIC and CPLD. (5)

(c) Implement full adder using PLA. (5)
