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322202

May, 2019

M.Tech. (VLSI D) - IInd SEMESTER

VLSI Design Verification and Testing (MVL-202)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) What is a layered testbench? (1.5)
   (b) How is verification different from testing? (1.5)
   (c) How is a queue different from linked list? (1.5)
   (d) What are void functions? (1.5)
   (e) How do we separate the testbench and design? (1.5)
   (f) Explain the concept of OOP. (1.5)
   (g) What are various class methods? (1.5)
   (h) How do we control multiple constraint blocks? (1.5)
   (i) What is pre-randomize function? (1.5)
   (j) What is a random number function? (1.5)

PART–B

2. (a) Explain the various testbench components. (7)

   (b) What do you understand by constrained-random stimulus? (8)

3. (a) Differentiate between: Fixed-size arrays and dynamic arrays. (7)

   (b) Explain the method to create new types with typedef. (8)

4. Explain the procedural statements with suitable examples. (15)

5. (a) Explain how to create new objects in System Verilog. (7)

   (b) Differentiate between static variables and global variables. Explain various scoping rules. (8)

6. (a) What is randomization in System Verilog? Explain in detail. (7)

   (b) How are valid constraints different from in-line constraints? (8)

7. Write a note on: Random number generators, Atomic Stimulus generation and Scenario Generation. (15)