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322101

December, 2019

M.Tech. (VLSI) - I SEMESTER

RTL Simulation and Synthesis with PLDs (MVL-101)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART - A

1. (a) Declare a data object of data class variable & data type bit having initial value "1111". (1.5)

(b) Differentiate between Propagation delay and Time skew with the help of waveform. (1.5)

(c) What is the difference between NOC and SOC? (1.5)

(d) What is the difference between RTL source code and encrypted source code? (1.5)

(e) Differentiate between ASICs and FPGA in detail. (1.5)

(f) What is the difference between simulation and synthesis? Explain with examples. (1.5)

(g) Explain the difference between defect, fault and error with the help of an example. (1.5)

(h) What is an LUT? Implement 4X1 multiplexer using three inputs and two input LUTs. (1.5)

(i) Discuss the need of testing in VLSI circuits. (1.5)

(j) Differentiate between Floor planning and Placement with the help of examples. (1.5)

PART - B

2. (a) Draw a signal driver for the following :

Z = transport '1' after 4ns; 7 after 8ns; 5 after 7ns;

wait for 2ns;

Z = transport '8' after 8ns; 8 after 9ns;

wait for 8ns;

Z = transport '5' after 22ns; 9 after 25ns; (8)

(b) Write a VHDL code for T flip flop with preset and clear inputs using behavioral modelling? (7)

3. (a) Differentiate between (i) VHDL and Verilog (ii) Variable and signal assignment statement. (8)

(b) Write a VHDL code for modulo-3 counter using with-select signal assignment statement. (7)

4. Given the following netlist with seven cells [C1, C2, C3, C4, C5, C6, C7] and seven nets:

N1 = {C1, C3, C4, C7} N2 = {C1, C2, C4, C5}
N3 = {C2, C3, C6, C7} N4 = {C5, C6, C7}
N5 = {C3, C4, C5, C6, C7} N6 = {C1, C3, C5, C6}
N7 = {C2, C4, C6}

Solve it using Linear ordering algorithm of floor planning. (15)

5. (a) Differentiate between (i) Transient faults and Intermittent faults. (ii) Fault Collapsing and Fault Equivalence. (10)

(b) Discuss the design flows of Full custom ASICs and Semi-custom ASICs along with their differences. (5)

6. (a) Discuss the various classes of FPGA in detail. Also discuss the various FPGAs with its architecture, logic block type and programming technology. (8)

(b) Discuss the various low power VLSI design techniques in detail. (7)

7. Design an FSM that has an input T and output D. The machine is a sequence detector that produces D = '1' when it detects the sequence "0010". Write a VHDL code for the above FSM. (15)
