6. (a) What are shift registers? Explain with suitable circuit diagram the working of a 4-bit SIPO shift register. (8)

(b) Design the circuit diagram and explain the working of a shift register as a twisted ring counter. (7)

7. (a) What is the effect of propagation delay in asynchronous counters? How it limits the frequency of the applied clock pulse? For what minimum value of propagation delay in each FF will a 10-bit ripple counter skip a count when the frequency of applied clock is 10 MHz. (8)

(b) Design a MOD-12 asynchronous up-counter, make the truth table, draw the waveform diagram and explain its working. (7)

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321403

May-2026

B.Sc.(H) Physics, Semester-IV

Digital Systems and Applications

(PHU–210–V)

Time : 3 Hours] [Maximum Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART – A

1. (a) Write the binary, hexadecimal and BCD equivalent for the number $(124.5)_{10}$.

(b) Obtain the value of b if $(292)_{10} = (204)_b$.

(c) What is meant by the parity of a binary code? Design a five-bit even parity generator using XOR gate.

(d) What is the principle of duality? Obtain the dual expression of (A + C) $(\overline{A}+B) = AB + \overline{A}C$. (1.5)

(e) An encoder circuit has 100 input lines. How many minimum output lines are there? (1.5)

(f) How many input and output lines are there in a multiplexor circuit with four-address line? (1.5)

(g) Differentiate between combinational and sequential digital circuits with examples. (1.5)

(h) What are D-type and T-type flip flops? (1.5)

(i) How many states do have a 5-bit (i) ripple counter, (ii) ring counter and (iii) twisted ring counter have? (1.5)

(j) Three counters, MOD-10, MOD-8 and MOD-6 are connected in cascade? What is the modulus of the cascaded counter? (1.5)

PART – B

2. (a) Draw the DTL circuit for NAND gate and explain its working. (5)

(b) Prove the following using Boolean Algebra and implement simplified expression using NAND gates only.

$A+B[AC+(B+\overline{C})D]=A+BD.$ (5)

(c) What are the main points of minterm and maxterm expressions? Expand $B\overline{C}+AB\overline{D}+ABCD$ to minterms and maxterms. (5)

3. (a) Solve the following expression using K-map and implement the simplified expression using NAND gates only : $Y(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 9, 13, 15) + \sum d(7, 10, 11)$. (6)

(b) What is the limitation of Half-subtractor circuit? Write Boolean expression, truth-table and the NAND gate equivalent circuit for full subtractor. (6)

(c) Subtract –24 from +42 in 2's complement form using 8-bit notation. (3)

4. (a) Draw the circuit diagram of a 4-bit binary adder-subtractor circuit and explain its working. (6)

(b) What is a decoder circuit? Design a 4-to-16 decoder using two 3-to-8 decoders. Write the function table and explain its working. (6)

(c) Distinguish between a multiplexer and a demultiplexer. (3)

5. (a) What is race around condition? Draw the MS flip-flop circuit and explain how it prevents racing problem. (6)

(b) Convert a D flip-flop into JK flip-flop. Make the excitation table of the circuit. (6)

(c) Explain 'Preset' and 'Clear' operations in Flip-flops. (3)