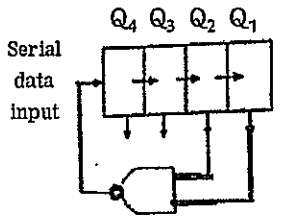
6. (a) The initial state of the following shift register circuit is $Q_4\ Q_3\ Q_2\ Q_1$ = 0111. Explain in detail, the state of the register after 4 clock pulses.



(b) What are shift registers? Explain with suitable circuit diagram the working of a 4-bit serial in, serial-out shift register. (8)

7. (a) Design a MOD-12 ripple/asynchronous up-counter, make the truth table, draw the waveform diagram and explain its working. (7)

(b) How synchronous counters are advantageous over asynchronous counters? Design a MOD-8 synchronous counter and explain its working. (8)

C

Roll No. ..... Total Pages : 4

321414

May–2026

B.Sc. Physics, Semester–IV

Digital Systems & Applications (BPH24–403T)

Time: 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) Convert $(11001011.11)_2$ into its equivalent BCD and octal codes. (1.5)

(b) Implement the logic circuit of the function, $Y = (A + C)(\overline{A} + B)$ using NOR gates only. (1.5)

(c) What is duality thorem? What is the dual circuit of an OR gate? (1.5)

(d) Write the features of minterm and maxterm expressions. (1.5)

(e) Express +76 and −76 in 1's complement and 2's complement form using 8-bit notation. (1.5)

(f) A demultiplexer circuit has 10 output lines. How many input lines and select lines are there? (1.5)

(g) Discuss T-type and D-type flip flops. (1.5)

(h) Explain 'Preset' and 'Clear' operations in Flip-flops. (1.5)

(i) How much time will it take to load a 4-bit data in a PIPO shift register if the clock frequency is 10 MHz? (1.5)

(j) The frequency of the input clock-waveform given to a MOD-8 ripple up-counter is 16 MHz. What will be the frequency of the output-waveform? (1.5)

PART–B

2. (a) Draw the DTL circuit for NAND gate and explain its working. (5)

(b) The output of a three variable logic circuit becomes high when none of the inputs or only two-inputs are high, otherwise the output is low. Write the truth table, Boolean expressions and draw the logic circuit using NAND gates only. (5)

(c) Prove the following using Boolean Algebra and implement simplified expression using NAND gates only. $AB + A\bar{B}C + B\bar{C} = AC + B\bar{C}$. (5)

3. (a) Solve the following expression using K-map and implement the simplified expression using NAND gates only :

$Y(A,B,C,D) = \sum m(0,1,4,5,6,8,9,12,13,14)$ (6)

(b) Show that a full adder circuit is the cascade of two half adders. Implement the full adder circuit using NAND gates only. (6)

(c) Subtract -31 from +49 in 8-bit notation in 2's complement form. (3)

4. (a) Draw the circuit diagram of a 4-bit binary adder-subtractor circuit and explain its working. (7)

(b) Implement a 4-to-16 decoder circuit using two 3-to-8 decoders and explain its working. (8)

5. (a) Differentiate between combinational and sequential circuits. Design a J-K flip-flop circuit and explain its working. (7)

(b) What is race around condition? Draw the MS flip-flop circuit and explain how it prevents racing problem. (8)