MODELING AND SIMULATION OF CNT BASED DEVICES FOR NANOELECTRONICS APPLICATIONS

THESIS

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October, 2019

DECLARATION

I hereby declare that this thesis entitled, "**MODELING AND SIMULATION OF CNT BASED DEVICES FOR NANOELECTRONICS APPLICATIONS**" by **BAL KRISHAN,** being submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under Faculty of Engineering & Technology of J.C.Bose University of Science & Technology, YMCA Faridabad, during the academic year 2012- 2017, is a bonafide record of my original work carried out under guidance and supervision of **Dr. S. K. Agarwal, Professor Department of Electronics Engineering, J.C.Bose University of Science and Technology, YMCA Faridabad** and **Dr. Sanjeev Kumar, Director, DNS College of Engineering & Technology, Amroha, Uttar Pradesh** and has not been presented elsewhere.

I further declare that the thesis does not contain any part of work which has been submitted for the award of any degree either in this university or in any other university.

(Bal Krishan)

Registration No: YMCAUST/PH26/2011

CERTIFICATE

This is to certify that this Thesis entitled, **“MODELING AND SIMULATION OF CNT BASED DEVICES FOR NANOELECTRONICS APPLICATIONS”** by **BAL KRISHAN**, being submitted in fulfillment of the requirement for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under Faculty of Engineering & Technology of J.C.Bose University of Science & Technology, YMCA Faridabad, during the academic year 2012- 2017, is a bonafide record of work carried out under our guidance and supervision.

We further declare to the best of my knowledge, that the thesis does not contain any part of the work which has been submitted for the award of any degree either in this university or in any other university.

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// ABSTRACT heading kept inside
ABSTRACT

Silicon based devices have been serving humankind tenaciously for so many years, that now it is undoubtedly considered as nature's blessing to humanity. Silicon being the point of interest over different semiconductors, has taken over around 90% of electronic devices under its usage. Portable semiconducting devices need that the whole set-up is available on a one chip, which is known as system on a chip(SoC).

To realize a high performance portable device, it is crucial to have a chip which is power, area and speed efficient with larger functionality. After applying various technologies in realizing high performance SoCs, it is noted that CMOS innovation is the most faithful. This is because complementary metal oxide semiconductor not only provides small power and vast noise margin but also be the perfect option to create large integration circuits. At device/circuit levels of speculation, it has been Si MOSFET/Si CMOS which have kept Moore's law substantial till date. The scaling down/scaling of silicon devices is the main impetus for keeping Moore's law. However, Nanoscale device dimensions bring a severe limitation in case of CMOS. It is extremely difficult to scale MOSFET below 32nm/22nm due to SCEs, rise in leakage power, oxide tunneling, limitation of channel transport and sensitivity to process variations in IC manufacturing etc. Thus, when MOS dimensions are in nanoscale, it is difficult as well as vital to design robust circuitry. Hence, advanced devices are the necessity that can be used in place of MOS based FET and can enlarge the expansible of metal oxide semiconductor devices lower than 22nm/18nm technology node.

Now the question arises that to what extent would we be able to keep Moore's law legitimate with silicon based MOSFETs? Additional scaling of a device dimensions require that the supply voltage (V_{DD}) should be decreased, to keep a check on power consumption and to stop device breakdown. But, this has resulted in a remarkable reduction in the speed of operating speed of the devices. Although, the recent the device should surpass the current resolutions, should authorize advanced applications and hence cost should decrease. There are numerous advanced devices like Double gate MOSFET, Fin FET, Pi-FET, Gamma FET etc., but it would be extremely tough to replace conventional MOSFET with these optional devices as these devices are complex, expensive and can't prove to be an ideal arrangement.

A new material and its associated device having a lot of probable to substitute silicon as well as complementary metal oxide semiconductor and can also the expansibility of the devices under twenty two nanometer, be the CNT and its extension device is CNT based FET. Carbon nanotube has a remarkable design with proficient properties which builds it a faithful potential material. Likewise, carbon nanotube based FET be also one of the encouraging building blocks that accompaniment the present Si MOS based FET and which extends the sustainability of Moore's law further. MOSFETs two parameters i.e. V_t and t_{ox} are the main cases /factors, which are responsible for initiation of the leakage of current in MOS based FETs. Miniaturization of MOS based FET, effects its performances as well as fabrication issue.

The impediment of the MOSFET innovation because Zener breakdown will happen at the junction of source and drain, lithography restriction and besides, the control of yield for the item are the limitations to proceed scaled the normal MOS based FET into smaller sizes. Small mobility of carrier in Si also demeans the MOSFET transistor performance. Silicon bulk MOS based FET is nearly to its end and the scaling of measurements underneath 22nm technology is a great troublesome, because of different short channel effects. In addition, additionally scaling of device dimensions request that the supply voltage (V_{DD}) should be downsized, to hold control utilization and to avert device breakdown.

The utilization of CNTFETs in integrated circuits will altogether build the speed of operation, lessen power consumption and will essentially expand the packing density in integrated circuits. Without any doubt it will augment the life of Moore's law fundamentally. These points of interest of CNTs have given us enough reasons to go for CNTFET based designing. Digital applications of CNTFET are available to explore and analog applications still need a wise inspection.

Now, it’s the time to go ahead with these technologies of 21st century.
Therefore, in the thesis we have opted CNTFETs in designing some prevalent analog primary building blocks and at the end we have compared their performance with the conventional CMOS based analog building blocks. The different analog fundamental building blocks designed and developed in this thesis work incorporate folded cascode operational amplifier, folded cascade operational amplifier based low pass filter and operational transconductance amplifier based high pass filter, all utilizing CNTFETs. It is found that the CNT based design has many benefits when compared

with the conventional CMOS based designing, but, a few issues should be conveyed to expand the domain of CNT based designing.

This thesis work investigates the bits of knowledge of the most exceptional utilization of CNT in semiconducting industry, CNTFET. The inspiration of CNTFET invention is due to its amazing features, mainly semiconducting feature. In addition, the persistent push to discover later nanotube based semiconducting device, which can implement as outstanding as MOS based FET also initiate the exploration of CNTFET to be extra forceful. In this work, a comparison is being made between conventional MOSFET and different types of CNTFETs. Lastly closed a future substitution of MOSFET. The real contrast in CNTFETs and MOSFET is that it has CNT in channel rather than Silicon. CNTFETs demonstrate enhanced characteristics with scaling of technology. CNTFET bandgap is straightforwardly influenced by its chirality and diameter, which is the greatest favorable position over MOSFETs. Investigation of different types of CNTFETs comparison is made in this work.

Simulation and Analysis of Carbon Nanotube Based cum CMOS based Folded Cascode Operational Amplifier is presented in this research work. The proposed configuration has the rise in DC gain; fall in average power in CNT based folded cascode Operational Amplifier in contrast with CMOS based folded cascode Operational Amplifier individually. But, the output resistance has decreased in CNT based Folded Cascode Operational Amplifier in contrast with conventional CMOS based Folded Cascode Operational Amplifier. As a result, the bandwidth of carbon nanotube based folded cascode operational amplifier is little due to small output resistance. Further, it is found that CNT based FC-Op-Amp's performance can be upgraded by the optimization of numbers of CNTs.

In this research work, N Type CNT based FET based FC-OpAmp is analyzed through Transient Response. In the Frequency Response of N Type CNTFET based Folded Cascode Op Amp, plainly the amplifier is efficiently working since the DC Gain is practically consistent upto 1 MHz. It is likewise evident that the N Type CNTFET based Folded Cascode Operational Amplifier is acting as low pass filter, so it has applications in the low pass circuits. Further, it is clear from Phase response that it is stable amplifier. In this way, we can utilize it in strong conditions where stability is fundamental concern.

In this research, Simulation of Low Pass Filter is presented. The simulation consequence of proposed CNT based FET based LPF demonstrates that the frequency response of Low Pass Filters are working effectively. It has applications in the low pass circuits. In electronics, these filters are broadly used as a part of numerous applications. In addition, it is clear from the Phase response of CNT based FET based LPF that it is a stable Filter. Along these lines, we can utilize it in capable conditions where stability is primary concern.

In this thesis, research work mainly focuses on design and simulation study of CNT based HPFs has been performed. This chapter mainly focuses on design and simulation study of CNT based HPFs. There are three latest categories of high pass filters which follows the model of CNT based FET and hspice have been used to design at 45nm technology node. Out of the three types of high pass filters, the first one makes use of N type CNT based FETs as sinks and P type CNT based FETs as sources and is named as pure CNTFET based operational transconductance amplifier. The next two sorts are hybrid technology based operational transconductance amplifier high pass filters. Between the two, one engages a combination of N type CNT based FETs as sinks and traditional P type MOS based FETs as sources known as N type CNT based FET - P type MOSFET - Operational transconductance amplifier - High pass filter. Later one is P type CNT based FET - N type MOSFET - Operational transconductance amplifier – High pass filter employing P type CNT based FETs as sources and traditional N type MOS based FETs as sinks. After the examination, enhancement in many of the performance calculating parameters is remarked in carbon nanotube based FET based operational transconductance amplifier high pass filters, primarily CNTFET based operational transconductance amplifier high pass filter. Further, Bandwidth, Output Resistance, Average Power, Phase Margin and Unity Gain Frequency are computed at different voltage level of CMOS –OTA.

The major objective of this thesis is to design and analyze the CNT based analog devices for Nanoelectronics applications. Design and investigation of CNTFET based devices are also presented in this thesis.

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ABBREVIATIONS AND SYMBOLS

Symbol		**Description**
CNT	:	Carbon Nanotube
CNTFET	:	Carbon Nanotube Field Effect Transistor
C_h	:	Chirality
a	:	Grapheme lattice constant
T_{OX}	:	Oxide Thickness
L_{ch}	:	Physical Channel length
S	:	Pitch
fc	:	Cutoff frequency
K_{OX}	:	Dielectric Constant
g_m	:	Transconductance
NM	:	Noise Margin
CMOS	:	Complementary metal oxide semoiconductor
SoC	:	System on chip
Si	:	Silicon
MOSFET	:	Metal oxide semiconductor field effect transistor
IC	:	Integrated circuit
SCEs	:	Short channel effects
nm	:	Nanometer
V_t	:	Threshold voltage
t_{ox}	:	Thickness of oxide
Op- Amp.	:	Operational amplifier
LPF	:	Low pass filter
HPF	:	High pass filter
OTA	:	Operational transconductance amplifier
SiO_2	:	Silicon dioxide
S/D	:	Source/Drain
S RAM	:	Static random access memory
DIBL	:	Drain induced barrier lowering
V_{GS}	:	Gate to source voltage

V_{DS}	:	Drain to source voltage
E	:	Electric field
V. B .	:	Valance band
C .B .	:	Conduction band
CMP	:	Chemical-mechanical planarization
PD-SOI	:	Partially depleted Silicon on insulator
SET	:	Single electron transistor
SPICE	:	Simulation Program with Integrated Circuit Emphasis
NW	:	Nanowire
Ge	:	Germanium
Al_2O_3	:	Aluminium oxide
HfO_2	:	Hafnium
DOS	:	Density of state
ANN	:	Artificial neural networks
I_D	:	Drain current
V_D	:	Drain voltage
D_{CNT}	:	Diameter of the carbon nanotube

CHAPTER 1
INTRODUCTION

The information revolution has been determined usually through continuous development in ICs development. To date, packing density per chip of integrated circuits is about doubling in each eighteen months after 1960[16]. The example, called as Moore's law, has patrolled the electronic industry. The vast majority of advanced equipment used in computerized digital applications is CMOS.

Aggressive miniaturization of MOS based circuits has inspired to more and more packing density, high practical complication and superior performance [17]. MOSFET is a chief part of a CMOS ICs. The essential changing segment used to make digital logic in integrated circuits is MOS based FET. MOS based FET switching speed and as a result circuit speed increases with scaling down. Advance change in digital computers (i.e. better speed and packing density) needs pursued with advancement in scaling down.

1.1 MOSFET- A BASIC BUILDING BLOCK OF INTEGRATED CIRCUIT

MOS based field effect transistor is a kind of FET. There is a insulating gate in it and the gate voltage controls the device conductivity. This ability to vary conductivity with the measure of connected voltage may be used for amplifying/switching the electronic signals. Julius Edgar Lilienfeld had first patented the basic principle of FET in 1925.

1.2 HISTORY

The fundamental rule of such type of device was first authorized by J.E. Lilienfeld in 1925. D. Kahng and M. M. Atalla at Bell Labs envisioned the MOS based FET as a branch to the approved FET design in 1959. Operationally and on a very basic level exceptional in connection to the BJT, the MOS based FET was prepared by depositing a securing film on the plane of semiconductor and after that setting a metallic contact on it. Crystalline Si for the semiconductor and a thermally oxidized film of SiO_2 for the cover is utilized by it. The Si MOS based FET did not distribute restricted electron traps at the interface betwixt Si and its neighborhood oxide layer, and in like way was

naturally free from the catching and scrambling of bearers that had obstructed the execution of before FETs.

1.3 MOS TRANSISTOR – STRUCTURE AND CHANNEL FORMATION

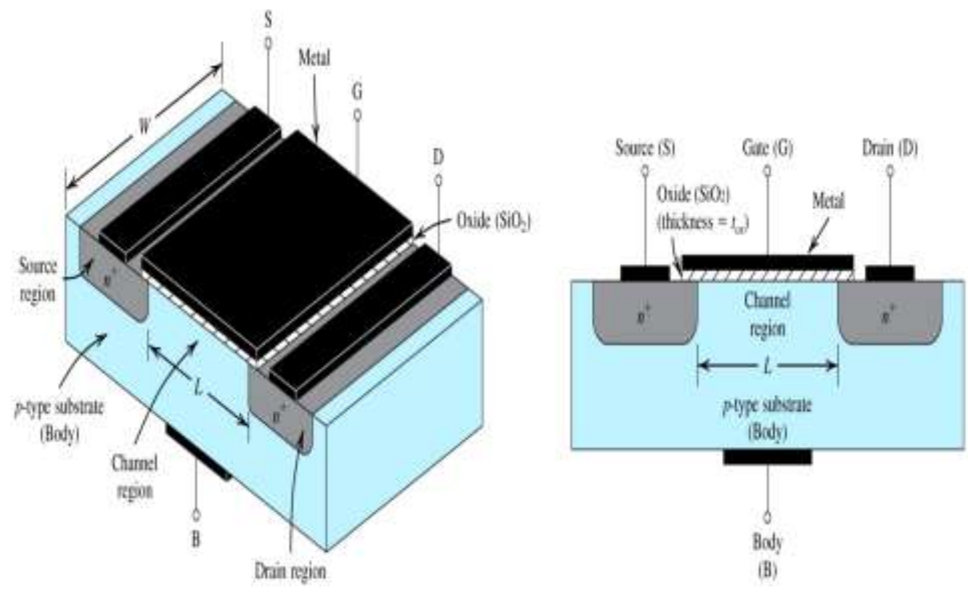


Fig. 1.1: MOS Structure [18]

The MOS based FET, which is usually known as MOS transistor has four terminals: source, drain, gate and substrate. The source terminal supply the carriers either electron or hole. The drain terminal collects the carriers send by the source terminal. The carriers proceed between S to D region via a conducting path called channel. The flow of carriers in the channel is managed by applying voltage at a third terminal known gate of the MOSFET [1]. The channel may be made either electrically or physically. Contingent upon how the channel is made, MOSFETs are divided into two types (a) Enhancement type and (b) Depletion type [19].

In the enhancement type MOSFET, the channel is made electrically by utilizing voltage at the gate terminal whereas in the depletion type MOSFET, the channel is made physically by creating a physical layer between the source and drain at the time of fabrication. Figure 1.1 demonstrates the basic structure of MOS structure.

A semiconductor, either p-type or n-type is taken as a substrate. On the substrate, two diffusion regions are made. In the event that the substrate is p-type, the

diffusion regions are of n^+ type (n^+ shows heavily doped n-type). Whereas for n-type substrate, the diffusion regions are of p^+ type (p^+ shows heavily doped p-type). These diffusion regions are generally known as source and drain. Betwixt the source and drain, a layer of oxide is made over pinnacle of the substrate. This layer of oxide is known as gate oxide and it assumes to be a vital part in deciding the MOSFET characteristics. On top of the oxide layer a metal or polysilicon is deposited. At that point four metal contacts are taken from the source, gate, drain and the bulk to shape the electrodes. There are distinctive symbols used to represent MOSFETs, and these are shown in Figure 1.2.

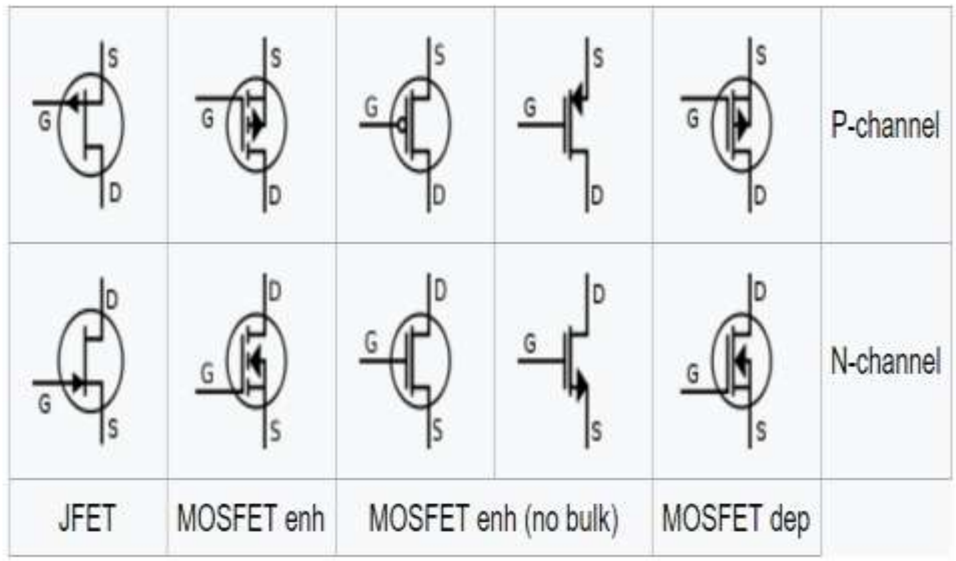


Fig. 1.2: Circuit symbols for MOSFET

1.4 OPERATION OF ENHANCEMENT-TYPE n MOS TRANSISTOR

If a voltage is connected at the gate terminal, a conducting channel is formed underneath the oxide layer betwixt the source and drain. A MOSFET is called n-channel or basically nMOS when the channel is formed with electrons, though, it is known as p-channel or just pMOS when the channel is made of holes. Here we clarify the operations of a n type E-MOS based FET. The structure of the n type E-MOS based FET is appeared in Figure 1.3.

1.4.1 Operation

When gate voltage is zero.

The MOS structure is a combination of metal, oxide and semiconductor which behaves like parallel plate capacitor. Gate oxide acts as dielectric betwixt the plates. Two p-n junctions are associated as side by side diodes. The S/D contacts are secluded by two depletion regions without conduction of current.

Making a channel for current stream.

When gate is subjected to positive supply, the gate attains a positive charge and this positive charge repels the holes away from the surface in the p type substrate resulting in the formation of depletion region. Thus a depletion region is formed when hole concentration at the surface is less than that in the bulk. Furthermore increment in the supply voltage outcomes in the widening of the surface inversion layer which further increasing the bending of bands.

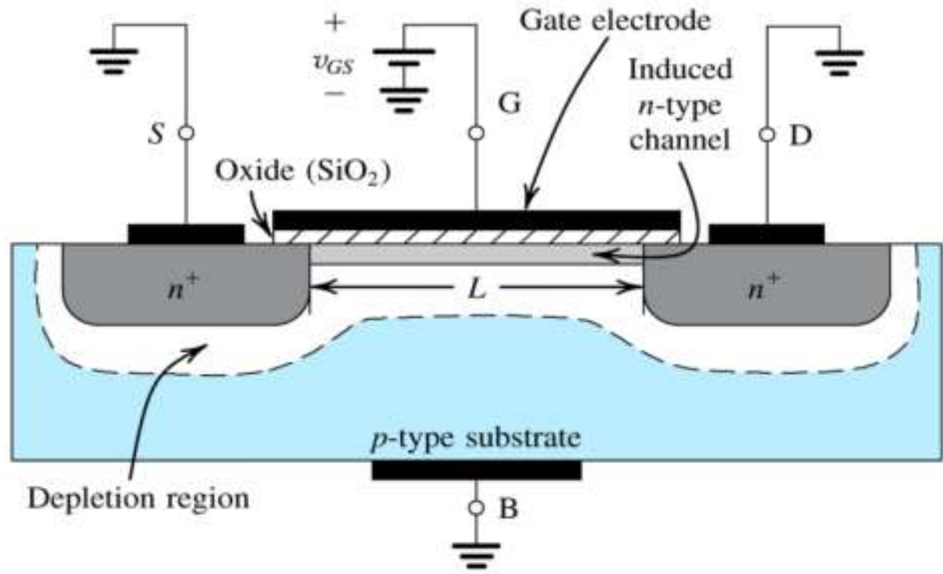


Fig. 1.3: N-Channel Enhancement MOSFET

This will exceed the electron concentration near the surface than the hole concentration and a channel is said to made which supports flow of electrons betwixt source and drain. Thus, a channel is formed just as the gate voltage exceeds Vt. The amount of current flow and thus the channel conductivity depends on the field as MOSFET is a field effect transistor.

Effect of applying drain voltage.

An n channel enhancement type MOSFET conducts when $V_{GS}>Vt$. As $V_{GS}>Vt$, the electrons moves from source to drain through the induced channel contributing to the drain current, whose direction is opposite to that of direction of movement of free electrons i.e. betwixt drain and source. The channel is controlled by the net voltage (V_{GS} - Vt).

Operation as rising drain voltage

When $V_{DS}= 0$, no I_D moves from drain to source. As V_{DS} is increased, a drain current move from drain to source through the conducting medium which is proportional to the applied V_{DS} and the MOSFET is said to be operating in Linear Region. When V_D is further enlarged, the channel depth at the drain side starts to decrease and the channel is said to be tapered. When $V_{DS} = V_{DSsat} = V_{GS} - V_t$, the depth of channel at drain side is reduced to zero and the channel is said to be tapered[19].

Triode region: $V_{DS}<V_{DSsat}$

Saturation region: V_{DS} -V_{DSsat}

The operation of MOSFET is divided into three conditions depending on the voltage connected at the gate terminal.

1. Accumulation
2. Depletion
3. Inversion

Accumulation (V_{GS} is small negative)

Whenever a negative voltage is connected at the gate terminal, the majority carriers (holes) from the p-type substrate are pulled in towards the gate terminal and are collected underneath the gate oxide layer. This condition is called accumulation. If a negative voltage is apply on the gate, holes are drawn to the semiconductor-insulator interface. A conducting surface extends from the bulk all the way to the interface. But because both source and drain are n-type, in accumulation mode, it's like a npn transistor (source and drain are insulated by two reverse biased pn junctions), electrons in source can't go to drain. That is, there is no conduction channel formed.

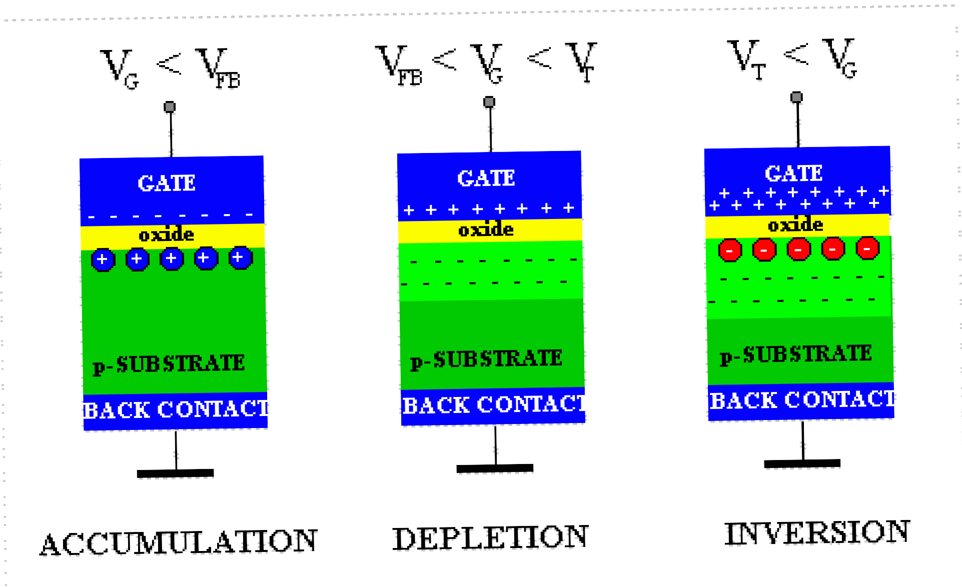


Fig. 1.4: MOS capacitor under different bias conditions

Depletion (V_{GS} is small positive)

Presently, if a little positive voltage is connected, the holes will be repulsed into the substrate. The repulsed holes will move into the substrate and make negatively charged fixed acceptors ions underneath the gate oxide layer. These fixed negatively charged ions make the depletion.

Inversion (V_{GS} is large positive)

If the positive gate voltage is sufficiently substantial, the majority carrier holes are repulsed into the substrate and the little amount of minority carrier i.e. electrons are pulled in towards the gate oxide surface. The attracted electrons accumulate underneath the gate oxide layer and make a conducting path betwixt source and drain. The conducting path is known channel and the condition is known as inversion.

1.5 COMPARISON BETWEEN N-CHANNEL TYPE MOS BASED FET & P-CHANNEL TYPE MOS BASED FET

Comparison between N channel type MOS based FET and P channel type MOS based FET is given in table 1.1

Table 1.1: Comparison of MOSFET

N Channel type MOS based FET	P Channel type MOS based FET
Source and drain are n-kind material.	Source and drain are p-kind material.
Channel is n-kind silicon.	Channel is p-kind silicon.
Gate is n^+ polycrystalline silicon.	Gate is p^+ polycrystalline silicon.
Well is p-kind material.	Well is n-kind material.
Conduction when $V_{GS} > V_T$.	Conduction when $V_{GS} < V_T$.
E-Mode when threshold voltage is greater than zero.	E-Mode when threshold voltage is less than zero.
D-Mode when threshold voltage is less than zero.	D-Mode mode when threshold voltage is greater than zero.
Electrons are layer carriers in inversion.	Holes are layer carriers in inversion.
Substrate is p-kind material.	Substrate is n-kind material

1.6 APPLICATION - CMOS CIRCUIT

The MOSFET is used as a part of advanced integral metal oxide semiconductor logic, in which its p-type channel and n-channel are utilizing like building blocks. This complementary metal oxide semiconductor is an innovation for manufacturing ICs. CMOS technology is used in S RAM, MPs, MCUs and digital logic based circuits. Many analog circuits like CMOS based image sensor, data converters use CMOS technology for some sorts of communication.

Noise immunity and low power consumption are the important attributes of complementary metal oxide semiconductor. As single transistor of the pair is regularly off, the sequence arrangement pulls significant power only momentarily throughout switching betwixt on and off states. So, CMOS devices don't waste plentiful heat like other types of logic, for instance TTL logic or N type metal oxide semiconductor logic, that regularly keep few standing current, even when not vary the state. Complementary metal oxide semiconductor too provides bulk functions on a single chip. This was principally hence complementary metal oxide semiconductor changed into the most used innovation to be implemented in VLSI chips.

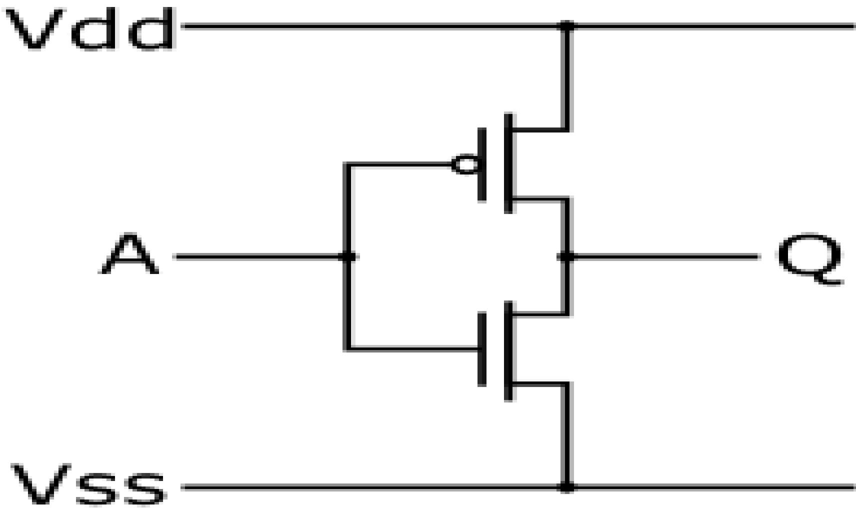


Fig. 1.5: CMOS Inverter

1.7 CMOS

The significant concern, which builds complementary metal oxide semiconductor circuits striking, is that the circuits dissipate very small dc power. The utilization of low power makes CMOS based circuits essential in convenient uses in which battery drain is basic to the lifetime of the system like portable PCs, digital watches. In addition, little power dissipation is extremely imperative in very thick circuits. For working conditions, when no. of devices per chip increments, low power dissipation is critical in keeping room-temperature. Likewise as the temperature of Si rises, it finally become intrinsic, implying that the free carrier concentration inside the conduction band, outcomes mostly from inter band thermal generation, invalidating the impact of doping, hence failure of device occurs. Not with standing utilizing broad heat sinking strategies, this is hard to dissipate of wasted heat completely.

However, are complementary MOS circuits are developed to such an extent that they dissipate little dc power? Power dissipation is alleviated by having no less than one transistor in cutoff, where it's I_D is astonishingly low for all viable logic inputs between V_{DD} and ground. Along these lines, the power source is constantly shielded from ground by a high resistance path. A complementary metal oxide semiconductor circuit is composed in such a way that a current move in the circuit only during transitions/switching with the conspicuous exemption of leakage current.

Insistent miniaturization of the MOS circuits has led to more and more packing density, high functional complexity and better performance [17].

In addition, when the MOS based FET gate length enters nm range, SCEs - threshold voltage roll-off and DIBL becomes significant [20-22], which constrains the scaling capacity of planar bulk/SOI MOS based FET. A few leakage current mechanisms in MOS based FET, for example, reverse-bias P-N junction current, weak inversion current and DIBL are being obtainable by short-channel effect. The performance of the transistor in nano-scale MOS based FET is affected by the tunneling effect. When barrier distance is reduced, effect of tunneling will rising exponentially. MOS based FETs, V_t and t_{ox} are main elements in nano-scale which introduce the leakage current. Miniaturized the traditional MOSFET, convey to transistor performance matters as well as fabrication matter. The limitation of the MOS based FET technology is because of the fact of Zener breakdown occurs at source and substrate junction, limitation of lithography and furthermore the product's yield control are the limitations to proceed scaled the traditional MOS based FET into miniature sizes. Mobility of the low carrier in Si (in comparison to CNT) also diminshes the performance of MOS based FET.

When size of device touches the nanorange, the new possibilities emerge from exploiting the physical and chemical properties at the nanorange. The intrinsic physical properties such as conductivity, density and chemical reactivity of bulk materials are independent of their sizes [1-15].

1.8 SHORT CHANNEL EFFECTS

Primary aim of miniaturization of transistors is rising pace and lowering cost. When the size of circuits goes smaller, its capacitance decreases, in this manner increasing operating speed. In a similar token, smaller circuits permit a greater amount of them in a similar wafer, distributing the aggregate cost of a one wafer between many dies.

In any case, with substantial diminution arrive incredible issues, for this situation as undesirable symptoms, the supposed SCEs [23]. Exactly while channel of MOS based field effect transistor turns into an alike form of size as the width of depletion layer of S/D, the transistors begin carrying on in a surprising way, that influence designing, authenticity and performance. The impacts are classified as follows:

Drain-Induced Barrier Lowering

The effect is better comprehended when we watch the potential barrier profile that an electron needs to overcome to go between source and drain.Under typical situations (V_{DS}=0 and V_{GS}=0), there is a potential barrier which stops the electrons from spilling out of source to drain. The voltage of gate has the capacity of letting the barrier down to the point where electrons are able to move. Ideally the primary voltage that would control the hindrance. A big V_{DS} widens the drain depletion region to a point which diminishes the potential barrier as the channel turns up shorter. In this way, the effect is relevantly called Drain Induced Barrier Lowering.

The top figure 1.6, demonstrates a slit of a short channel (solid line) and a long-channel MOS based FETs. The base part shows the potential hindrance profile across the surface of the channel (between source and drain). In the left side, V_{DS}=0, while in the right the drain voltage is raised to show the drain induced barrier lowering effect.

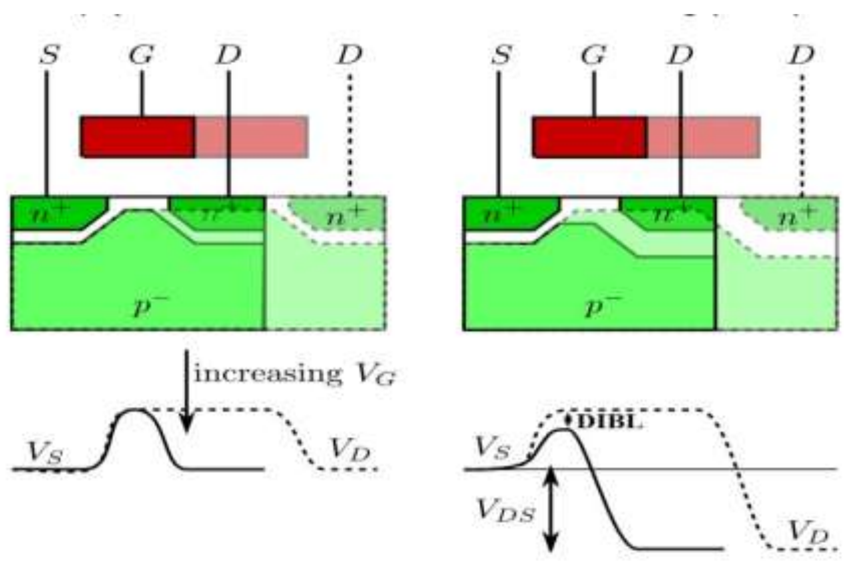


Fig. 1.6: DIBL

The drain is adequately close to the source to which in turn forms the depletion region usually made by the gate. That is, the drain depletion region enlarges to the source, forming a special depletion region called as punch through. Then a high drain voltage can open the bottleneck and give to turn on the transistor as a gate

would. This tends to decrease the threshold voltage of the transistor, which leads to higher leakage current.

DIBL lowering impact may be given by calculating Vth as a function of two maximum drain voltages, V_D .

$$\mathbf{DIBL} = \frac{(\mathbf{Vth}\ (\mathbf{V_D^{low}}) - \mathbf{V_{th}}\ (\mathbf{V_{supply}})}{\mathbf{V_{supply}} - \mathbf{V_D^{low}}}$$

Where V_D^{low} is a very low drain voltage and Vsupply is the supply voltage (the most elevated drain voltage whicht can be connected). This capacity is constantly positive and no DIBL impact would return 0.

Surface Scattering

The velocity of charge carriers is characterized by the mobility of that carrier times the electric field along the channel. At the point when the carriers move along the channel, they are pulled in to the surface by the vertical electric field generated by the voltage of gate. So, the charge carriers begin continuous crashing and bouncing against the surface, all through their path, following a zigzagging way. Figure 1.7 demonstrates Surface Scattering.

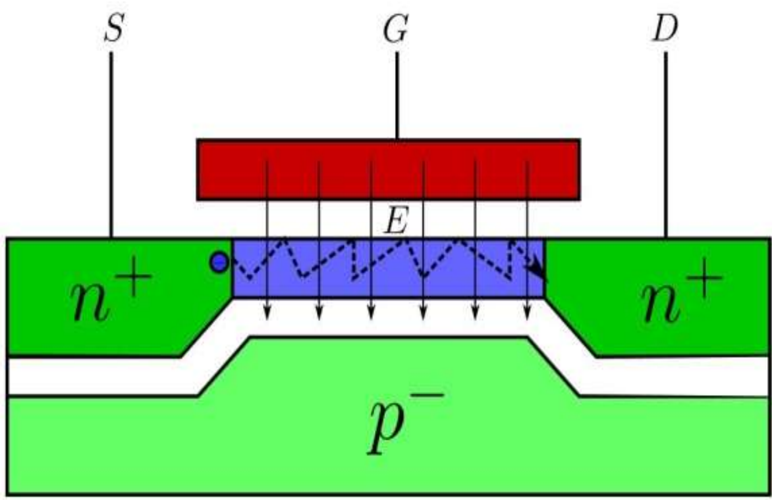


Fig. 1.7: Surface Scattering

This adequately decreases the surface mobility of the carriers, in contrast with their bulk mobility; amend in carrier mobility effect the C-V relationship of the transistor.

When the electron goes via the channel, it is attracted to the silicon- silicon dioxide interface and bounces against it. This effect reduces the electron's mobility. Short-channel impact, when the length of the channel begins smaller, the lateral electric field produced by V_{DS} becomes stronger.

To repair that the vertical field of the gate voltage demands to increment proportionally, that can be done by diminishing the thickness of oxide. As a symptom, surface scattering gets heavier, decreasing the effective mobility in comparison to the longer channel nodes

Velocity Saturation

The velocity of charge carriers is relative to the electric field which drives them, however it is sufficient for little fields. As the field gets more grounded, their velocity goes to saturate. It suggests that over a critical electric field, they have a tendency to settle their speed lastly can't move speedier. Velocity saturation is essentially found in short channel MOS based FET transistors, since they have higher electric fields.

The critical velocity is described by the material the charge carriers are moving through. Specifically, in diffusion it is characterized by their doping concentration. As first-order estimation, the carrier velocity is described as below:

$$v_d = \frac{\mu E}{1+E/E_c} \qquad (1)$$

Where E is electric field, μ is the mobility of carrier and Ec is the critical electric field.

Impact Ionization

As specified before, short-channel transistors make strong lateral electric fields, as the partition among source and drain is very little. This electric field offers the charge carrier with high velocity, and thus, high energy. The carriers which have sufficiently high energy, to generate difficulties are called hot carriers.

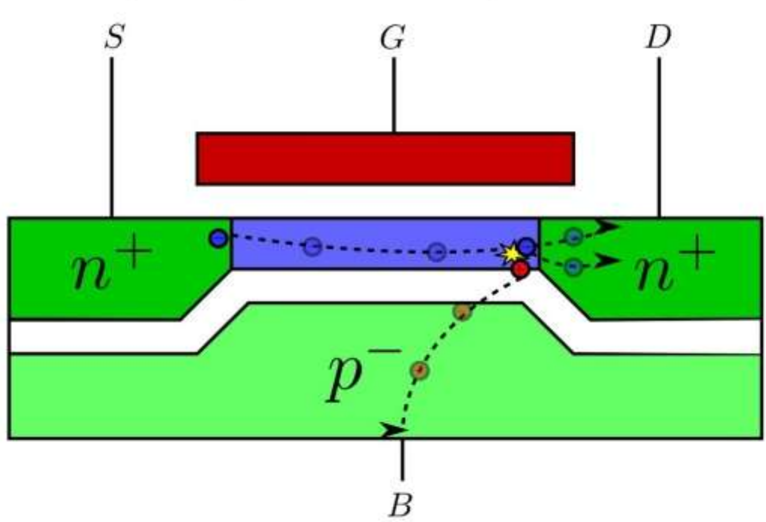


Fig. 1.8: Impact Ionization

These commonly appear to be close to the drain, where they have the most energy. As they are moving via a Si lattice, there is a probability that they collide with an atom of the structure. Adequately given energy, the energy gone to the atom upon collision can hit out an electron out of the V.B. to C.B. This starts an electron-hole pair: the hole is pulled in to the bulk while the created electron continues ahead to the drain. The substrate current is a respectable way to measure the effect ionization impact.

1.9 RECENT DEVELOPMENTS AND FUTURE PROJECTIONS

The trend of scaling down has come to such a degree that a normal device and its interconnect structure just don't work. For instance, contracting of gate oxide thickness has decreased it to almost a couple of atomic layers of SiO_2. At this low measurement, the quantum mechanical tunneling begins dominating and the ultra-thin gate oxide can't function as a insulator any longer. Along these lines, technologists are striving for elective material for gate oxides having high-K or high dielectric constant. This understands the reason for decreasing V_T of the MOS based device. Meanwhile, it avoids quantum mechanical tunneling because of increased thickness.

Then again, the field oxide which is utilized to isolate the metal wires makes high parasitic coupling capacitances. The coupling capacitances effectively affect timing and functionality. It can present crosstalk noise which may violate the functionality of a circuit. It can also lead to delay degradation. Thus, to decrease the

parasitic capacitance, materials with low-K or a low dielectric constant are utilized for insulating metal layers.

Generally, aluminum has been the metal utilized for interconnection wires. Yet, as another metal, copper which has a superior conductivity than Al is discovered more appropriate for interconnects. Cu interconnect will have lesser parasitic resistances and henceforth lesser RC wire delay. However, there is an issue with Cu interconnects. Cu can easily diffuse into Silicon and henceforth, it degrades the device attributes. To keep the Cu diffusion into Si, IBM analysts have built up a process called the Dual Damascene process which utilizes an extraordinary metallization step. In this metallization process, Cu is filled into the trenches etched into the insulator and after that a CMP step is utilized to expel the additional material from the top.

Silicon on Insulator

The silicon-on-insulator (SOI) technology has been created and found to be an alternative to conventional CMOS technology. The fundamental favorable reason of SOI innovation is the reduction of the parasitics related with the CMOS devices. This gives better transistor characteristics when contrasted with a conventional CMOS device. The SOI procedure is appeared in Figure 1.9.

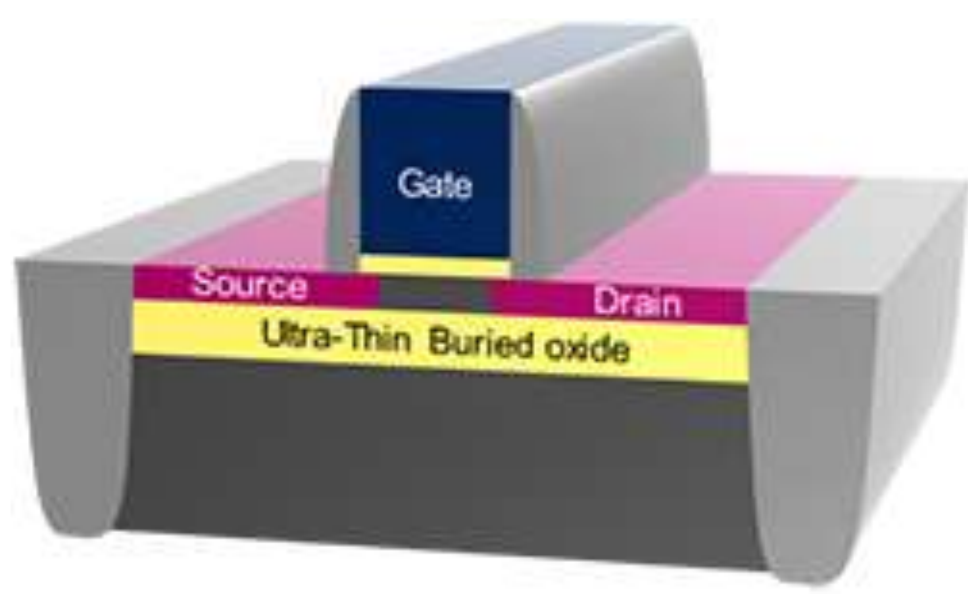


Fig. 1.9: Silicon-on- insulator process

Silicon on insulator transistors are made over a thin layer of Si deposited over a thick layer of silicon dioxide. As the miniaturization below the 22 nanometer node innovation then the process-induced changes of transistor is increases and below 22 nanometer there is a great challenge for pursued improvement of PD-SOI CMOS [24, 25].

Three-Dimensional Chips

The idea of the three-dimensional Chips has been presented with the help of Figure 1.10. In the 3D integration, extra active layers, included between the metal layers can implement logic at one level, memory at another level, and I/O at on another level. This decreases the interconnect length between active layers and hence the delay. Another approach is to bond completely processed wafers on which the circuits are manufactured. Just the interconnections between the dies have to be made and packaged. This sort of integration is not completely 3D, but rather 2.5D, and is called systems on a package.

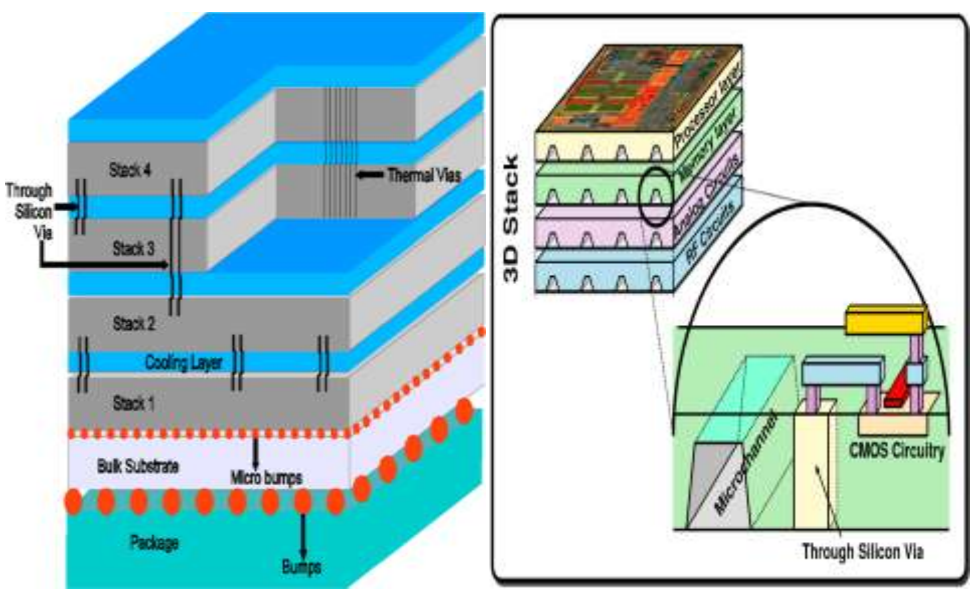


Fig. 1.10: Three Dimensional Chip

In double-gate MOS based FET; there are two gates which are placed on the opposite sides of channel of silicon to manage the potential of channel. This is most effectively executed like a vertical structure. This "Fin FET" structure has been broadly explored

[26-30], and can be achieved on silicon on insulator substrate/bulk Silicon substrate [31, 32].

Nanoelectronic Devices

Scaling the MOS devices has already achieved the nanometer level. Be that as it may, this down-scaling can't sustain when the dimension achieves the molecular dimension. At this stage, the conventional CMOS device structure can't be accomplished and subsequently, the conventional IC design and technology have to be totally changed. Researchers have proposed numerous new devices at the nanometer dimensions which are frequently called nanoelectronic devices. The distinctive nanoelectronic devices can be categorized as follows:

Solid-state

- RTD
- SET
- Ballistic electrons devices

Molecular

- Organic transistors
- CNTs
- Monomolecular transistors

As the nano devices are controled by the use of a little number of electrons or one electron, devices size and power consumption supposed to be only a small fraction of that in conventional MOS based devices.

1.10 CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Traditional bulk innovation has been strength of character for the designing of circuit for the last 30-40 years. It may be accredited to miniature of physical sizes of CMOS semiconducting devices that result in considerable performance increment of MOS based FETs. In any case, additionally scaling of devices underneath 22nm face serious difficulties such as SCEs, leakage, loss of control, reliability, self-warming etc. When size of MOS based FET fall below a few tens of nanometers, then it generates low transconductance, leakage of gate oxide, degradation of mobility and increased delay.CNT based FETs are unique semiconducting devices which are estimated to continue scalability of the transistor while raising its performance. The major

difference betwixt CNT based FETs and MOS based FETs is that CNTs are used as a channel in former device, which allows high current density, because of high carrier mobility in CNTs as compared to bulk Si. [33, 34].

The mentioned issues posture considerable difficulties to the designing of circuit and fabrication at nano-range. Therefore, there is a necessary requirement for substitute material to Si and substitute device structure to bulk MOS based FET, so the performance degradation of devices underneath twenty two nanometer node may be ceased. Newly structures of semiconducting device such as multi gate MOS based FETs, Fin based FETs [26, 27], Trigate devices, strained Si devices and high-k metal gate devices have been succeeded. The resulted in scaling the device dimensions below 22 nm and performance is better, But, the structures of the newly semiconducting devices are complicated, expensive and have thermic problems. To realize a high performance portable device, it is crucial to have a chip which is power, area and speed efficient with larger functionality. After applying various technologies in realizing high performance SoCs, it is noted that CMOS innovation is the most faithfull. This is because complementary metal oxide semiconductor not only provides small power and vast NM but also be the perfect option to create large integration circuits. At device/circuit levels of speculation, it has been Si MOSFET/Si CMOS which have kept Moore's law substantial till date. The scaling down/scaling of silicon devices is the main impetus for keeping Moore's law. However, Nanoscale device dimensions bring a severe limitation in case of CMOS. It is extremely difficult to scale MOSFET below 32nm/22nm due to SCEs, rise in leakage power, oxide tunneling, limitation of channel transport and sensitivity to process variations in integrated circuits manufacturing etc[24, 25].

Thus, when MOS dimensions are in nanorange, it is difficult as well as vital to design robust circuitry. Basic boundaries of CMOS technology and expectations of Moore's law have provoked researchers to find appropriate substitute for these devices. There are many proposed alternatives [35-39], CNT based FETs is a faithful solution for CMOS devices due to its extraordinary properties/characteristics [35, 40].

There is a quick need of new device structures that can change the traditional MOS based FET and can broaden the scalability of MOS based devices beneath 18-22 nanometer technology node. Be that as it may, the new semiconducting device must outperform the present solutions, must empower newly applications and result in a huge cost drop.

A newly material and its related device that can supplant silicon and complementary MOS and can expand the adaptability of device underneath twenty two nanometer is carbon nanotube and its related transistor, CNT based FET. CNT has extraordinary properties that make it a faithful material in future. Also, CNT based FET is a faithful basic building block to supplement the traditional Si MOS based FET and can realize the development of the authenticity of Moore's law further.

1.11 CARBON NANOTUBE

Carbon powder produced by a direct current arc-discharge in the middle of carbon electrodes in 1991, he found a set of molecules which have been the item of extreme scientific investigation ever since. By HRTEM microscope, a long molecular structure containing of many coaxial cylinders of carbon was found. The investigation runs the research domain for CNT, while the production of C filaments had already commenced in 1970s and 1980s by the synthesis of vapor grown C fibers.

The discovery of single walled carbon nano-tube is more huge as this structure is more basic and turned into the premises for the conceptual studies of huge bodies [1–6, 8-15, 41-48]. A SWNT is a 1-D conductor which may be metallic and semiconducting relying on the arrangement of C atoms decided by their chiral vector, Ch, whose magnitude and relationship with D_{CNT} is stated by Equation (1) & (2) separately where 'a' is the Graphene lattice constant (0.249 nm) and n_1, n_2 are positive integers which specify the chiral vector of the tube.

$$Ch = a\,(n_1^2 + n_2^2 + n_1 n_2)^{1/2} \qquad (1)$$

$$D_{CNT} = Ch / \pi \qquad (2)$$

This also explains that single wall carbon nanotube is a sheet of graphene that is rotated up and joined together across a wrapping vector, $Ch = n_1.a_1 + n_2.a_2$ as appeared in Figure 1.11(b), where a_1, a_2 are unit vectors. D_{CNT} is the diameter of the carbon nanotube. Chirality is the key concept used to identify and describe the different configurations of CNTs and their resulting electronic band structure. A broad range of electrical, thermal, and structural properties depending on the tube diameter, length, and chirality, or twist.Different ways of rolling the graphite sheet will give different types of carbon nanotube.

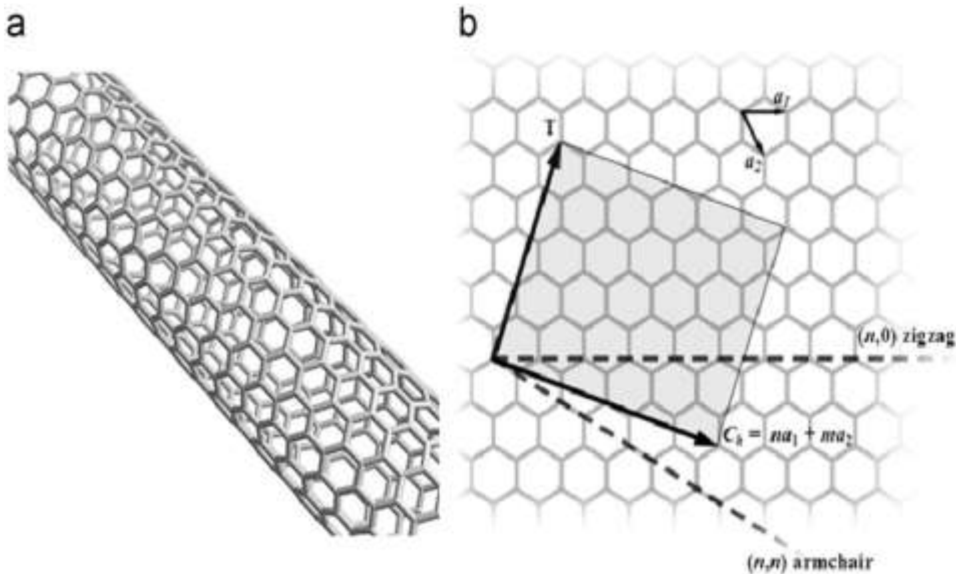


Fig. 1.11: (a) Single wall carbon nanotube (b) Graphene sheet in terms of C_h, n_1 and n_2

1.12 STRUCTURE OF CNT

CNT is a empty cylinder, which is made of single or many concentric layers of C atoms in a lattice arrangement [42]. Fundamentally they are categorized as follows: MWNTs and SWNTs.

Single-Walled Carbon Nanotube

A graphene sheet that rolls like a cylindrical shape, is known as single walled nanotube. It is one dimensional with axial symmetry. The diameter of single walled nanotube is generally 1nm–2nm and length is around 100micrometers. The characteristically little geometric size of SWCNTs of∼1 nm prompts the optimization of the coupling betwixt the gate and the channel of a transistor and gives awesome potential in the use of nano-scale devices and circuits [50-65].

Single-walled nanotube are classify into following categories: armchair, zigzag and chirality. Armchair nanaotube and zigzag nanotube are otherwise called a chiral single walled nanotube as its replica is analogous to the native structure. The title of armchair and zigzag appear from the shape of cross-sectional ring as given in Table 1.2. Then again, chiral nanotubes show spiral consistency with its mirror picture can't be rebuilt from the initial one. Figure 1.12, demonstrates the terminations of these three sorts of single walled nanotube and from this figure, this presents the terminations are incorporated of hemisphere of fullerene [49].

Table 1.2: Categorization of CNT

Type	Shape of cross section	Chiral vector
Armchair		(n,n)
Zigzag		$(n,0)$
Chiral	Combination of armchair and zigzag cross section	(n,m)

The hemisphere, otherwise known as 'cap', holds 6 pentagons and a suitable no. of hexagons which totally fit the hemisphere's shape.

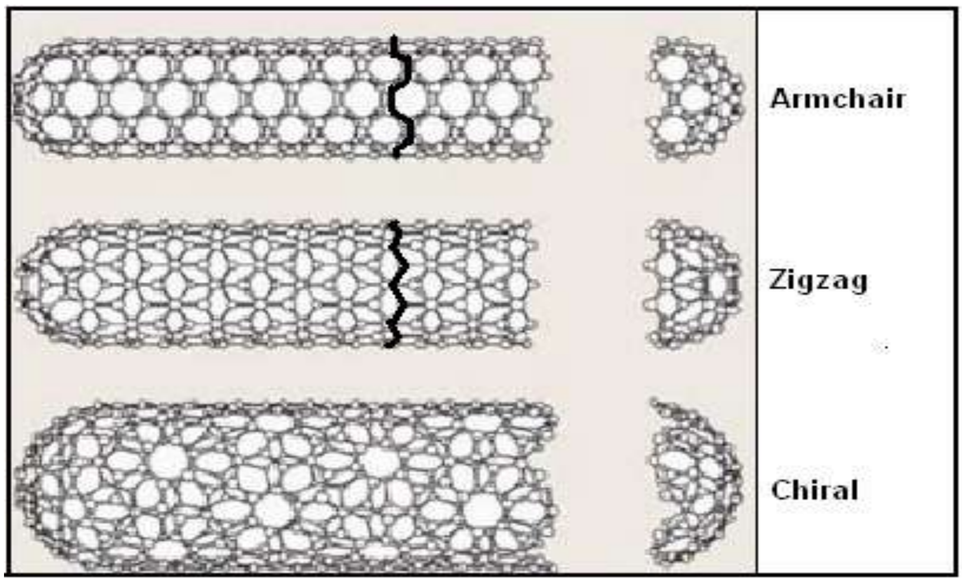


Fig. 1.12: Three kinds of SWNT

The three sorts of single walled nanotube rely upon the chirality component. The chirality is depicted by a solitary vector known as the chiral vector [49]. Figure 1.13,

shows the vector, C_h as given beneath. Vectors OA and OB describes the chiral vector and translational vector.Ch may be given as

$$C_h = na_1 + ma_2,$$

Where a_1 , a_2 = unit vectors and n, m = integers such that $0 \leq |m| \leq n$.

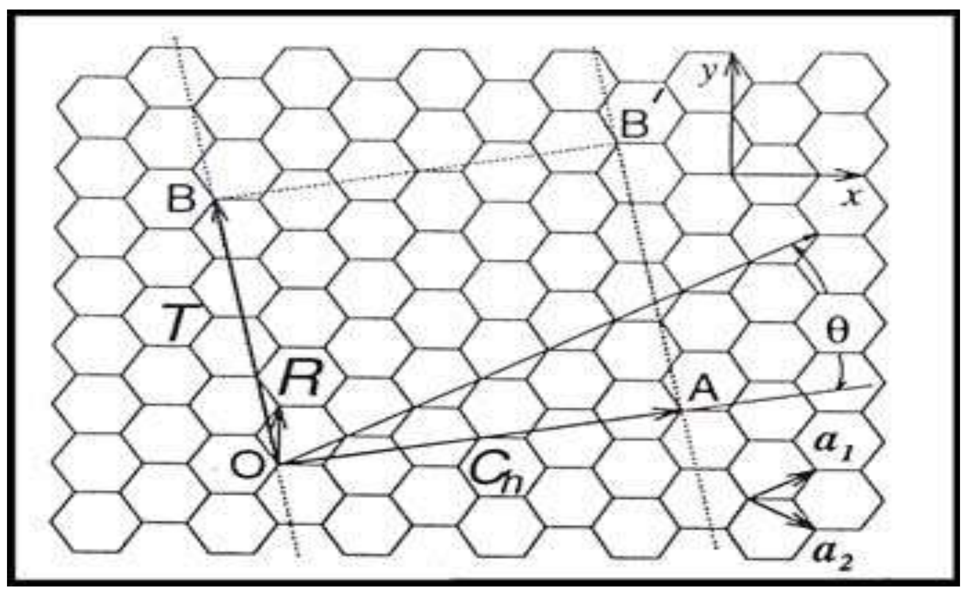


Fig. 1.13: State vectors a_1 and a_2 and axis vector T about which a Graphene sheet is rolled

Distinctive method for rotating the graphene sheet will give diverse kind of CNT as presented early. Expecting the graphene sheet is turned about vector T, if vector T is parallel with Carbon-Carbon bond, a structure is gotten known as armcahair structure. Conversely, if vector T is perpendicular with Carbon-Carbon bond, at that point zigzag structure is gotten. Otherwise, at that time chiral structure is set up if vector T is neither parallel nor perpendicular to Carbon-Carbon bond. The estimations of m & n are associated to that kind of a particular CNT structure. Armchair Single walled nanotube analogous to the case n = m and zigzag analogous to m = 0 although all other conjunction lead to chiral nanotubes.

Multi-Walled Carbon Nanotube

The first nanotube discovered by scientist Iijima is MWNT in 1991. Since at that time, the new epoch of research in CNT has begun. A multi walled carbon nanotube is made of a set of coaxially arranged single walled carbon nanotube of different radius

[66].The separation betwixt nearest neighbor shells is roughly about the vander-Walls distance for two graphite C lattice that is around 3.4Å. Multi walled nanotube's external distance across is really relies upon the improvement procedure and especially of order 20nm and up to 100nm. Figure 1.14, portrays multi walled nanotube's structure.

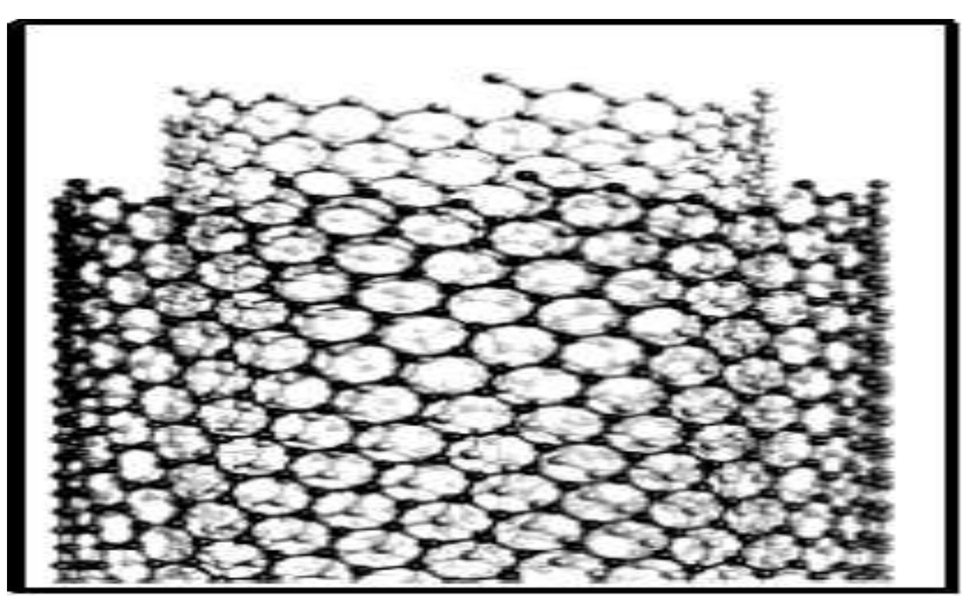


Fig. 1.14: Structure of Multi-Walled Carbon Nanotube

There is a procedure to destroy the concentric shells in Multi-walled carbon nanotube beginning with the external shell. This should be possible by applying huge current into the multi walled carbon nanotube and thus the external shell will have substantial part of current streaming by means of. The concentric shell will ultimately end separate as the current value surpasses 10^9 A/cm^2.The breaking procedure of concentric shells is because of what is called current induced electrical breakdown. The procedure is clarified in Figure 1.15.

MWCNTs can be made in high amounts and are simpler to clean (in contrast with SWCNT and DWCNT). This makes their manufacturing costs essentially lower, and is a purpose behind their adoption in various areas of research. Utilizations of multi walled carbon nanotubes have been basically focused around their utilization in composites where they can be utilized as an added substance. either to: I) improve the mechanical properties of a material, or ii) to improve the electrical properties of a material. Beside being utilized as added substances, functionalized multi walled

carbon nanotubes are being used in a variety of medicinal and biotechnological applications..

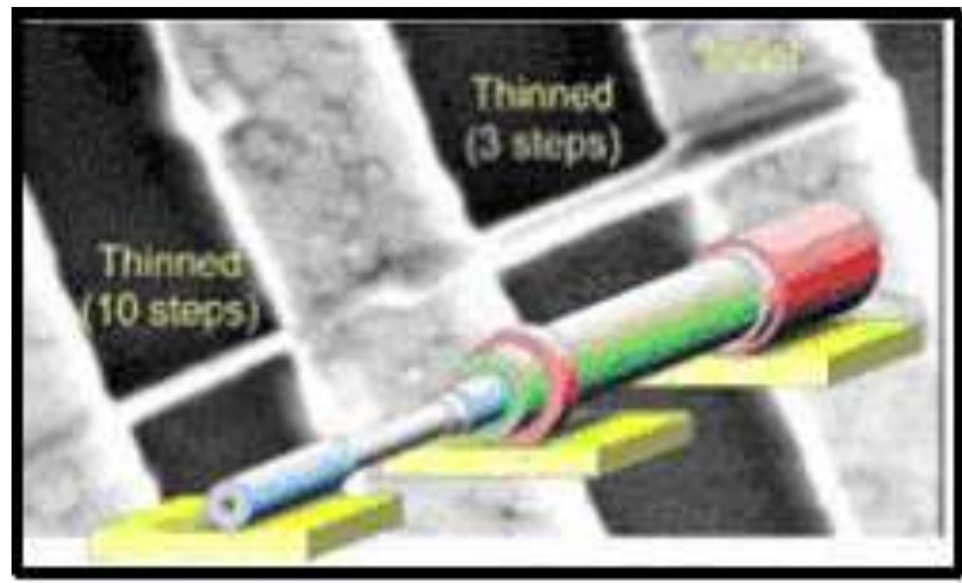


Fig. 1.15: Current induced electrical malfunction process in MWNT

1.13 ATTRIBUTES OF CNT

The motivation behind why carbon nanotube is extremely fitting for future semiconducting electronic applications is not because of carbon nanotube small dimensions but rather its remarkable attributes uniquely the electrical attributes [42]. One of the attributes of carbon nanotube is that the transport of carrier is 1-D in CNT. The carrier movement can subdue the scattering impact and in the meantime can motivate the ballistic transport. In this way, carbon nano tube's power dissipation is less.

The chemical bonds in the midst of the Carbon atoms in carbon nanotube are contented and there is no requirement for uninvolved dissemination of dangling bonds as in Si. Hence the carbon nanotube based semiconducting devices are not bind to utilize the SiO_2 as the insulator however large dielectric constant and crystalline insulator may be utilized. The primary electrical and mechanical properties are summarized in Table 1.3 underneath.

Table 1.3: Basic electrical and mechanical properties of CNT

Electrical conductivity	Metallic/Semiconducting
Electrical transport	Ballistic
Energy Gap	E_g (eV) ≈ 1/d (nm)
Max. current density	~10^{10} A/cm^2
Thermal conductivity	6000 W/km
D_{CNT}	One to hundred nanometer
Gravimetric surface	Up to millimeters
E- Modulus	> 1500 m^2/g

1.14 MOTIVATIONS FOR TRANSISTOR APPLICATIONS

The chirality and diameter of CNTs is directly affects its band gap. If these parameters are managed, CNTs would turn into a faithful possibility for upcoming nano-size based transistor devices. Besides, CNTs has the perfect and hollow cylindrical structure, which doesn't have boundaries. So, it causes no boundary scattering. Just forward scattering and back scattering can be watched as carbon nanotubes are also quasi- one dimensional material. Quasi-ballistic transport can also be seen in CNTs at moderately large lengths and small fields due to elastic scattering MFPs in CNTs are long, normally around micrometers.

CNT have strong covalent carbon–carbon bonding, thus making them chemically inert and move a lot of electric current. On a basic level, carbon nanotube can conduct warm about and additionally diamond, and because of its downsized dimensions, CNT based FET should switch dependably using altogether less power than a Si- based gadget.FET comprising of carbon nanotube are called CNT based FET and lately they have pulled in the consideration as conceivable building blocks of future nanoelectronics due to their extraordinary properties [68].

1.15 CNTFET TECHNOLOGY

CNTs were first found by Dr. Iijima in 1991, while considering the surface of graphite electrode anode in an arc discharge [69]. CNTs have remarkable and marvellous mechanical, electrical and thermal attributes and are supposed as faithful upcoming materials. CNTs are hundred times more stronger in comparison to steel, have better FE attribute, have substantial current density of more than 10^9 A/cm^2, and have

thermal conductivity higher in comparison to diamond. Carbon nanotubes have two structures: SWCNT and MWCNT. A critical and main use of carbon nanotube is CNT based FET. A CNT based FET is a faithful future semiconducting device and can possibly supplant the coventional MOS based FET and the expand the legitimacy of Moore's law further. A CNT based FET has extensive g_m, little capacitance, about perfect sub threshold slope and exceptionally hard covalent bonding. This has been discovered that the CV/I attribute of an intrinsic n and p sort CNT based FET is thirteen times superior to the traditional MOS based FET. There are two sorts of CNT based FETs: SB CNT based FET and MOS based FET-like CNT based FET. A SB CNT based FET may be realized by directly joining the intrinsic SWNTs to the metal S/D contacts.This kind of CNT based FET demonstrates ambipolar carrier transport. The MOS CNT based FET has carbon nanotube based channel joining heavily doped S/D contacts. This has unipolar conduction, has high I_{ON}, larger on current to off current proportion and lower leakage power.

The structures of CNFET fundamentally look likes the structure of MOS based FET except that the Si channel is substituted by the CNT. The major difference betwixt CNT based FETs and MOS based FETs is that CNTs are used as a channel in former device, which allows high current density, because of high carrier mobility in CNTs as compared to bulk Si. However, the arrangement continues changing to enhance the performance of the semiconducting device. A distinctive structure of a MOS based FET like CNT based FET device is given in Fig. 1.16.

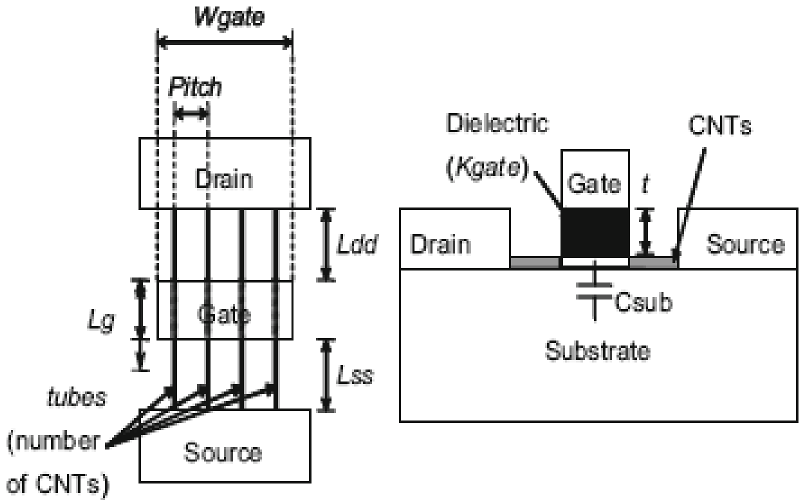


Fig. 1.16: Schematic CNTFET cross-section

The carbon nanotube channel region is undoped, whilst another region are heavily doped, so acting as the S/D broadened region and/or interconnects betwixt two contiguous devices. CNTs are large A.R. proportion cylinders of C atoms. The electrical attributes of a SWCNT give the potential for molecular scale base electronics; a typical semiconducting SWCNT is 1.4 nanometer in diameter with a 0.6eV bandgap (i.e. Egap α $1/D_{CNT}$). Presently CNT based FETs are accessible with a metal carbide S/D contact and a best gated structure with thin gate dielectrics (Figure 1.17).

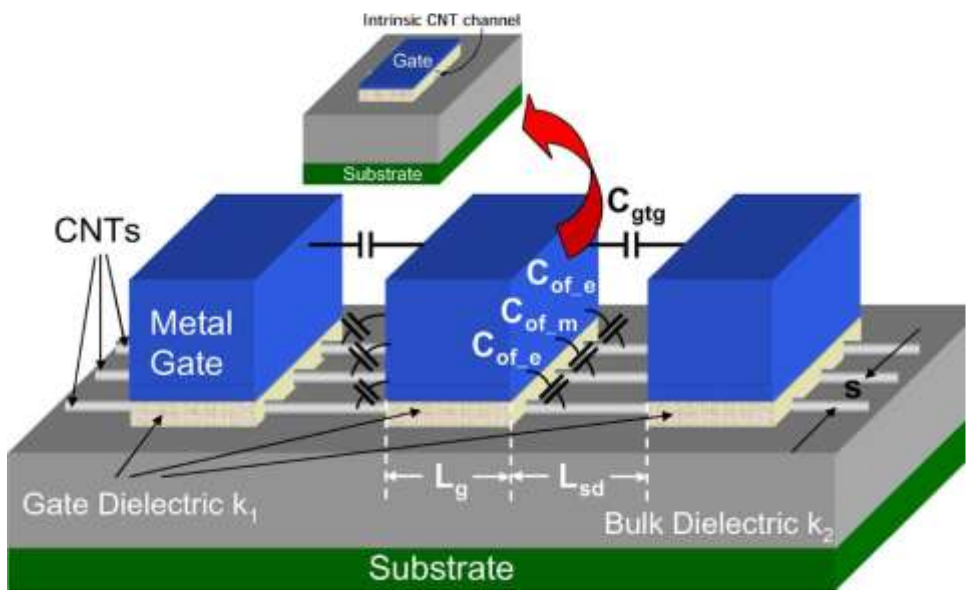


Fig. 1.17: Three dimensional device structure of a CNT based FET With multiple channels

In CNT based FET and MOS based FET, sub threshold slope and resistance of contact are similar. While a Si field effect transistors current drive is typically calculated in current per unit device width, the CNT based FETs current is measured in current per tube (as reflecting the structure of the CNT based FET as an array of equal CNTs with constant spacing and fixed diameter). Jie Deng et. al. have proposed Carbon-Nanotube Field-Effect Transistors.

The model is legitimate for CNT based FETs with metallic/semiconducting carbon nanotube channel. This model considers different non idealities such as quantum confinement impacts, the acoustical/optical phonon scattering in the channel region and the screening impact by the presence of numerous carbon nanotubes in the

channel. The model is near experimental models and is exceptionally successful for outlining analog/digital circuitry.

Along the size of device measurements to accomplish high performance, the necessity of exact circuit simulators becomes salient to capture different impacts, mainly at nanosize. The semiconductor device designers and specialists require advanced and exact circuit simulators to definitely compute and predict the power utilization, timing, yield, functionality and noise etc. of the devices.Numerous circuit simulators have been evolved, such as PSICE, ViewSPICE, TSPICE, ZSPICE and forecast different performance calculating parameters. Although, HSPICE, the circuit test system evolved by Synopsys is found to be additional efficient and exact. This is being known as enterprises "gold standard" its exactness and proficiency. This has device foundry-authentic MOS based FET models along the state of the art simulation/analysis algorithms. Moreover, this has reasonably precise CNT based FET models that can be utilized for simulation of CNT based FET based circuit.

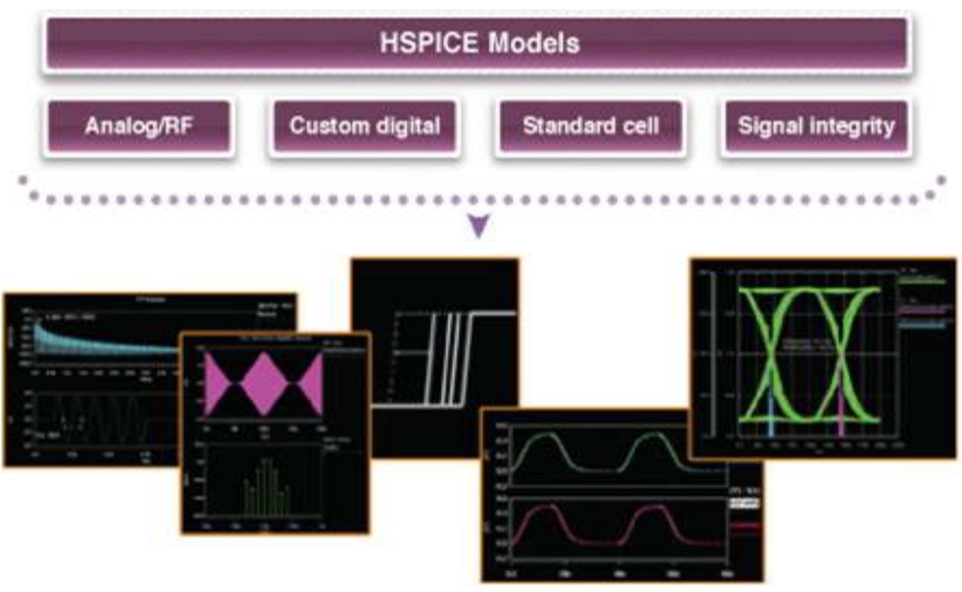


Fig. 1.18: HSPICE models flow chart

1.16 MOTIVATION OF RESEARCH

The advance in Si innovation keeps on outpacing the noteworthy speed of Moore's rule, yet the finish of device scaling now looks just ten to fifteen years away. Hence, this is of extreme enthusiasm to discover newly, nano-size semiconducting devices that may supplement a fundamental Si stage by furnishing it with new capacities or

that may even supplant existing Si innovation and permit gadget downsizing to proceed to the atomic scale.While gadget sizes reach the nanorange, new chances appear from utilizing the physical and chemical properties at the nanorange. Quantum event and dimensional transport may guide new utilitarian gadgets with altogether different power/performance tradeoffs.

1.17 RESEARCH OBJECTIVES

The final goal of this research work is the apply electronics circuits in analog based circuits specifically utilizing CNT based FETs.

The various objectives planned are as follows:

1. To design carbon nanotube based electronic circuit.
2. To make device compact.
3. To enhance the device parameters by incorporating different types of materials.
4. To analyze the designed carbon nanotube based device by the variation of carbon nanotubes.
5. To design the nanoelectronics devices.

1.18 ORGANIZATION OF THE THESIS

A definitive goal of this work is the actualize electronics circuits in common and analog based semiconducting circuits specifically utilizing CNT based FETs. CNTFET is a device that can possibly change the traditional bulk innovation effectively. In this manner, different analog blocks have been outlined utilizing CNT based FETs rather than the traditional MOS based FETs. As the present Si based electronic circuits confront some extreme difficulties as far as high power dissipation, extensive delay, less reliability, large cost, substantial self-warming etc., so, the need of the time is to supplant the fundamental material Si with some newly material and the traditional MOS based FET with another device. Carbon nanotube and CNT based FET are the material and device separately that can possibly change Si and the bulk MOS based FET because of their remarkable attributes. The utilization of CNT based FETs has extensively decrease power dissipation, enlarged speed, enlarged integration levels, decreased self warming and has resulted in reliable ICs. The brief details of these chapters are given below.

This thesis contains eight chapters, including the present one.

The first chapter deals with the general foundation of the research work done. The inspiration behind work is given. The different issues identified with the analog blocks simulated in the thesis are narrated in detail. The details regarding the models and the design tool utilized in simulating of the analog type blocks are explained.

The second chapter, deals with the survey of carbon nanotube based electronics circuits (analog type and digital type circuits) composed till date. It features the imperative focuses about the best in class identified with the proposed circuits.

The chapter 3 gives a complete analysis of CNT based FET and a comparison is being built betwixt conventional MOSFET and different types of CNTFETs. And finally concluded a future replacement of MOSFET. The major difference in CNTFETs and MOSFET is that it has CNT in channel instead of Silicon. CNTFETs show improved characteristics with scaling of technology. Chirality and diameter are instantly of CNT affects the bandgap of a CNTFET, which is the biggest advantage over MOSFETs. Study of various types of CNTFETs is made and a comparison is made in this chapter.

In Chapter 4, design and full analysis of CNT based cum CMOS based folded cascode Operational-Amplifier has been carried out. Gain of DC voltage, B.W., average power and o/p resistance have been evaluated. CNT based folded Cascode Op Amp results in high performance as the increment of carbon nanotubes. As, the increment in DC voltage gain is 41.48% in pCNT based folded cascode Operational Amplifier and 13.93% in nCNT based folded cascode Operational Amplifier; decrease in average power is by 16.86% in pCNT based Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS based folded cascode Operational Amplifier respectively.Still, the output resistance has diminished in carbon nanotube based FC-OP AMP in contrast with traditional complementary metal oxice semiconductor based Folded Cascode OP AMP. Low output resistance has resulted in a small B.W. in carbon nanotube based FC-OP AMP. Further, the design analysis have disclosed that its performance may be enhanced streamlined at various CNTs.

In Chapter 5, Transient analysis of N type Carbon Nanotube based cum CMOS based Folded Cascode operational amplifier has been carried out. In this chapter, simulation of N Type CNFET based folded cascode Op Amp based on CNTs has done at 45 nm technology. N Type CNT based FET based FC-Op Amp is

analyzed through Transient Response. In the Frequency Response of N Type CNTFET based Folded Cascode Op Amp, it is clear that the amplifier is efficiently working since the DC Gain is almost constant upto 1 MHz. It is also clear that the N Type CNTFET based Folded Cascode Op Amp is working as low pass filter, so it has applications in the low pass circuits. Further, it is clear from Phase response that it is stable amplifier. So, we can use it in robust conditions where stability is main concern. Furthermore, it is clear that the amplifier is power efficient since in all the conditions, the Transient Power is in nano watts.

In chapter 6, Design and Simulation of CNT based FET based LPF has been performed. In this research paper, simulation of Low Pass Filter has done at 45 nm technology using hspice. The simulation result of proposed CNT based FET based LPF show that the frequency response of Low Pass Filters are working satisfactory. It has applications in the low pass circuits. In electronics, these filters are widely used in many applications. Moreover, it is clear from the Phase response of CNT based FET based LPF that it is stable Filter. So, we can use it in powerful conditions where stability is main concern.

In chapter 7, Design and Simulation study of CNT based HPFs has been performed. This chapter mainly focuses on design and simulation study of CNT based HPFs. There are three latest categories of high pass filters which follows the model of CNT based FET and hspice have been used to design at 45nm technology node. Out of the three types of high pass filters, the first one makes use of N type CNT based FETs as sinks and P type CNT based FETs as sources and is named as pure CNTFET based operational transconductance amplifier. The next two sorts are hybrid technology based operational transconductance amplifier high pass filters. Between the two, one engages a combination of N type CNT based FETs as sinks and traditional P type MOS based FETs as sources known as N type CNT based FET - P type MOSFET - Operational transconductance amplifier - High pass filter. Later one is P type CNT based FET - N type MOSFET - Operational transconductance amplifier – High pass filter employing P type CNT based FETs as sources and traditional N type MOS based FETs as sinks. After the examination, enhancement in many of the performance calculating parameters is remarked in carbon nanotube based FET based operational transconductance amplifier high pass filters, primarily CNTFET based operational transconductance amplifier high pass filter. Further,

Bandwidth, Output Resistance, Average Power, Phase Margin and Unity Gain Frequency are computed at different voltage level of CMOS –OTA.

Chapter 8 finishes up the thesis work. It features different issues, which should be tended to in future. The different analog fundamental building blocks designed and developed in this thesis work incorporate folded cascode operational amplifier, folded cascade operational amplifier based low pass filter and operational transconductance amplifier based high pass filter, all utilizing CNT based FETs. It has been noticed that the CNT based design has many benefits in contrast with the conventional CMOS based designing, but, a few issues should be conveyed to expand the domain of CNT based designing.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

Ordinary CMOS innovations have been a spine for circuit outlining for the last 30 to 40 years. It may be assigned to the scaling of physical sizes of conventional MOS based semiconducting devices that have arised about the remarkable achievement improvement of MOS based FETs. In any case, additionally scaling of devices underneath 22nm face serious difficulties such as SCEs, leakage, loss of control, reliability, self-warming etc. When size of MOS based FET fall below a few tens of nanometers, then it generates low transconductance, leakage of gate oxide, degradation of mobility and increased delay. CNT based FETs are unique semiconducting devices which are estimated to continue its scalability, when rising achievement of transistor. The major difference betwixt CNT based FETs and MOS based FETs is that CNTs are used as a channel in former device, which allows high current density, because of high carrier mobility in CNTs as compared to bulk Si [33, 34]. Such problems create sizeable difficulties into circuit outlining and manufacture at nanosize. In this way, it is requirement for search the substitute material of Si and optional semiconducting device structure to the conventional MOS based FET, so that degradation in the performance of the devices underneath 22 nanometer technology node may be paused. The developed novel device structures are multigate MOS based FETs, FinFETs, high k metal gate type devices,Trigate type devices[26, 27]. The mentioned solutions have actually upgraded the accomplishment and have developed in downsizing the semiconducting device sizes underneath 22 nanometer but, the new device structures have the issue of thermal, cost and complexity.

To realize a high performance portable device, it is crucial to have a chip which is power, area and speed efficient with larger functionality. After applying various technologies in realizing high performance SoCs, it is noted that CMOS innovation is the most faithfull. This is because complementary metal oxide semiconductor not only provides small power and vast NM but also be the perfect option to create large integration circuits. At device/circuit levels of speculation, it has been Si MOSFET/Si CMOS which have kept Moore's law substantial till date. The scaling down/scaling of silicon devices is the main impetus for keeping Moore's law.

However, Nanoscale device dimensions bring a severe limitation in case of CMOS. It is extremely difficult to scale MOSFET below 32nm/22nm due to SCEs [24, 25], rise in leakage power, oxide tunneling, limitation of channel transport and sensitivity to process variations in IC manufacturing etc. Thus, when MOS dimensions are in nanorange, it is difficult as well as vital to design robust circuitry. Hence, advanced devices are the necessity that can be used in place of MOS based FET and can enlarge the expansible of metal oxide semiconductor devices lower than 22nm/18nm technology node.

2.2 RECENT DEVELOPMENTS AND FUTURE PROJECTIONS

The trend of scaling down has come to such a degree that a normal device and its interconnect structure just don't work. For instance, contracting of gate oxide thickness has decreased it to almost a couple of atomic layers of SiO_2. At this low measurement, the quantum mechanical tunneling begins dominating and the ultra-thin gate oxide can't function as a insulator any longer. Along these lines, technologists are striving for elective material for gate oxides having high-K or high dielectric constant. This understands the reason for decreasing V_T of the MOS based device. Meanwhile, it avoids quantum mechanical tunneling because of increased thickness.

Then again, the field oxide which is utilized to isolate the metal wires makes high parasitic coupling capacitances. The coupling capacitances effectively affect timing and functionality. It can present crosstalk noise which may violate the functionality of a circuit. It can also lead to delay degradation. Thus, to decrease the parasitic capacitance, materials with low-K or a low dielectric constant are utilized for insulating metal layers.

Generally, aluminum has been the metal utilized for interconnection wires. Yet, as another metal, copper which has a superior conductivity than Al is discovered more appropriate for interconnects. Cu interconnect will have lesser parasitic resistances and henceforth lesser RC wire delay. However, there is an issue with Cu interconnects. Cu can easily diffuse into Silicon and henceforth, it degrades the device attributes. To keep the Cu diffusion into Si, IBM analysts have built up a process called the Dual Damascene process which utilizes an extraordinary metallization step. In this metallization process, Cu is filled into the trenches etched into the insulator and after that a CMP step is utilized to expel the additional material from the top.

Silicon on Insulator

The silicon-on-insulator (SOI) technology has been created and found to be an alternative to conventional CMOS technology. The fundamental favorable reason of SOI innovation is the reduction of the parasitics related with the CMOS devices. This gives better transistor characteristics when contrasted with a conventional CMOS device.Silicon on insulator transistors are made over a thin layer of Si deposited over a thick layer of silicon dioxide. As the miniaturization below the 22 nanometer node innovation then the process-induced changes of transistor is increases and below 22 nanometer there is a great challenge for pursued improvement of PD-SOI CMOS [24, 25].

Three-Dimensional Chips

In the 3D integration, extra active layers, included between the metal layers can implement logic at one level, memory at another level, and I/O at on another level. This decreases the interconnect length between active layers and hence the delay. Another approach is to bond completely processed wafers on which the circuits are manufactured. Just the interconnections between the dies have to be made and packaged. This sort of integration is not completely 3D, but rather 2.5D, and is called systems on a package.In double-gate MOS based FET; there are two gates which are placed on the opposite sides of channel of silicon to manage the potential of channel. This is most effectively executed like a vertical structure. This "Fin FET" structure has been broadly explored [26-30], and can be achieved on silicon on insulator substrate/bulk Silicon substrate [31, 32].

Nanoelectronic Devices

Scaling the MOS devices has already achieved the nanometer level. Be that as it may, this down-scaling can't sustain when the dimension achieves the molecular dimension. At this stage, the conventional CMOS device structure can't be accomplished and subsequently, the conventional IC design and technology have to be totally changed. Researchers have proposed numerous new devices at the nanometer dimensions which are frequently called nanoelectronic devices. As the nano devices are controled by the use of a little number of electrons or one electron, devices size and power consumption supposed to be only a small fraction of that in conventional MOS based devices.

So, the designing of robust conventional MOS based circuits are becoming very tough and important, while the sizes of CMOS are in nanoscale. Basic boundaries of CMOS technology and expectations of Moore's law have provoked researchers to find appropriate substitute for these devices. There are many proposed alternatives [35-39], CNT based FETs is a faithful solution for CMOS devices due to its extraordinary properties/characteristics [35, 40]. Silicon bulk MOS based FET is nearly to its end and the scaling of measurements underneath 22nm technology is a great troublesome, because of different short channel effects. In addition, additionally scaling of device dimensions request that the supply voltage (V_{DD}) should be downsized, to hold control utilization and to avert device breakdown. The utilization of CNTFETs in integrated circuits will altogether build the speed of operation, lessen power consumption and will essentially expand the packing density in integrated circuits. Without any doubt it will augment the life of Moore's law fundamentally. These points of interest of CNTs have given us enough reasons to go for CNTFET based designing. Digital applications of CNTFET are available to explore and analog applications still need a wise inspection.

Now, it’s the time to go ahead with these technologies of 21st century.
A detailed literature review of analog & digital applications of CNT based FETs is presented in this chapter.

In paper [70], optimal design of an inverting amplifier MOS based, CNT based FET based and hybrid technologies based are analyzed at 32 nano meter node. The performance of an inverting amplifier are analyzed with the changing of carbon nanotube's parameters - number of CNTs, pitch, diameter in pure CNT based FET and hybrid technologies and the optimization of performance, power and area are achieved. The extent, chances and problems related with proposed models are also explored. Its established that pure CNT based FET amplifier gave good amplification whereas hybrid p type CNT based FET n type MOS amplifier offered outstanding frequency response and p type MOS n type CNT based FET amplifier hence giving better transient performance when compared with planar CMOS.

The invention of first CNT based FET, as shown in Figure 2.1, has also been reported by Sander J. Tans et. al.[71]. This is a three terminal switching device, contain of one carbon nanotube semiconducting type placed betwixt two electrodes of metal. An

important step towards molecular nanoelectronics is the fabrication of this switching device. The present device, conversely, works at room temperature, in this manner meeting an imperative prerequisite for potential practical applications. Electrical estimations on the nanotube transistor show that its operation attributes can be subjectively portrayed by the semiclassical band-bowing models right now utilized for conventional semiconductor devices. The manufacture of the three-terminal switching device at the level of a solitary atom presents to an imperative stride towards molecular electronics.

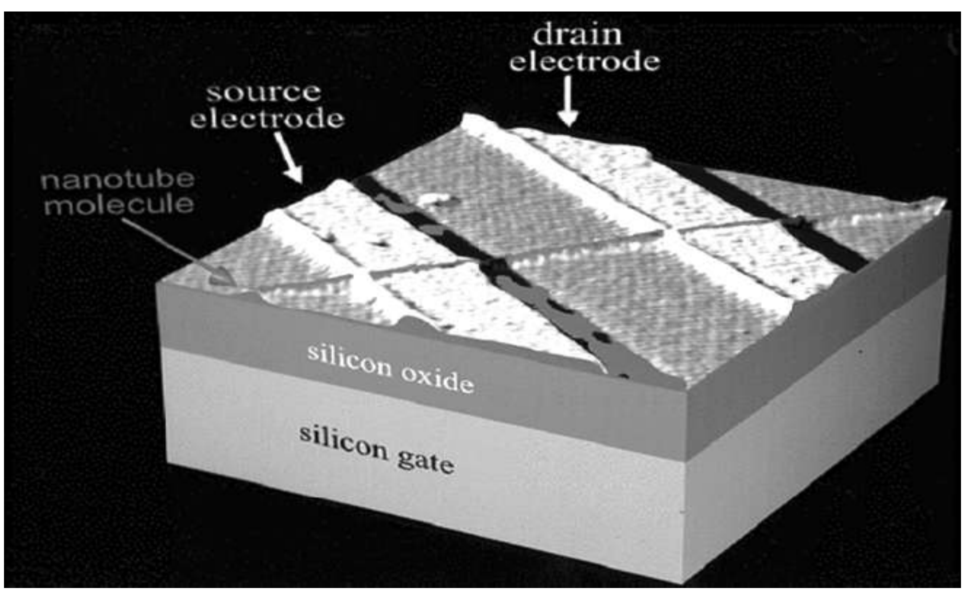


Fig. 2.1: First CNT based FET[71]

Kureshi et.al. [72] represents the CNT FET and Complementary metal oxide semiconductor based 6T static random access memory cell are analyzed at 32 nano meter node. HSPICE designs, did utilizing Berkeley prescient innovation demonstrate. Because of innate characteristics of CNT based FET, similar to great gate controllability, drive current and immunity to SCE, CNT based FET cell out performs in saving of leakage power, the write margin, read SNM and speed in comparison to MOS based cell.

Trigate Si nanowire (NW) proposed [73] MOSFETs fabrication and characterization at temp. betwixt 77 and 300 K in the dark and under light pumping. Nanowire width of W and height of H, gate length of Lg, and gate oxide thickness of Tox,

respectively, are 7nm to 25nm, 16nm, 34nm to 52nm, and 7nm. The mentioned are experimentally explored quantum transport properties of Silicon nanowire based MOS based FETs in the dark and under optical pumping through temp.-dependent voltage-current characterization. When device features sizes are in nano-range, appropriate design on the measurements of NW and length of channel are essential in a structure like the studied devices, to utilize the quantum interference impacts for a particular set of qualities also to stifle the impact for traditional ICs applications from present and future point of view.

Islamshah Amlani et. al. [74] proposed an approach to compute frequency response function of high impedance SWCNT based field effect transistor based nanosize semiconducting device. A top gate type CNT based FET is designed like a CS amplifier whose response of frequency is calculated. Designing of AC and DC characteristics utilizing the same physical parameters is given in fig.2.2, with satisfactory agreement of computation which permits forecasting intrinsic performance of the semiconducting device.

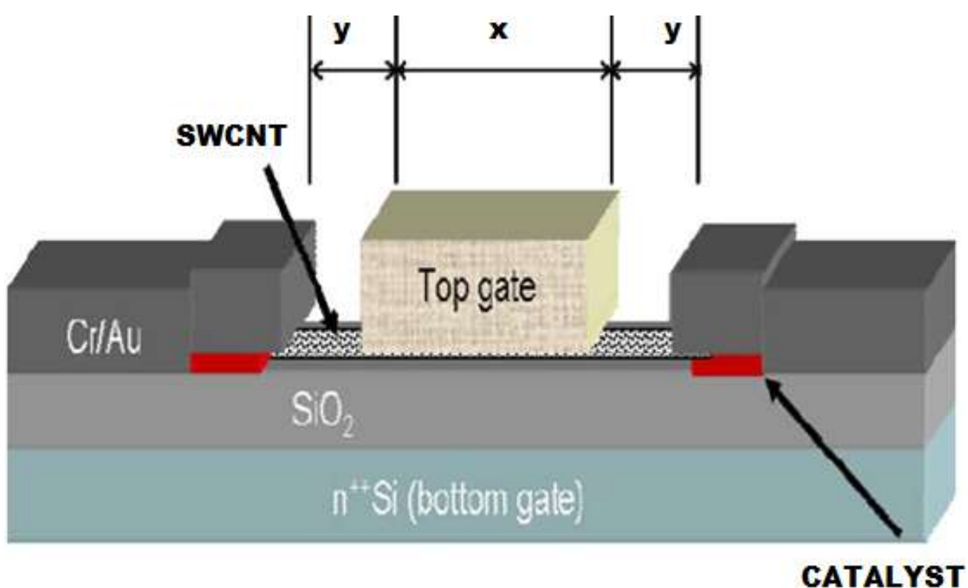


Fig. 2.2: Three dimentional fabricated Single Walled Nanotube based Field Effect Transistor [74]

Bipul et.al. [75] demonstrated an in-depth investigation of NW and CNT based device performance under process changeability. This additionally clarified that NW/CNT based field effect transistors are less sensitive to numerous process parameter varieties because of their intrinsic device structures and geometric properties. This was watched that a 2 i/p NAND gate with NW/NT based field effect transistors demonstrated less performance change than its conventional MOS based FET counterpart more than 4 times and about 2 times less than FinFET semiconducting devices at 45 and 32 nanometer innovations, respectively. The investigation additionally support NW and NT examine for high performance circuit applications and is trusted that procedure parameter changes will drastically constrain the possibility of future traditional MOS based FET semiconducting devices, will continue to even more extremely restrict the performance of emerging devices.

Jie Deng et. al. [76] also proposed a compact SPICE Model for CNT based FETs (Figure2.3). The proposed design model is authentic for CNT based FETs, which have metallic/semiconducting carbon nanotube as a channel. This model looks different non idealities like quantum restriction impacts, the acoustical/optical phonon scattering in the channel region and the screening impact by the existence of many carbon nanotubes in the channel. It is a test model that is extremely viable for analog and digital circuitry.

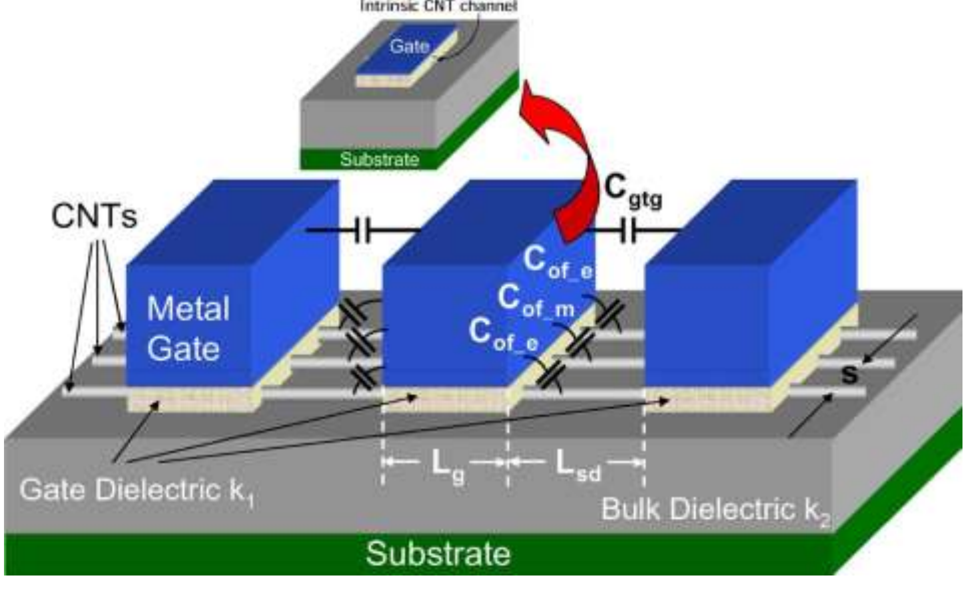


Fig. 2.3: A Compact SPICE Model for CNT based FETs

In paper [77], an analytical answer for the charge essential equation of the FETToy Model is given. Under the different physical parameters values and biasing condition, the accuracy for the proposed model is investigated. Advance examinations were done to evaluate the model precision in the subthreshold region and within the existence of short channel effects. The result of the examinations was compared with those obtained by some unique models created before in the scholarly works. These show prevalent accuracy of the proposed design model with compared with substitute models. This examines the exactness of the proposed design model in various diverse ways- for different values of the physical parameters, temp. values and biasing condition, in subthreshold region and in existence of SCEs. Comparing the consequences of these examinations with those of the some different models developed earlier in the literature work, showed fantastic exactness of the proposed design model.

Jie Deng et. al.[40], in his second paper, as an expansion of his initially papers, shows a total circuit dense model for a SWNT. Proposed model is comprehensive circuit suited CNT based FET model and is actualized utilizing hspice. The model considers different non idealities, similar to the flexible scattering in the channel, the resistive S/D parasitic resistance, SB-resistance and the different parasitic capacitances (Figure 2.4).

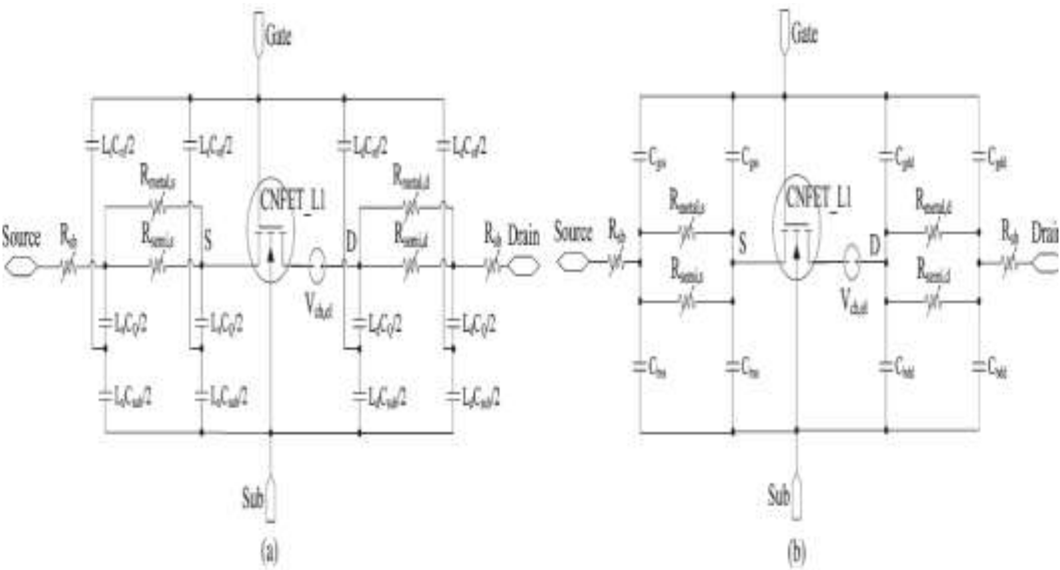


Fig. 2.4: (a) Six-capacitor (b) Four-capacitor models for CNT based FET [40]

Gaurav et.al. [78] introduce different parts of semiconducting device qualities and Mixed mode circuit behavior of Si and Ge NW based MOS based FETs have been examined. Essential parameters, for example, transconductance, o/p conductance, Ion/Ioff proportion and SCE parameters have been obtained and compared for Si and Ge. Simulation of assorted mode circuit has been made for transient examination of inverter and 3 phase ring oscillator. Consequences of these simulations give bits of knowledge into the circuit behavior of these future age devices.

Lan Wei et.al.[79] introduced a systematic model of a characteristic CNT based FET. Carriers of the channel are examined by utilizing the ballistic transport presumption. The surface potential model created is non iterative and utilizes logical electrostatic model and piecewise quantum capacitive model. The proposed design is effective and results in quick circuit simulation and optimization of system. The model captures SCEs like DIBL and quantum capacitance with reasonable precision.

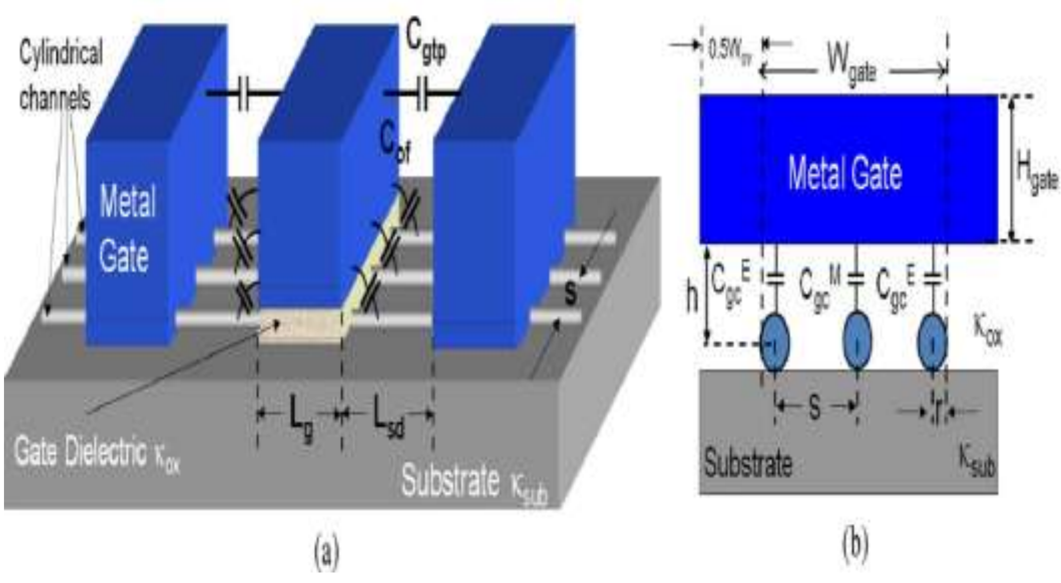


Fig. 2.5: (a) Multiple conducting one dimensional channels. (b) Cross section of CNT based FET

In paper [80], model of an atomistic quantum transport simulation to evaluate the performance of CNT arrangement transistors within the sight of functional non-perfect impacts is proposed. It demonstrates that the non-perfect factors in the manufacture process can significantly influence the performance of carbon nanotube

array field effect transistor. In order to increase the I_{off}, the standard deviation of nanotube diameter dissemination is 0.24nanometer, which raises the static power consumption and decrease on-off current proportion. From proposed work it is discovered that the off-current may be expanded by an order of magnitude when diameter changes is expandes by 0.24 nanometer, which increased the static power utilization and reduce on/ off current proportion. A little factor of metallic type carbon nanotubes in the channel may essentially demean the on/ off proportion. Misalignment of the carbon nanotube orientation influences the on/ off current in short channel semiconducting devices.

Roberto Marani, et al. [81] displayed a CNT based FET design which is simply implementable in SPICE simulation. The proposed models are compared with that model accessible on the web and with exploratory information. They have watched a generally little mistake of under 5% in both the cases. They have checked their model by outlining and building up an analog to digital converter circuits. The model has performed well at the circuit level. A CNT based FET based CS amplifier has been composed and created utilizing the proposed CNT based FET model.

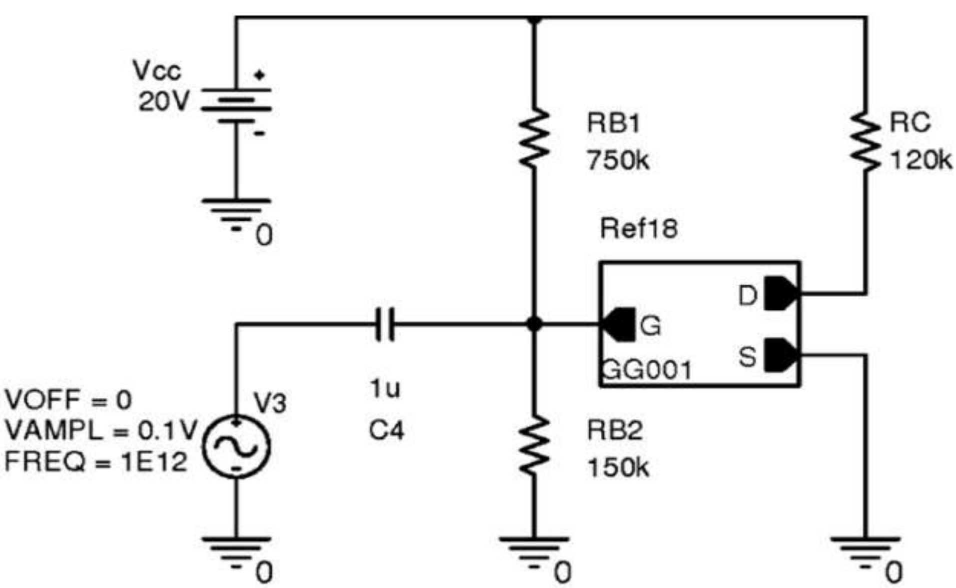


Fig. 2.6: CNT based FET amplifier in CS configuration[81]

Jeong et.al. [82] investigates the current - voltage qualities calculated from NW capacitor, that has been created by associating in parallel a huge no. of identically

prepared NW based field effect transistors. The ascertained capacitance data are compared with planar metal oxide semiconductor capacitor. In the paper the current-voltage information measured from NWCAP and examined the gate response of undoped and floating channel. Moreover, the NWCAP is appeared to display superior channel reversal compared with the traditional planar MOSCAP. So, the performance of NW based field effect transistor could be extraordinarily enhanced with the process refinements created in S/D regions.

Sheng Lin et al. [83] outlined CNT based FET based ternary logic gates. These gates are promising other options to the traditional logic gates bringing about power efficiency and minimized designing. Simulation study utilizing SPICE disclosed that the designed ternary logic consumes less power so results have little postponements in comparison to the traditional innovation.

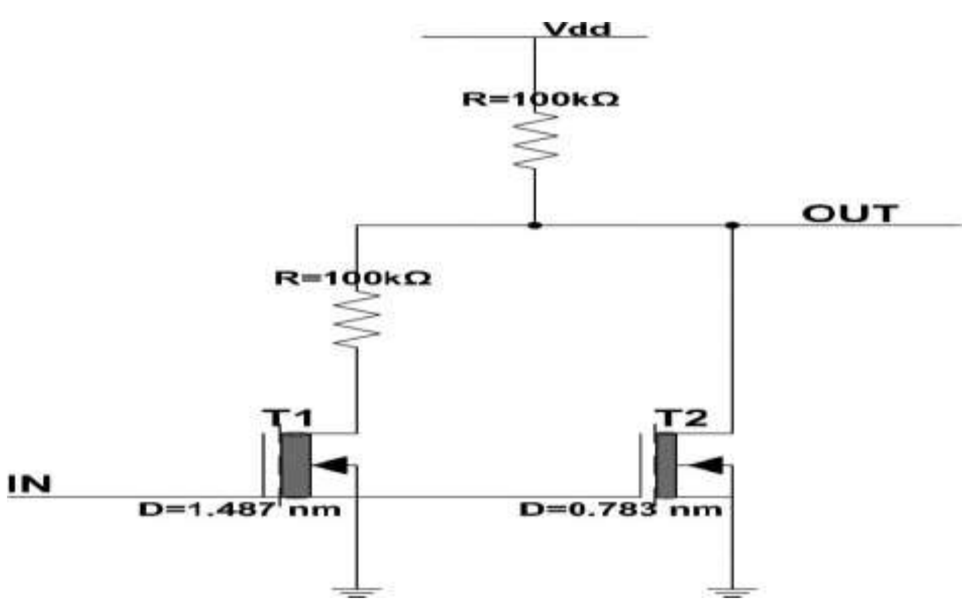


Fig. 2.7: CNT based FET based STI

Hidenki Tsuchiya et.al.[84] researched the performance possibilities of Si NW and semiconducting type GNR based MOS based FETs utilizing first principles band structures and ballistic current estimation based on the "top of the barrier" demonstrate, coming about silicon nanowire based MOS based FETs show a solid orientation dependence through the atomistic band-structure impacts, and [110] oriented silicon nanowire based MOS based FETs enhanced in shorter intrinsic

device delays than silicon ultrathin-body MOS based FETs if size of wire is scaled shorter than 3 nanometer. Besides, graphene nanoribbon based MOS based FETs displayed promising device performance if width of ribbon is composed larger than a few nanometers and a limited band gap may be set up. We have explored the performance possibilities of Silicon -UTB based MOS based FETs, Silicon nanowire based MOS based FETs, and semiconducting graphene nanoribbon based MOS based FETs by considering the first-principles band structures in view of the DFT strategy.

M. Bagherizadeh et. al.[85] has additionally composed and simulated new, low-power and high speed unique F/A adder cells utilizing CNT based FET. It is watched that the proposed design adders consume less power bringing about less delay in comparison the traditional innovation based adders.

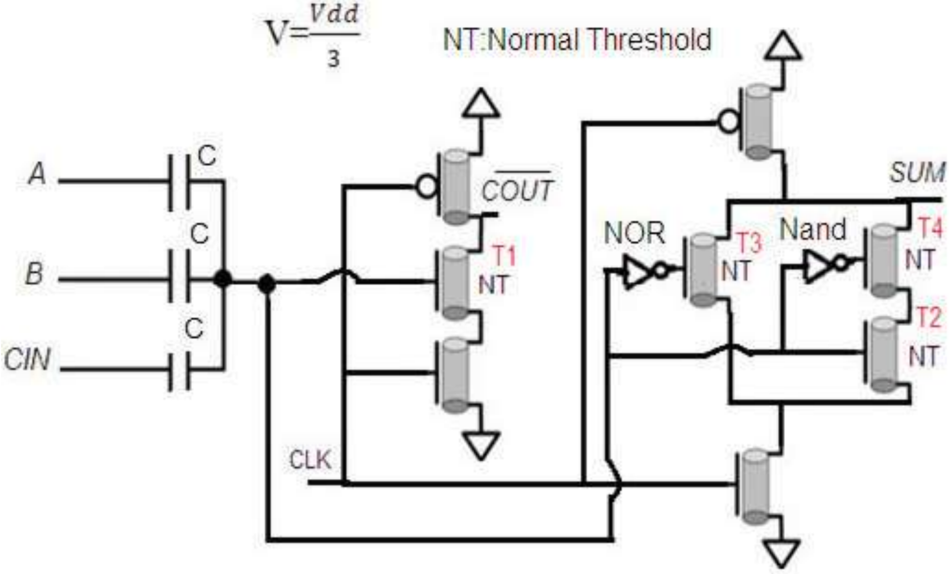


Fig. 2.8: Proposed CNT based FET based F/A

Saurabh et.al.[86] clarify, a total minimized model for carbon nanotube based transistors and interconnects have been explored. Since it doesn't include iteration based answers to calculate the charge and current, it is reasonable for undertaking huge scale circuit simulation. It result rises the extent of diagnostic design research utilizing carbon nanotubes. The models are adaptable with procedure and outline parameters and show huge precision when contrasted with numerical simulationa and

in addition estimation information. As an exhibit, the proposed models have been utilized for circuit simulation to benchmark the performance of carbon nanotube based transistors with 22nanometer bulk complementary metal oxide semiconductor transistors. Carbon nanotubes have the ability to outperform complementary type MOS transistors in both analog and digital fields, expecting that high level combination and procedure related difficulties are met. The model fills in as a standout amongst the most vital bridges betwixt carbon nanotube procedure and design, in this way bit of knowledge into the improvement of carbon nanotube based electronics.

Fabien Pregaldiny et al.[87] have outlined an analog frequency frequency doubler circuit utilizing both unipolar and ambipolar CNT based FETs. This type frequency doubler circuit utilizes the symmetry of the CNT based FET ambipolar response. The frequency of output signal in the model is double the frequency of the input signal, as expected.

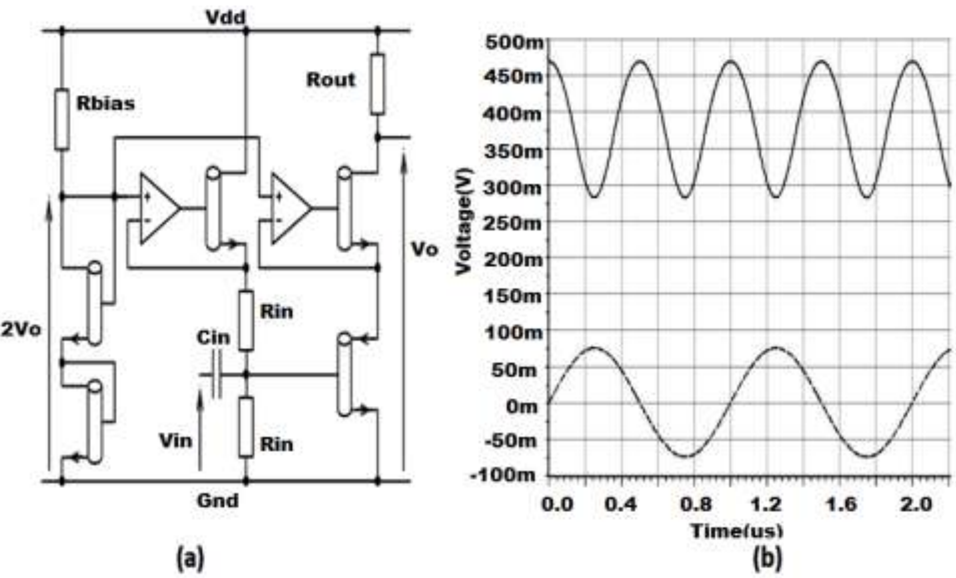


Fig. 2.9: (a) Carbon nanotube based Frequency doubler (b) Response of Frequency doubler

In paper [88], the performance of NW crossbar-based logic circuit is investigated, as far as territory, delay, and power, and we compare them and their MOS based FET counterparts. This was demonstrated that NW crossbars don't scale well in

implementing logic circuitry and faster NW field effect transistors are basic to the skill of nanowire crossbar logic circuits. On analysis and comparison, we propose a crossbar cell design utilizing small NW crossbars which may be manufactured with existing nano imprinting and lithography techniques. This outline is perfect with the traditional MOS based FET manufacture and design methodology. Utilizing logic synthesis tool SIS, we show that crossbar cells may be used to improve the performance of conventional standard cell-based integrated circuits. Results with the MCNC91 benchmark suite demonstrated that the joining of crossbar cells altogether lessened circuit area by 75% and power by 66% while delivering similar speed under area improvement. The outcomes likewise demonstrated that the utilization of crossbar cells enhances speed, power, and area by 5%, 9%, and 18%, separately, under speed improvement.

Derycke et al.[89] has demonstrated practically that n-sort CNT based FETs may not be realized by doping just rather a basic annealing of single wall nanotube based p type field effect transistors in a vacuum will create the n sort CNT based FETs. They utilized this strategy to fabricate first carbon nanotube based logic gates, voltage inverters. They additionally utilized spatially settled doping in implementing logic function on a single carbon nanotube package.

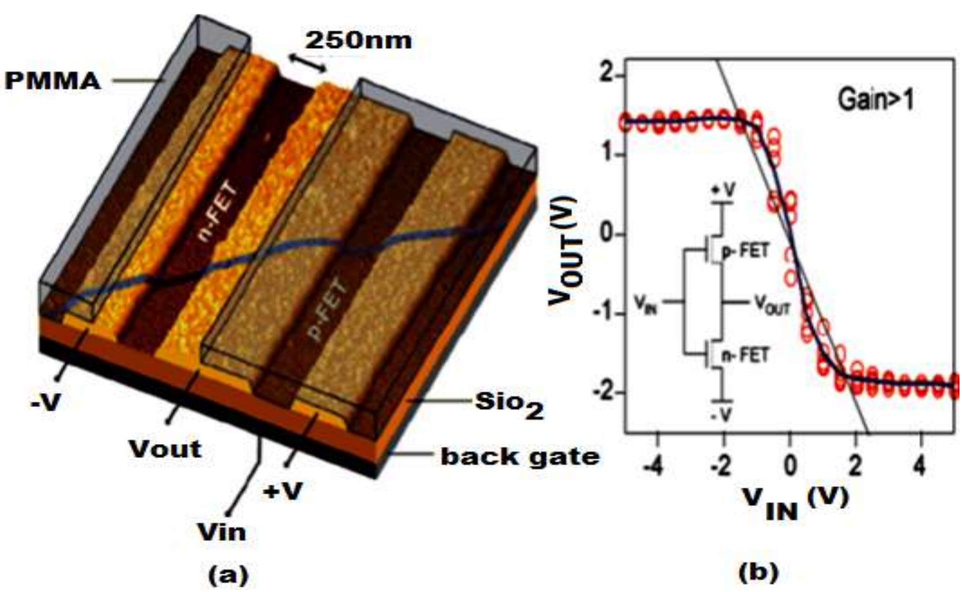


Fig. 2.10: (a) An intra-molecular logic gate (b) Features of the intra-molecular voltage inverter

In paper [90], temperature dependent transport estimations of cylindrical shaped GAA SNW P type MOS based FETs is proposed. Single hole tunneling conduct are seen at 4.2 K, and one of the devices displayed abnormally solid current peaks , that survived even at room temperature. The division betwixt two tops with indistinguishable shapes relates to the energy of 25meV to 26 meV. This esteem was stable with the entirety of the bound state energy spacing of boron atom and the single hole charging energy of a point with 3 nanometer radius. The radius is additionally tantamount to the Bohr radius of a solitary acceptor atom when the light hole compelling mass is utilized.

Yang et.al.[91] Presents temperature reliance of the qualities of a Si NW based SB MOS based FET device and is explored in detail. Palladium and titanium source and drain silicon NW type MOS based FETs coordinated with an Al_2O_3/TaN/Ta gate stack is created and described at various temperatures. Results demonstrate that schottky barrier silicon nanowire MOS based FETs work with various standards, compared to traditional MOS based FETs. From the I_{ON} and trans-conductance changes with temperature, it is discovered that device operation is ruled via carrier infusion at the interface of the source and channel instead of the carrier transport inside the nanowire channel. Further, the carrier infusion is dictated by the opposition betwixt schottky barrier tunneling and thermionic ejection. Schottky barrier height and width assume an essential part in schottky barrier silicon nanowire MOS based FET operation, and compelling height of barrier has been removed based on I_{DS}– V_{GS} qualities at various temperatures. Along with, the profile of schottky barrier at the source and channel interface was analyzed with a subjective investigation of the sub threshold swing.

In paper [92] we lately probed on CNT based FETs and their attributes and compare the performance of the devices with state of art Si MOS based FETs is performed. By decreasing the gate dielectric film thickness and working with high-k dielectric materials, for example, HfO_2, we viably lessened the operational voltages beneath 1 volt. The electrical attributes acquired, shows plainly superb the device performance in both the on and off-state with of CNT based transistor.

In paper [93], examination on the electrostatics of carbon nanotube based field effect transistors and of Si based SiCNW field effect transistors, 4G RNW field effect transistors and 3G RNW field effect transistors is finished. The examination finished up out at dimensional sizes comparing to the 65 and 45 nanometer ITRS nodes, additionally it completely represents quantum mechanical impacts. At long last the conclusion is that the CNT based FET shows a somewhat better performance as for the SiCNW FET and the 4G RNW FET, because of the joined impact of two particular attributes of the said devices. On the direct, the electron confinement at the surface of the NT improves the adequacy of the gate charge control, then again the charge restriction at the center of the cross section in the Si NWs is responsible for a depletion capacitance in series with C_{OX}, which decreases the effectiveness of gate. Therefore higher the DOS within Si NWs partially compensates for the above impact, and the only a slight distinction in the electron density inside the channel is obvious at each gate voltage.

A reduced model of current – voltage attributes and in addition the device property for a ballistic NW based MOS based FET is proposed [94]. An electrostatic relationship associating the gate overdrive to the density of carrier at the current bottleneck point is inferred, and is joined with the current expression to make a closed current formula of a ballistic NW based MOS based FET. We connected outcomes to a Si NW based MOS based FET with the utilization of the NW sub band parameter gave by a gathering at the University of Bologna. The electric current level ascents to a few tens of μA for the applied bias of a few tenths of a volt. As a matter of fact, the magnitude weakly relies upon the temperature, and the conductance is of the order of magnitude of the quantum conductance. Specifically, the conductance at low temperatures in the straight region is commanded by the quantum conductance. We investigated the sub threshold qualities, and the gate all around structure is shown to yield the perfect S factor of around 60 milli eV/dec if the SCE is ignored. The planar gate structure additionally incorporates the parasitic capacitance related with substrate, thus the estimation of the S factor will debase. Because of the DOS, the commitment of the quantum capacitance in the current equation is identified, and the basic significance of quantum capacitance in the NW based MOS based FET operation is called attention to. Ignoring the capacitance segment causing a genuine over estimation of the saturation current. The real current

magnitude of the NW based MOS based FET is fundamentally controlled by the quantum capacitance when the capacitance of gate is substantial, and the increase of the gate capacitance is such an incapable region for the enhancement of device performance.

Shin et.al.[95] showed the impacts of numerous gates on the enhancement of device performance of schottky barrier MOS based FETs in its definitive scaling limit. We likewise analyzed the stiffness of the CB bending of gate fields, for the most part decides the OFF state attributes in ultra short channel semiconducting devices.In spite of the fact that the band bending solidness is brought by various gates down to some degree, it stays high compared to its counterparts with doped source/drain, leading to fast increasing sub threshold slope with the decrease of the length of channel. Subjective nature of the outcome could be acquired by considering the equilibrium electrostatics just; it likewise recommends that the presence of SB barriers imposes a limit to the enhancement of the OFF-state performance by numerous gates. The ON currents are improved extensively by numerous gates, inspite of the increased size quantization impacts that successfully rise of SBs. The threshold voltage variety with the gate length is impressively suppressed as the quantity of various gates increments.

In paper [96], the simulation of silicon nanowire transistors for radio frequency applications, including the effects of the resistance and the parasitic capacitances is talked about. Because of the ultra narrow Si NW structure, the effects of the parasitic capacitances are important for silicon nanowire transistors. Parasitic resistance actuated by the ultra thin regions of SDE are the major supporter of the aggregate series resistance, it can firmly impact the radio frequency performance of silicon nanowire transistors. Contact resistance, has generally frail impact when compared with the SDE regions. The streamlining of the doping profile in the SDE regions of 10nanometer gate silicon nanowire transistors is explored with respect to the tradeoff betwixt parasitic capacitances and resistance.

In paper [97], a new MOS based FET outline which encapsulates zigzag semiconducting type SWNTs in the channel is watched. Examinations demonstrate the carbon nanotubes have high low-field mobilities, this may be as awesome as

$1X10^5$ cm^2/Vs. Thusly, we expect that MOS based FET performance may be enhanced by inserting carbon nanotubes in channel. To enhance the performance of a lately proposed carbon nanotube based MOS based FET device, we proposed another theory which associates carbon nanotube modeling to MOS based FET simulations. It is demonstrated that by framing huge mobility regions in channel, MOS based FET performance may be helped. Still, barriers betwixt carbon nanotube and Si because of the changes of band gaps and electron affinities will debase MOS based FET performance improvement. Our computations were gotten by making on our present carbon nanotube Monte Carlo simulator and quantum based device solver.

In paper [98], a quantum simulation of SNW FETs was implemented in the frame work of the effective mass hypothesis, in which the 3 D Poisson condition were resolved self-consistently with the mode-space non-equilibrium Green's functions conditions in the ballistic transport regime. The semiconducting device performance on the gate length and width for 3 sorts of gate setup has been examined; mostly aim on the contribution of the tunneling current to the total current. This additionally researched quantitatively the impacts of gate under lap and the corner rounding of Si body on the semiconducting device performance, inferring that the gate underlap is an essential factor in enhancing the subthreshold qualities of device. The corner rounding of Si body isn't a critical factor, for the devices with Si body width of a couple of nm.

Wang et.al.[99] noticed the scaling of NWTs to 10 nanometer gate lengths and underneath. The two dimentional scale length hypothesis for a cylindrical surrounding gate MOS based FET first, along these lines yielding a general rule betwixt the gate length and the NW size for satisfactory SCEs. Quantum confinement of electrons in the NW offered rise to ground-state energy and, thus a threshold voltage reliant on the radius of the NW. The scaling boundary of NW transistors calls attention to how exact the NW size can be controlled. The performance boundary of the NW transistor is evaluated utilizing applying a ballistic current model. Key issues i.e. the DOS of the NW material is talked about. Comparisons are made betwixt the model outcomes and the published experimental information of NW devices.

Iqbal et.al.[100] gave a broad numerical investigation of p-sort AMOSFETs, basic field effect transistor devices character are clarified by highlights that incorporated a single doping sort, ohmic contacts, and an incompletely gated intercontact region. The examination likewise introduced high quality transistor performance that relies upon achieving controlled S/D region lengths. The estimations of which rely upon the contact-height barrier and doping, and this needed a minimum gate region length. Unlike to MOS based FETs and TFTs, I_{ON} of the A-MOSFET rises firmly with the doping density of the active region. It likewise demonstrated poor reliance on the gate capacitance. Dissimilar MOS based FETs and TFTs, the length of the gated region may be resolved from the threshold voltage and the sub threshold swing; e.g., the sub threshold swing is debased as the gate length obtains smaller. The length of the gated region obtained impacted by the saturation behavior, and the A-MOSFET setup behaves as a basic resistor for short gate lengths.

In paper [101], the electrical properties and in addition the performance for low and high mobility 80 nanometer carbon nanotube models are compared, checked and observed to be in great concurrence with exploratory information. The mobility of high mobility model is twenty times that of the low mobility model with carrier conc. Low DIBL in the high mobility model is just to demonstrate that the threshold voltage is less dependent on drain bias voltage. The SCE is effectively controlled well in the high mobility model. In the low mobility model, high drain induced barrier lowering model displays a decreased threshold voltage due to the large drain bias voltage, so decreasing the hindrance height at source end of the channel. The high mobility model has quicker transient turning in ON and OFF states as compared to the low mobility model because of its steeper SS. Three times higher I_{on} and I_{off} proportion in the huge mobility model compared to the low mobility models so having outstanding electrical attributes of short channels.

In paper [102], the capacity of ANN approach for the modeling and simulation CNT based MOS based FETs is examined and explored. A numerical model of the C-V qualities depend on the two dimensional numerical NEGF simulation by methods for moscnt.1.0. From the numerical model, we got the expected database to streamline the proposed artificial neural network model. The comparisons are made betwixt NEGF simulation and recommended artificial neural network model. Examination

concluded that there is a outstanding agreement betwixt the numerical and anticipated esteems with minimum error.Artificial neural network model is significantly speedier than NEGF simulation.This implies that the proposed show is an exact and in addition quick estimation of NEGF model. With these highlights, we imported the neural based model carbon nanotube based metal oxide semiconductor field effect transistor in HSPICE s/w. Thus inferred that the model is a productive apparatus for simulation of nanosize circuits.

Paolo et.al.[103] exhibits new investigations concerning gas sensors in light of CNT based FETs. In spite of the fact that the devices have enabled us to acknowledge sensors with high affectability when compared to existing advances, yet the physical explanation of the interaction betwixt the gas atoms and the CNT based FETs has not been defined. We attempted to discover some consistency betwixt the physical explanations given by the different scientific groups working on the subject and to answer some unsolved inquiries. Additionally, considering selectivity be the chief issue, distinctive routes are investigated which have been proposed to beat this issue: functionalization utilizing polymers, diversification of the S/D metal electrodes, metal beautification of single wall carbon nanotube mats, exploitation of the desorption time of the diverse gasses. For every system we tried to assess the advantages/disadvantages.

In Rahman et. al.[104], novel three stage operational intensifiers (3SOA) are outlined and analyzed. The proposed 3SOAs utilizes 45 nano meter techonology CNT based FETs and the conventional MOS based FETs. The proposed structures are hybrid in nature, as they utilize conventional MOS based FETS and in addition CNT based FETs. The simulation study demonstrated a remarkable progress in DC gain, o/p resistance and power consumption in proposed hybrid devices in contrast with the conventional devices. It has been found that by differing the quantity of carbon nanotubes, the performance of the given 3SOAs may be optimized further.

M.Nizamuddin et. al.[105], designed and did calibrated simulation of CNT based FET based COTA. Three structures of CNT based FET based cascade operational transconductance amplifiers were simulated utilizing HSPICE and it has been compare to traditional complementary metal oxide semiconductor based cascode

operational transconductance amplifiers. The simulation work uncovered that the CNT based FET based cascade operational transconductance amplifiers fundamentally outperformed the traditional MOS based FET based cascode operational transconductance amplifiers. We accomplished huge increment in dc pick up, o/p resistance and SR of 81.4%, 25% and 13.2%, separately, in the proposed pure carbon nanotube based cascode oprerational transconductance amplifier in comparison to the traditional complementary metal oxide semiconductor based cascode operational transconductance amplifier. The power utilization in the pure CNT based COTA is 324 times less as compared to the traditional complementary based cascode operational transconductance amplifier. Moreover, the P.M., gain margin, common mode rejection ratio and power supply rejection ratio have notably rised in the proposed carbon nanotube based cascode operational transconductance amplifiers as comparison to the traditional complementary MOS based cascode operational transconductance amplifiers. Moreover, to watch the benefits of cascading, the proposed CNT based COTAs been compared with CNT based OTAs. By joining the idea of cascode in the CNT based FET based operational transconductance amplifiers, huge increments in gain (12.5%) and o/p resistance (13.07%) have been accomplished. The performance of the proposed COTAs has been additionally enhanced by changing the quantity of carbon nanotubes, pitch of carbon nanotube and diameter of carbon nanotube in the CNT based FETs utilized. In this way it is reasoned that the performance of the proposed cascode operational transconductance amplifiers may be essentially enhanced by utilizing ideal estimations of no. of carbon nanotubes, pitch of carbon nanaotube and D_{CNT}.

In paper [106], the simulation study has investigated that the carbon nanotube based operational transconductance amplifiers, especially the pure CNT based OTA has outperformed the bulk complementary metal oxide semiconductor generously. It is nothing but an enhancement all simulated performance parameters. The DC gain has been enlarged by 218%, SR has enlarged by 22.58%, and o/p resistance has additionally been enlarged by 55.2% in the pure carbon nanotube based operational transconductance amplifier compared to the traditional complementary MOS based operational transconductance amplifier. Moreover, power consumption is less in the pure carbon nanotube based operational transconductance amplifier.

In paper [107], VLSI innovation is being embraced generally these days for biomedical applications to enhance human services conclusion, checking and cure. Analog devices, for example, analog to digital converters for biomedical applications can be of unobtrusive accuracy however should be extremely energy efficient for a considerable length of time. CNT based FET may be the future substitute to be utilized in different high performance, low power semiconducting devices. In this work we have displayed a low power CNT based FET based two stage operational amplifier for biomedical analog to digital converters. A S/H circuit is additionally implemented utilizing CNT based FET based operational amplifier to be utilized as a part of biomedical analog to digital converters. Simulation consequences of CNT based FET based circuits are compared with MOS based FET semiconducting circuits. Results show enhancement of power consumption up to 80%. The proposed circuit simulations are completed in HSPICE. This is presumed that CNT based FET based circuits can be prime decision for low power based applications.

In paper [108], the acknowledgment of a developing progressive process innovation for circuit and system simulation depends notably on (1) special device characteristics given by the innovation, (2) an authentic creation process, and (3) an appropriate transistor compact model for the circuit design and simulation. Carbon nanotube based field effect transistors belongs to a category of rising advances for one dimensional semiconducting electronics which may can possibly supplant a current semiconductor process innovation because of their remarkable inherent properties, particularly in the domain of high frequency analog type circuit applications, for example, mixers, amplifiers and mixers. The current advance in CNT based FET process innovations has enlarged the demand for reasonable miniaturized models. The paper concentrates on the utilization of a lately growth physics based compact model TCAM for the design of analog high frequency circuits. Besides, the effect of vital CNT based FET innovation parameters on the conduct of chose high a frequency benchmark circuit is examined.

In paper [109], a newly logical model in view of the Wentzel-Kramers-Brillouin estimation for MOS based FET like, one dimentional ballistic transistors with SB contacts has been produced for the drain current. By utilizing an appropriate estimation of the Fermi-Dirac distribution function and transmission probability, an

investigative answer for the Landauer integral was obtained, which controls the limitations of available models and increases their pertinence toward high bias voltages required for simple applications. The simulations of o/p and transfer qualities are established to be in concurrence with the exploratory information for sub-10 nano meter CNT based FETs.

In paper [110], CNT based FETs are expected to have many benefits over Si based field effect transistors. While the majority of the literature manages digital applications, the paper provides a review on the current status of CNT based FET innovation for RF analog applications, including the respective requirements. Results for transistors and circuits accomplished so far and in addition possible fabrication approaches for performance advancement are examined.

In paper [111], a carbon nanotube based operational amplifier has been designed utilizing an 8 T operational amplifier benchmark model and the operational amplifier's performance has been inspected with the changes of the quantity of single wall nanotubes utilized as a channel region of the CNT based FETs. A simulation based appraisal of the impact of enlarged NTs in the channel region is done, showing a progressive enhancement in all the feature performance parameters of the carbon nanotube based operational amplifier in comparison to the traditional silicon based complementary metal oxide semiconductor based operational amplifier. An intense change in B.W. by 146% and a decrease in power utilization by 327.22% has been accomplished for a 5 tube CNT based FET based CNT based operational amplifier proposing CNT based operational amplifier as a more acceptable device for analog and mixed signal operations in future nanosized circuitry.

In paper [112], the relationship of CNT based FET and flexible resistive devices is examined to actualize programmable logic utilizing neural systems. A learning cell, in view of switched capacitors guideline, is composed with a specific end goal to apply a simplified learning rule to program the resistances related to each synaptic weight of the network. Electrical simulations approve the importance of such approach.

2.3 CONCLUDING REMARKS

In this chapter, carbon nanotube based electronics circuits (analog type and digital type circuits) composed till date is discussed. It features the imperative focuses about the best in class identified with the proposed circuits.

CHAPTER 3
ANALYSIS OF CNT BASED FET

This research work investigates the experiences of the utmost extraordinary utilization of CNT in electronic field, CNT based FET. The inspiration of research in CNT based FET is fuelled by the novel electrical attributes of CNT specially semiconducting feature. Furthermore, the continuous attempt to discover future nanoelectronic semiconducting device which may perform as magnificent as MOS based FET likewise push the exploration of CNT based FET to be further forceful. The initial segment describes an outline of the conformation of CNT based FET followed by the clarification of CNT based FET operational as a semiconducting switching device. The following segment gives the comparison amongst CNT based FET and MOS based FET. In this chapter a comparison is being made between conventional MOSFET and different types of CNTFETs. And finally concluded a future replacement of MOSFET. The major difference in CNTFETs and MOSFET is that it has CNT in channel instead of Silicon. CNTFETs show improved characteristics with scaling of technology. Chirality and diameter of CNTFET directly affects its bandgap which is the biggest advantage over MOS based FETs. Study of various types of CNTFETs is made and a comparison is made in this chapter.

3.1 INTRODUCTION

The supply of portable semiconducting devices need that the whole system – many innovation, analog, digital and many signal ought to be realized on one substrate, SoC. The SoC must be power, area and speed proficient along extensive usefulness to understand a superior convenient device. Different innovations have been utilized to realize high efficient system on chips, be that as it may, complementary CMOS innovation is a faithful. Complementary MOS gives low power, huge NM and is most appropriate for the realization of high integration level circuits. In any case, complementary MOS has severe constraints as the device size is nanorange. The scaling of MOS based FET beneath 32nanometer / 22 nanometer is very tough due to SCEs, increment in leakage power and sensitivity to process varieties in integrated circuits producing etc. So, the design of vigorous complementary MOS circuits is winding up to a great degree troublesome and significant when the MOS

measurements are in nanoscale. In this way, there is a quick need of new device structures that can supplant the traditional MOS based FET and can broaden the scalability of MOS based semiconducting devices underneath 22 nanometer /18 nanometer node. Although, the novel semiconducting device must surpass the present solutions, must empower newly uses and its outcome in a huge price diminishment. A newly material and its related semiconducting device that can possibly supplant silicon and complementary MOS and can broaden the scalability of devices underneath 22 nanometer is CNT and its related transistor, CNT based FET. Carbon nanotube has remarkable properties which makes CNT a faithful future material. Correspondingly, CNT based FET is a promising essential building block to supplement the current Si based MOS based FET and can bring about the augmentation of the legitimacy of Moore's law further.

3.2 STRUCTURE OF CNTFET

The structure of CNT based FET basically look likes the strucure of MOS based FET with the exception of that the Si channel is changed by the CNT. However, the arrangement continues changing with a specific end goal to enhance the device performance. The present segment, the structure of CNT based FET will be talked about. The structure may be arranged as back gated type CNT based FET, top gated type CNT based FET and of late another structure has been started known as vertical type CNT based FET. The advance in Si innovation keeps on running on the memorable pace of Moore's Law, yet the finish of the device scaling now has all the earmarks of being just ten to fifteen years aside. So, this is of intense enthusiasm to seek newly, sub-atomic scale devices that may backup a central Si stage by giving it new possibilities or that may even substitute existing silicon innovation and allow device scaling to proceed to the atomic scale. When the dimensions of device reach the nano-range, newly possibilities emerge from exploiting the chemical and physical attributes at the nanosize. The intrinsic physical properties like density, conductivity and chemical reactivity of bulk materials (example, a copper wire, a cup of water) are independent of their sizes [1-15]. Nanostructures are especial as compared with both individual atoms/molecules at the macroscopic bulk materials and at a smaller scale. They are known as mesoscopic structures. Research of Nanoscience focuses on the extraordinary properties of nanorange structures and materials which are not exist (or exist only very weakly) in structures of identical material composition but at other

scale ranges. Molecular Electronics with Carbon Nanotube is the future of electronic circuits [43-49, 67, 113-115]. At first, carbon nanotube field-effect transistors were straightforward devices made by depositing SWCNT (synthesized via laser ablation) from solution onto oxidized silicon wafers that had been pre-designed with platinum/gold electrodes. Electrodes performed as source with drain, associated through the CNT channel, and the doped silicon substrate done like the gate. But now several other techniques are being investigated for fabrication of CNTFET. Gas-phase catalytic growth of SWNTs from carbon monoxide is crutial for CNTs [116-119].

3.2.1 The Back-Gated CNTFET

Tans et. al. [120] for the first time demonstrated CNTFET in 1998 to demonstrate an innovatively exploitable exchanging conduct and denotes the beginning of CNT based FET research advancement. They managed to adjust the conductivity higher than 5 times of magnitude by applying electrical field to the CNT [113].

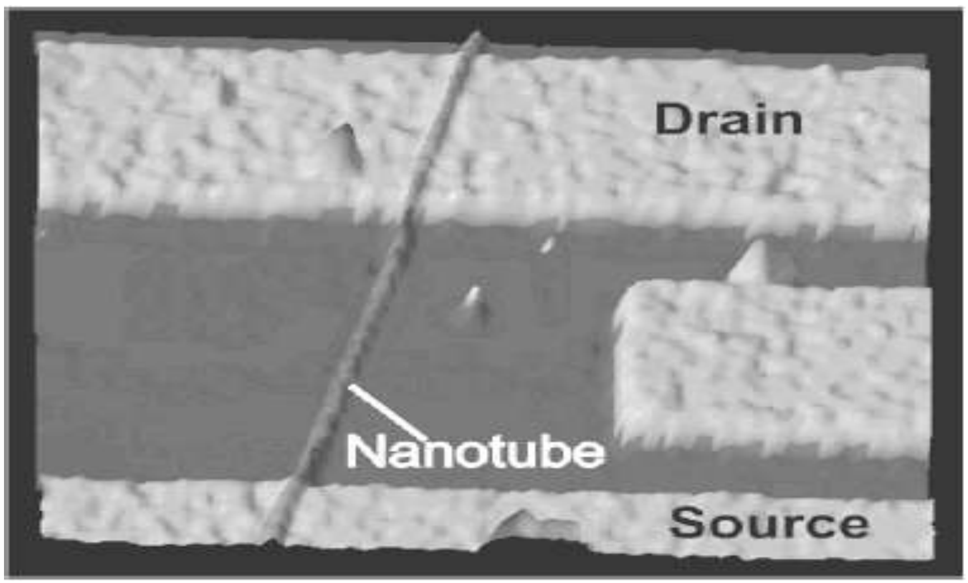


Fig. 3.1: Back-gated CNTFET [184]

Most of the earlier CNTFET devices were back-gated with very thick gate insulators manufactured of SiO_2 roughly around 100 nanometer to 150 nanometer [42]. The structure utilized a non local back-gate with CNT side attached to noble metal electrodes[121].A kind of metal which opposes the assault of acids and different reagents, does not corrode as well is called as Noble metal. The back-gated CNTFET

and the schematic of back-gated CNTFET are given in Figure 3.1 and Figure 3.2 separately.

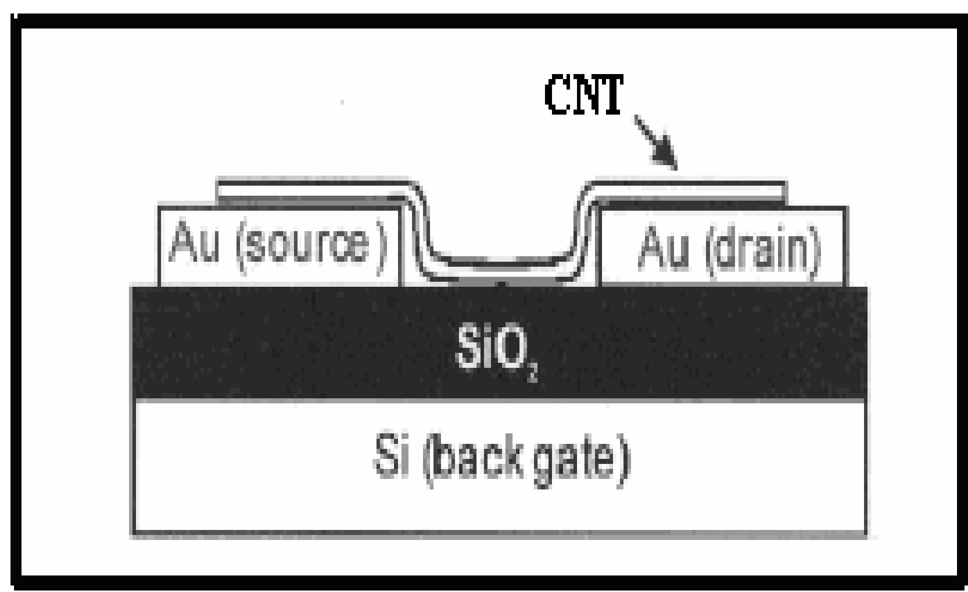


Fig. 3.2: The schematic of back-gated CNTFET [184]

This untimely development brings about poor qualities like little drive current, low transconductance (10^{-9}S) and huge contact resistances (>1MΩ) [67]. As the CNT is just simply laid on the gold electrode, the bad contacts and feeble vander waals force lead to the unsuitable attributes [42].The performance may be enhanced by enlarging the capacitance of gate by diminishing the thickness of insulator or broadening the dielectric constant. Though, the capacitance of gate computation of CNTFET is distinct from MOS based FET. The beginning of Al_2O_3 layer over designed Al gate is capable to lesser the voltage of gate and raises the transconductance [113]. Also enhancement is followed by the initiation of top-gated structure. In order to have a complex integrated circuit each CNTFET is need to be gated individually.

3.2.2 The Top-Gated CNTFET

The coming generation of CNTFET came in top-gated structure that improved the device performance. The newly structure is anticipated to bring better achievements as the performance of back-gated structure is very poor in terms of device operation. Also the structure is created by dispersing the CNT on an oxidized wafer [42]. AFM picture is utilized to recognize the SWCNT and after that the source/drain terminals,

which made of Ti, are created over the CNT. A gate dielectric film about 15nm-20nm is deposited at 300°C via CVD process. Ultimately, utilizing lithography a 50 nanometer-thick gate electrode is patterned. Figure 3.3, represents top-gated CNTFET.

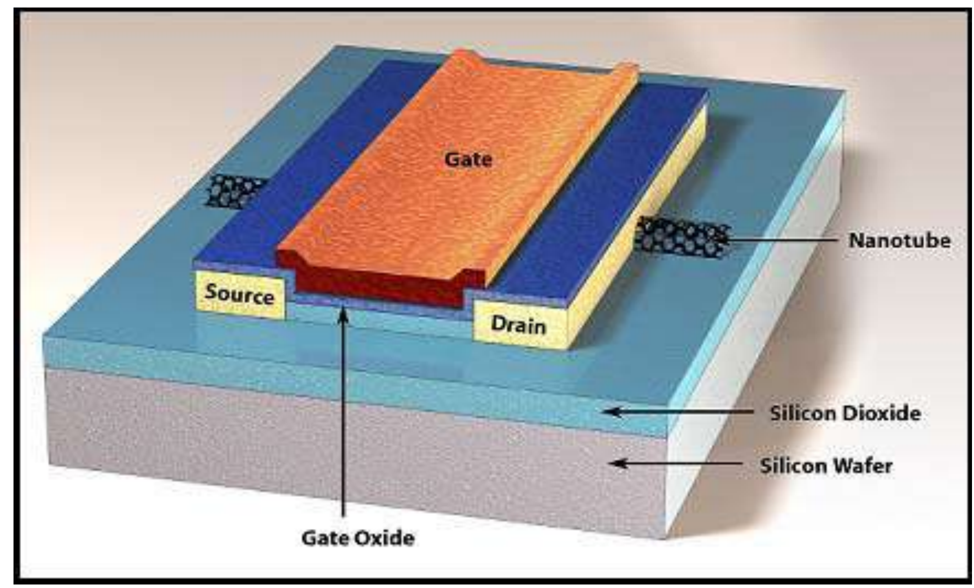


Fig. 3.3: Top-gated CNTFET [184]

The structure offers preferable out-turn in comparison to earlier structure. The enhancement comes from the scaling of the measurement and the attainment of superior device geometry as well as the device performance [121]. For e.g. the electrical field is enlarged because of the device geometry and contact resistance is decreased by picking an appropriate of contact material. Besides, V_{th} is wholly less than back gated structure, drive current is substantially higher and transconductance is comparatively high (3.35µS for each CNT).

3.2.3 The Vertical CNTFET

Vertical CNTFET is the latest development that has been reported in field of CNTFET progress. Choi et. al.[122] proposed the structure with surround-gated in 2004. Size of the transistor may be as little as the cnt's diameter that fits to tera-level CNT based FET and density of 10^{12} components for every cm^2. The developing of vertical CNT based FET incorporates the inevitable steps: nano-pore arrangement by anodization took after by synthesizing the CNT, metal-cathode development, oxide

deposition and designing and in conclusion gate electrode development. The structure of vertical CNTFET is given in Fig. 3.4.

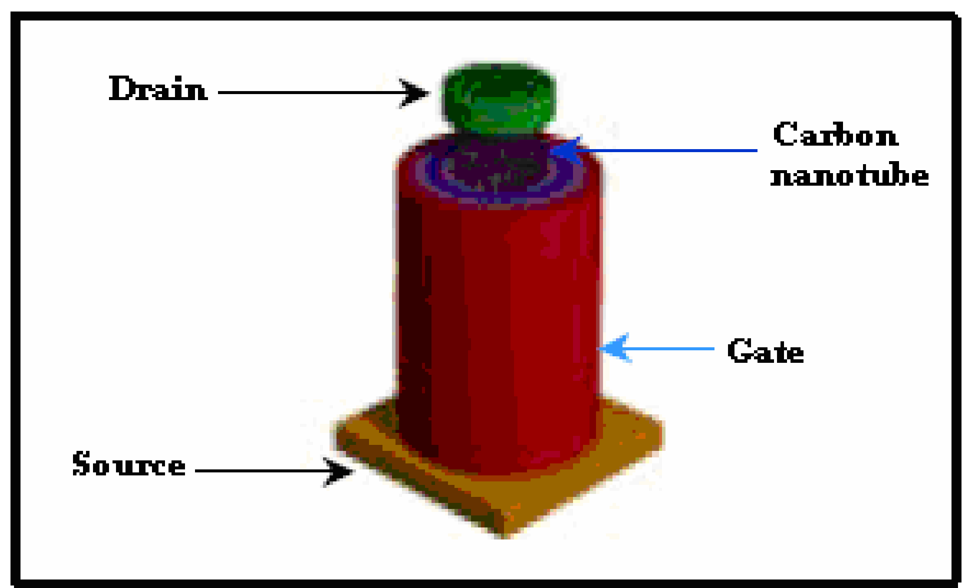


Fig. 3.4: Vertical CNTFET [184]

In the above structure, every CNT is electrically joined to base electrode, source, upper electrode, drain and gate electrode is put around the CNT. Every cross point of S/D electrode compares to a transistor component along a single vertical carbon nanotube. The hole-diameter across of gate oxide determines the quantity of CNT in transistor. The vertical CNT based FET grants higher packing densities which may be accomplished since S/D areas can be organized on top of each other [113].On the other way, since the active devices are never again bound to the surface of mono-crystalline silicon wafer, genuine three dimensional structures can be construct feasible. The vertical view of CNTFET is appeared in Figure 3.5.

3.3 OPERATION OF CNTFET

The fundamental guideline operation of CNTFET and MOSFET continues as before, Where electrons are donated by source terminal and drain terminal will gather the electrons. As it were, current is really moving out of drain to source. The gate terminal will control intensity of current in the channel of transistor. The transistor is in off state when no gate voltage is connected. In the accompanying segment, the operation of two distinct structures is talked about. The underlying structure is called SB-CNTFET and

the later one is MOS based FET-like CNTFET. The contrast in the structures of these two CNTFETs is somewhat distinctive however brings about various transistor operation.

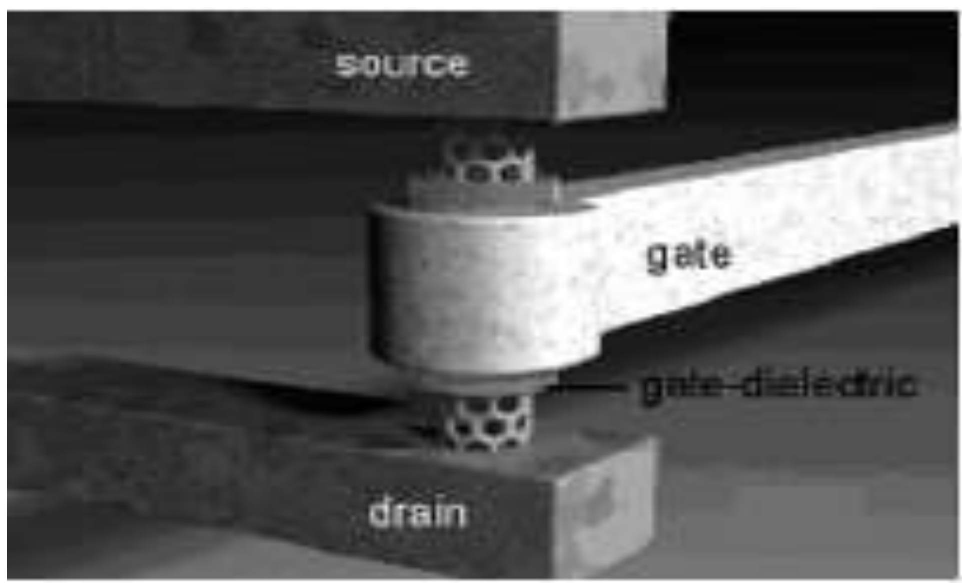


Fig. 3.5: Other view of vertical CNTFET [184]

3.3.1 Schottky-Barrier CNTFET

Schottky barrier (SB), a potential barrier, exists at each contact betwixt metal and semiconductor. The barrier's height is decided by the filling of metal-induced gap states. The states become accessible in the energy gap of semiconductor caused by interface made with the metal. Schottky barrier is managed by the local work functions distinction of metal and CNT. Schottky barrier is additionally colossally delicate to vary of local environment at the contact [41]. Case in point, the gas adsorption differs the work function of metal surfaces. In perspective of the way that the device utilizes metal as its S/D contacts and SB at its terminal contact betwixt CNT and metal, So this is known as SB CNF based FET. SB-CNT based FET is given in Figure 3.6 underneath.

Direct tunneling via the SB barrier at the source-channel junction forms the principle of SB-CNTFET. The gate voltage controls the barrier width and hence the device transconductance depends on the gate voltage. In the channel, enormous barrier limits the current at short gate bias. If the gate bias is enlarged, the width of barrier is lowered, which in turn enlarges quantum mechanical tunnelling via the barrier, hence

an increased amount of current flow in transistor channel. By regulating the transmission coefficient of the device, the transistor action occurs in SB-CNTFET.Schottky-barrier CNT based FET manifests extremely robust ambipolar conduction especially as the oxide thickness of gate is diminshed, even the SB barrier is zero [123].This kind of conduction makes leakage current to increment exponentially with supply voltage specially as diameter of CNT is huge, which brings in controling potential of device. So, in request to enhance the performance of Schottky-barrier CNT based FET, the ambipolar conduction must be reduced.In this direction, one of the arrangements is to enlarge the gate oxide thickness. In the event that the oxide thickness of gate is excessive, hence no ambipolar conduction exists when SB hindrance is zero. The leakage current is, thus, diminished and as a result, the transistor performance is enhanced. The other option is to fabricate asymmetric gate oxide, proposed lately to attenuate the ambipolar conduction [124].The other issue with them that Schottky-barrier CNT based FETs suffer from metal-induced-gap states that restrict least channel length and therefore enlarges S/D. Schottky-barrier CNT based FET is also incompetent to place gate terminal near to source since this can increment parasitic capacitance.

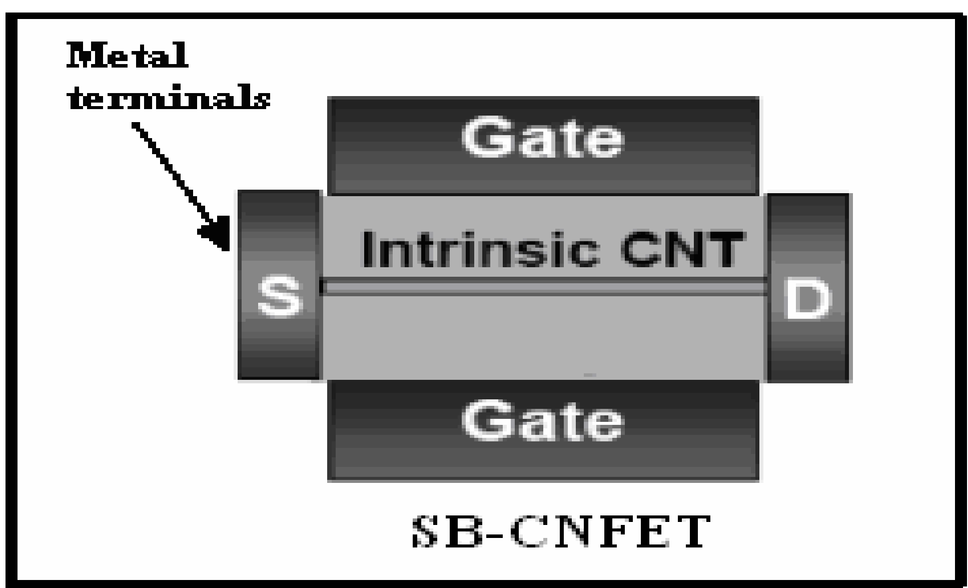


Fig. 3.6: Schottky-barrier CNFET (SB-CNTFET) [184]

3.3.2 MOS BASED FET LIKE CNT BASED FET

MOSFET-like CNTFET have structures slightly different than schottky barrier-carbon nanotube field effect transistor since they use heavily doped terminals rather than

metal. With a specific end goal to manage the issues encountered in Schottky-barrier CNT based FET, these are operated like ordinary MOS based FET.Dissimilar Schottky-barrier CNT based FET, S/D terminals are heavily doped such as MOS based FET and therefore known as MOS based FET-like carbon nanotube field effect transistor. The semiconducting device, as given in Figure 3.7, works on the principle of modulating the hindrance height by gate voltage application. In this condition, I_D is controlled by no. of charge that is induced in the channel by the gate.

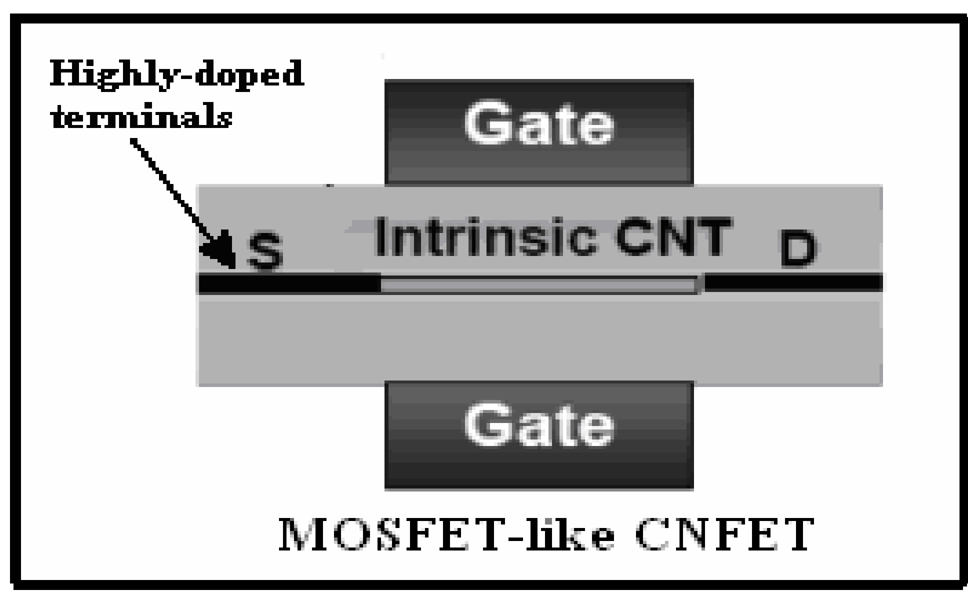


Fig. 3.7: MOS based FET like CNT based FET [184]

These have following advantages over SB-CNTFET: (1) the device is capable to attenuate ambipolar conduction in Schottky-barrier CNT based FET. (2) It likewise gives extensive channel length limit on the grounds that the density of metal-induced-gap-states is essentially decreased. (3) Parasitic capacitance betwixt Gate/Source terminal is altogether diminished and therefore permits rapid operation of the transistor. (4) Speedy operation may be accomplished in light of the fact that length betwixt gate and source/drain terminals may be isolated by the length of source to drain, that diminishes parasitic capacitance and transistor delay metric. (5) It works like Schottky-barrier CNT based FET with negative the SB height amid condition and in this manner it conveys higher I_{on} in comparison to Schottky-barrier CNT based FET.

3.3.3 P-TYPE VERSUS N-TYPE CNTFET

CNTFET are regularly p-type that implies they are adjusting current in the channel when negative gate voltage is connected to the semiconducting device. For p-sort operation, when negative gate voltage is associated, it will lead current in the channel from source to drain and the current is a result of holes movement. On the other hand, a n-sort CNTFET conducts at whatever point a positive door voltage is associated with device, which is current stream in the channel from source to drain is because of the conduction of electrons.To put it plainly, CNTFET conveys current either a positive or a negative gate voltage is associated. The attribute, allowing both holes and electrons conduction in a similar semiconducting device, is known as ambipolar attribute. Thusly, CNTFET is an ambipolar device because this conducts current either in negative or positive supply voltage.

Typically, when carbon nanotube is utilized to create CNTFET with no further preparing, the devices are invariably p-type. Therefore, with a specific end goal to deliver n-type CNTFET, the other process is required. There are two methods for creating n-sort CNTFET from p-sort CNTFET. The change procedure may be build possible by annealing/doping process.

Annealing is a procedure of changing over p-sort CNTFET into n-sort CNTFET via vacuum annealing. In the procedure, p-sort CNTFET is warmed under vacuum to desorb any adsorbed gas, for example, O_2 and toward the finish of the procedure, the p-sort CNTFET is changed over into n-sort CNTFET. The transformation procedure is reversible on the grounds that if n-sort CNTFET is uncovered to air, the semiconducting device will come back to its original p-sort attribute. This way toward annealing is graphically appeared in Figure 3.8 beneath.

The other procedure is in which the p-sort CNTFET is doped utilizing electron donors, for example, alkali metals and is portrayed in Figure 3.9. This is called doping process, Alkali metals, for example, potassium, will give the same outcome as in annealing procedure with p-sort CNTFET is changed into n-sort CNTFET. Transformation procedure from p-sort to n-sort and vice versa is imperative particularly to create CNT based complementary logic circuits. Along these lines this transformation gives a potiential solution for assemble nanotube-based logic circuit following for building complimentary logic circuits both p-sort and n-sort CNTFET are required.

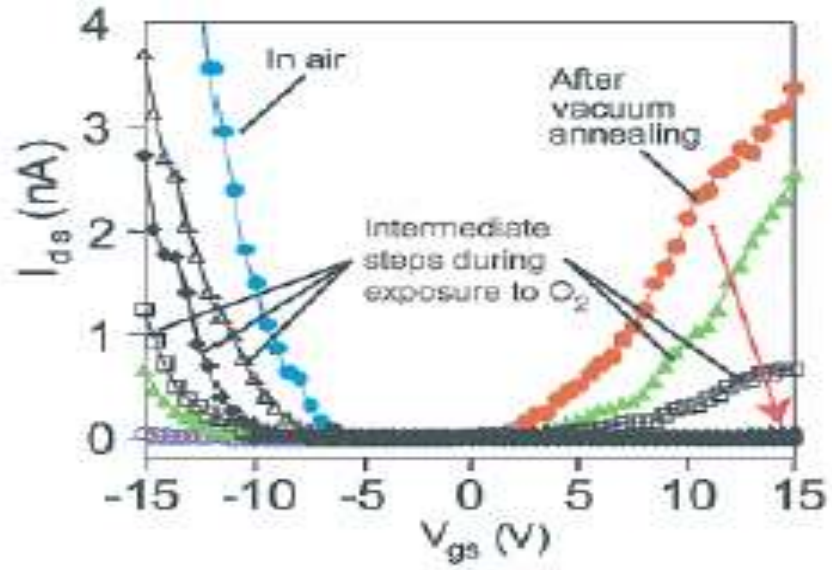


Fig. 3.8: Feature of CNTFET because of annealing process [184]

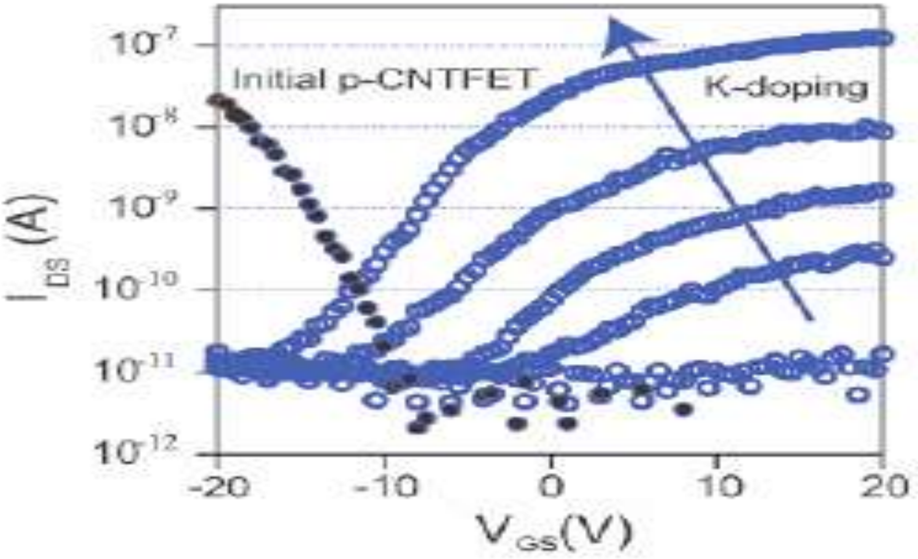


Fig. 3.9: CNTFET feature because of exposure to potassium atom [184]

3.4 COMPARISON BETWEEN CNT BASED FET AND MOS BASED FET

In this segment we have given a brief comparison betwixt the performance of CNT based FET and MOS based field effect transistor.

Simulation Performed For CNTFET Analysis

The alteration of I_d versus V_d and I_d versus V_g at 0.1nm diameter,0.2nm diameter and 1nm diameter shown in fig. 3.10, fig. 3.11, fig. 3.12 separately. Chirality and diameter, of CNT based FET is affects its band gap, which is the biggest advantage

over MOSFETs. Study of various types of CNTFETs is made and a comparison is made in this work.

Table 3.1: Technology Parameters of CNTFET

S. No.	Parameter	Value
1.	Thickness of Oxide	4 nm
2.	Length of Physical Channel	45nm
3.	Supply	0.9 V
4.	Gate Dielectric	HfO_2
5.	Dielectric Constant	16

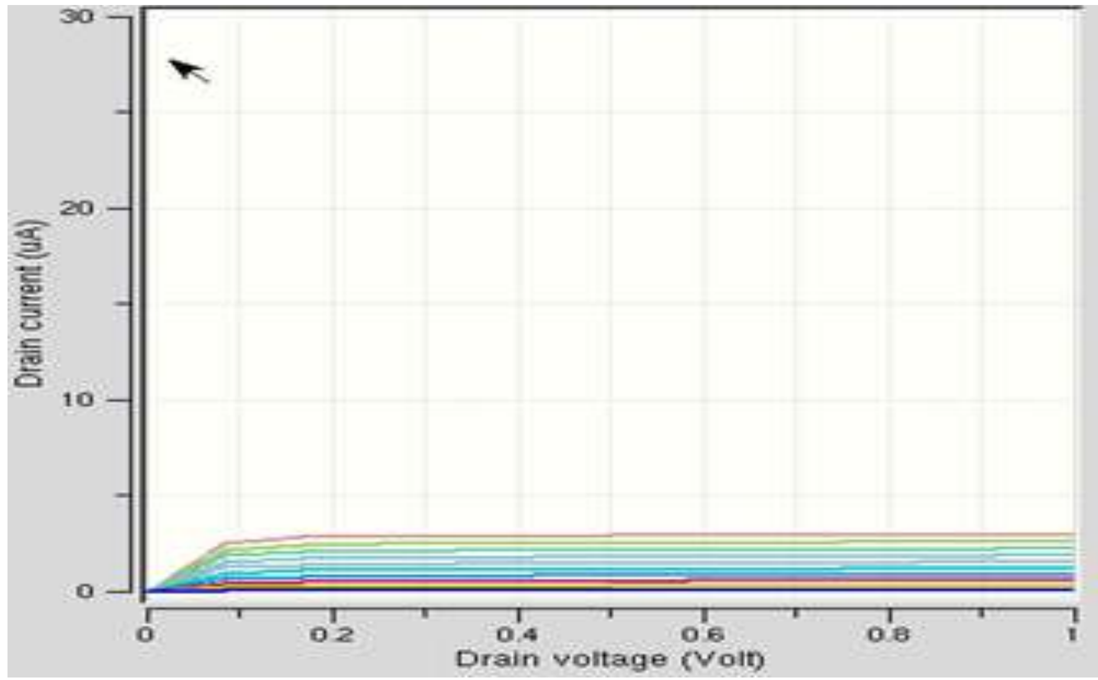


Fig. 3.10: I_d versus V_d at 0.1nm diameter

The variation of I_d versus V_d at 0.1nm and 0.2nm diameter of carbon nanotube shown in figure 3.10 and figure 3.11 respectively for a CNT based FET. The drain current rises as the gate voltage increases. I_d is high when the value of carbon nanotube diameter is high. A transfer characteristic of carbon nanotube field effect transistor is given in figure 3.12 at 1nm diameter of carbon nanotube. It is clear that CNTs diameter is more remarkable when gate voltage is low. For the large diameter of carbon nanotube, the switching speed is high.

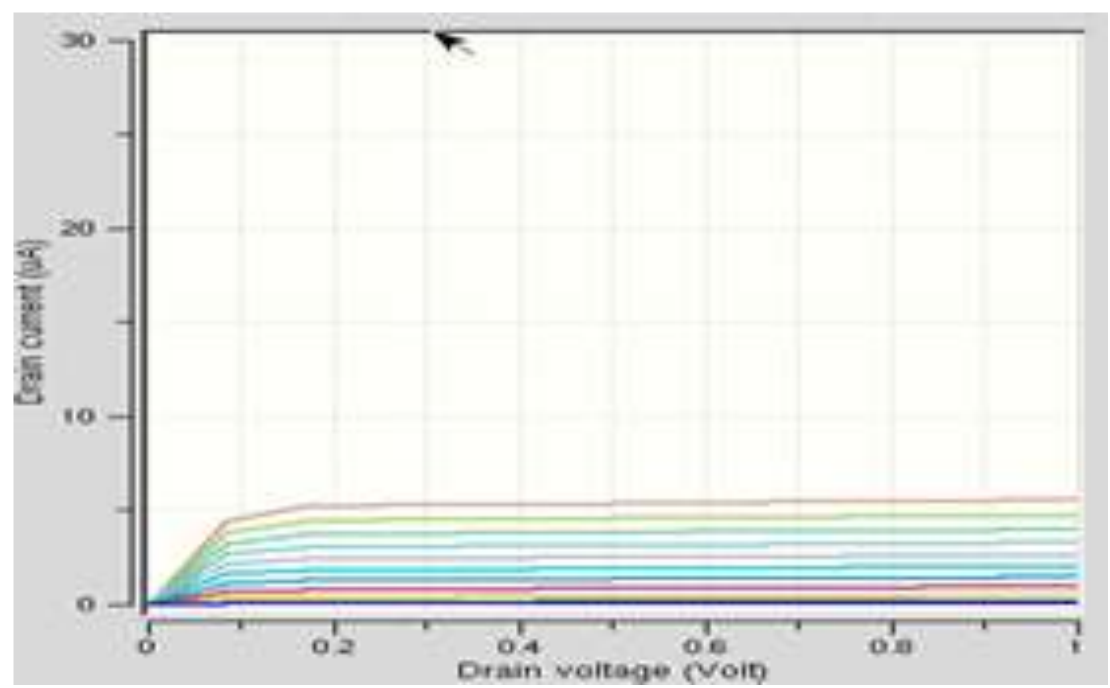


Fig. 3.11: I_d versus V_d at 0.2nm diameter

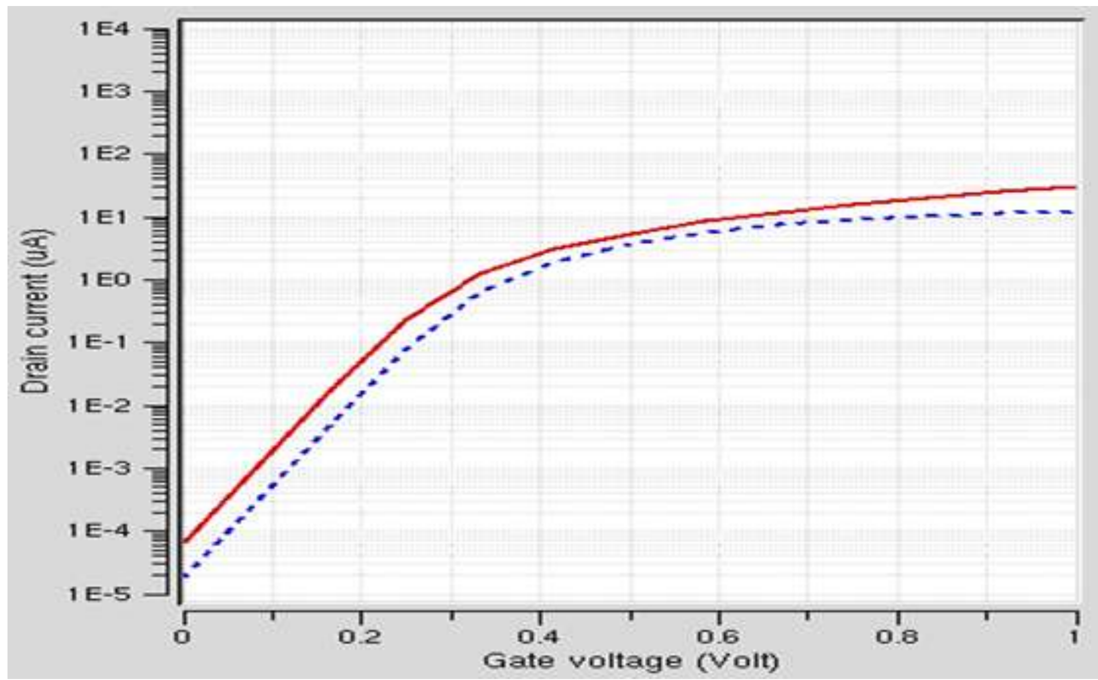


Fig. 3.12: I_d versus V_g at 1nm diameter

Comparison between CNT based FET and MOS based FET -

(1). The contact resistance modulation is responsible for the switching of carbon nanotube field effect transistor, while switching of silicon MOS based FET occurs by changing the resistivity of channel.

(2). CNT based FET is able of distributing 3-4 times larger drive currents in compare to silicon MOS based FET.

(3). The transconductance of CNT based FET is about 4 times greater than MOS based FET.

(4). In case of CNT based FET, average velocity of carrier is about double in comparison to MOS

Table 3.2: The energy band gap of carbon nanotube is inversely proportional to D_{CNT}.

S.No.	Nanotube Diameter (nm)	Gate Insulator Thickness (nm)	Gate Insulator Dielectric Constant	Gate Voltage (V)	Drain Saturation Current (micro- ampere)
1.	0.1	1.5	3.9	1	2.5
2.	0.2	1.5	3.9	1	5.9
3.	0.3	1.5	3.9	1	7.8
4.	0.4	1.5	3.9	1	11.3
5.	0.5	1.5	3.9	1	14.8
6.	0.6	1.5	3.9	1	18
7.	0.7	1.5	3.9	1	21
8.	0.8	1.5	3.9	1	24.5
9.	0.9	1.5	3.9	1	27.1
10.	1	1.5	3.9	1	30

Diameter controls energy band gap and thus current, so it is keep fixed. Comparison proved improvement.

3.5 CONCLUDING REMARKS

MOSFET has been used widely in electronics industries. With the increasing technology, we are scaling down the channel length of MOS which may results in many short channel effects. To get rid of all these drawbacks of conventional MOSFET we are studying CNTFET (Carbon nano tube field effect transistors). In this chapter a comparison is being made between conventional MOSFET and different types of CNTFETs. And finally concluded a future replacement of MOSFET. The major difference in CNTFETs and MOSFET is that it has CNT in channel instead of silicon. CNTFETs show improved characteristics with scaling of technology.

In this work, many essential principles of CNTFET are given. Beginning with different sorts of CNTFET structure, followed by the operation of CNTFET. From this chapter, this may be seen that from CNTFET structure and its behavior, the semiconducting device is in reality more or less the same as MOS based FET except that the material for transistor. Besides, Carbon nanotube Field Effect Transistor will play important role in designing of electronic circuits which are the base of digital computers.

CHAPTER 4

SIMULATION AND ANALYSIS OF CARBON NANOTUBE B-ASED CUM CMOS BASED FOLDED CASCODE OP AMP

CMOS Technology is reaching its limit. Actually, Silicon and CMOS has been utilized maximum. So, a new material along with new device which can replace silicon as a material and CMOS as a device is a need of hour. In this chapter, CNT as a new material and CNTFET as a new device will be explored in place of silicon and CMOS respectively. To meet the problems faced by conventional technology.

In this chapter, Simulation and Analysis of innovative folded cascode Operational Amplifier based on carbon nanotubes (CNT) has been performed utilizing HSPICE Software at 45 nanometer technology. Design Parameters like technology node, Supply Voltage, Number of CNTs, CNT Pitch, CNT Diameter, Thickness of Oxide, Dielectric Constant and Gate Dielectric were chosen as per design requirements. Performance Measuring parameters like DC voltage gain, avg. power, B.W. and o/p resistance have been calculated. CNT based folded cascode Op Amp results in high performance with the increase of CNTs were studied. For e.g., the increase in DC gain is 41.48% in pCNT based folded cascode Operational Amplifier and 13.93% in nCNT based folded cascode Operational Amplifier; decrease in average power is by 16.86% in pCNT based Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS based folded cascode Operational Amplifier separately. However, the output resistance has diminished in carbon nanotube based FC-OP AMP in comparison to traditional complementary metal oxide semiconductor based Folded Cascode OP AMP. The low o/p resistance has resulted in a little B.W. in carbon nanotube based FC-OP AMP. Furthermore, the simulation studies have uncovered that the performance of the CNT based folded cascode Op Amp can be enhanced optimized at various CNTs.

4.1 INTRODUCTION

As complementary metal oxide semiconductor advances develop well into short channel length, the supply voltage declines and gadget attributes weaken. These

conditions posture severe difficulties in the design of Operational Amplifier. The intrinsic gain of transistor turns out to be low because of inferior output impedance [72, 125-128]. Now to guarantee facilitate change in field effect transistor performance with managing Moore's Law, this is important to search for elective such as CNT based FETs that guarantee to convey much preferred performance over existing MOS based FETs. CNT based FET innovation may also be effectively clubbed with the bulk complementary metal oxide semiconductor innovation on a solitary chip and utilizes a similar infrastructure [128]. There has been a plenty of work available in the writing on the digital usage of CNT based FET yet its analog applications have not been investigated [72, 129]. Keeping the foregoing in mind, this chapter examines in detail the performance of Pure CNTFET Folded cascode Op Amp at 45nm for obtaining high gain, low power consumption, and low output resistance etc. Cascode is a two-stage amplifier made out of a solitary transconductance amplifier followed by a current follower. The improvement of the cascode arrangement stems from the position of an upper transistor because the load of the input transistor's output terminal. The top transistor is called cascode device. As opposed to stacking the transistors one over another, that may decrease or restrict the swing of available signal, this is frequently beneficial to “fold” the cascode device. Folded cascade amplifier has the advantages like stability, better output swing than the telescopic amplifier and two stage amplifiers.

In the work, we simulated two carbon nanotube based FC-OP AMPs and compared their performance with the conventional carbon nanotube based FC-OP AMP, utilizes N type CNT based FETs as sinks and traditional P type MOS transistor as sources. This is being known as p type CNT based folded cascode Operational Amplifier. Correspondingly, the other proposed carbon nanotube based cascode operational transconductance amplifier utilizes P type CNT based FETs as sources and traditional N type MOS transistors as sinks and is being known as n type CNT based folded cascode Operational Amplifier. Simulation and analysis of innovative folded cascode Op Amp based on CNTs has been performed using 45 nm technology node. The simulation is being done by using HSPICE. The comparison study of the proposed carbon nanotube based FC-Op Amp with the traditional complementary MOS based Folded Cascode OP AMP has shown the increase in DC gain of around 41.48% in pCNT based folded cascode Operational Amplifier and around 13.93% in nCNT based folded cascode Operational Amplifier.

Further decrease in average power is by 16.86% in pCNT based folded cascode Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS-FC-OP AMP separately. However, the output resistance has diminished in carbon nanotube based FC-OP AMP in comparison to traditional complementary metal oxide semiconductor based Folded Cascode OP AMP. The low o/p resistance has resulted in a little B.W. in carbon nanotube based FC-OP AMP. Furthermore, the simulation studies have uncovered that the performance of the CNT based folded cascode Op Amp can be enhanced optimized at various CNTs.

4.2 CNT AND CNT BASED FET

Iijima watched concentrically nested C structures while exploring the soot of a arc-discharge demonstrating betwixt two graphite electrodes in 1991. A team of Iijima and Ichihashi of NEC [130] and Bethune and associates of the IBM Almaden Research Center in California [131] found single-walled carbon nanotubes (SWNTs) in 1993.These structures were multiwalled carbon nanotubes (MWCNTs). These are carbon's allotrope. Carbon nanotube is being supposed as a faithful and is being anticipated to supplant the generally utilized Si. CNT has amazing attributes such as tensile strength high in comparison to steel, electrical conductivity high in comparison to the best conductor silver, thermal conductivity high than diamond. The semiconductor industry is confronting some significant difficulties at the nanosize measurement. Such issues incorporate power and performance advancement, the device manufacture and control of process alteration at nano-size and integration of a various arrangement of materials and devices on a similar chip [33-34].

A SWCNT is a 1 D conductor, which may be metallic/semiconducting relying on the arrangement of C atoms decided by their Chirality, whose magnitude and D_{CNT} is given in Eqs. (1) and (2) separately, where 'a' is the graphene lattice constant(0.249 nanometer) and n_1, n_2 are positive integers which indicate the chirality of the tube. D_{CNT} is the diameter of the carbon nanotube.

$$C_h = a \sqrt{(n^2_1 + n^2_2 + n_1 n_2)} \qquad (1)$$

$$D_{CNT} = C_h / \pi \qquad (2)$$

A compact model for single-walled CNTFETs was proposed [72,128]. This CNTFET model can be simulated in HSPICE [72].

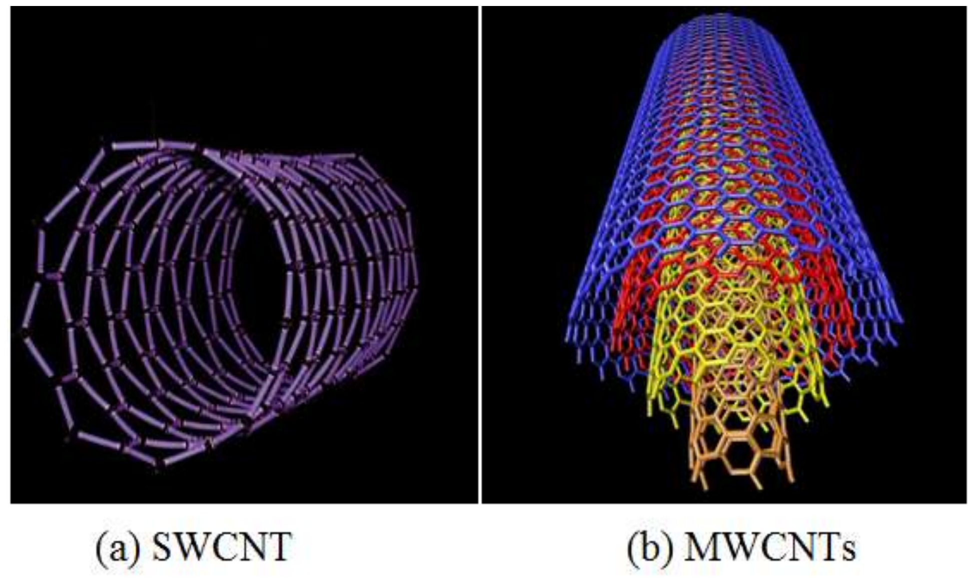


Fig. 4.1: Different types of Carbon NanoTubes

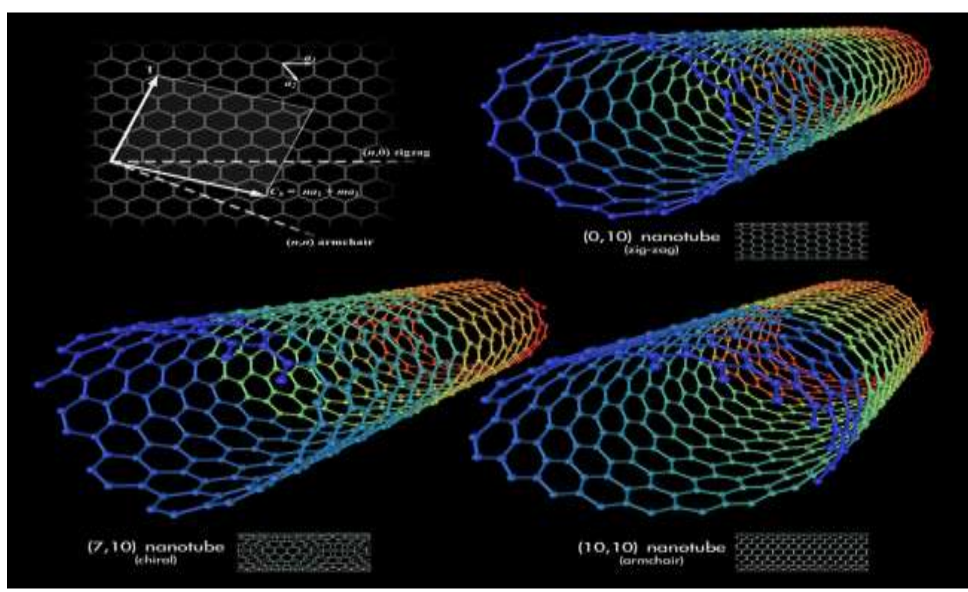


Fig. 4.2: Different types of SWCNTs

4.3 PROPOSED CNTFET BASED FOLDED CASCODE OP AMP DESIGN

The Figure 4.4 demonstrates the schematic of a folded-folded cascode operational amplifier utilizing a class AB output buffer. In the frequency response of the Op-Amp., the load of the operational amplifier is a 1 picofarad capacitor. Folded cascode Operational transconductance is designed at different carbon nanotubes (N). The

widths of CNT based FET and metal oxide semiconductor based field effect transistors are selected to be identical for a reasonable comparison.

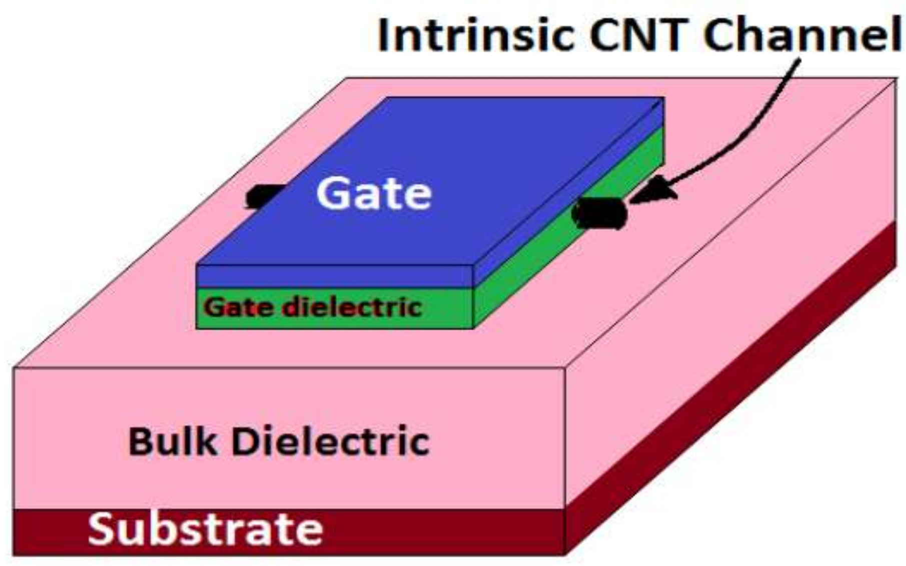


Fig. 4.3: Three Dimensional CNTFET structure

We simulated two carbon nanotube based FC-OP AMPs and their performance compared with the traditional. Figure 4.4, describes the circuit diagram of the proposed carbon nanotube based FC-OP AMP. This utilizes N type CNT based FETs as sinks and traditional P type MOS transistor as sources. This is being known as p type CNT based folded cascode Operational Amplifier. Correspondingly, the other proposed carbon nanotube based cascode operational transconductance amplifier utilizes P type CNT based FETs as sources and traditional N type MOS transistors as sinks and is being known as n type CNT based folded cascode Operational Amplifier.

4.3.1 Variation of CNTs (N)

The current drive in a CNTFET depends both on the no. of carbon nanotubes per device (‘N’) and thus DC Gain increases with CNTs as shown in figure 4.5.

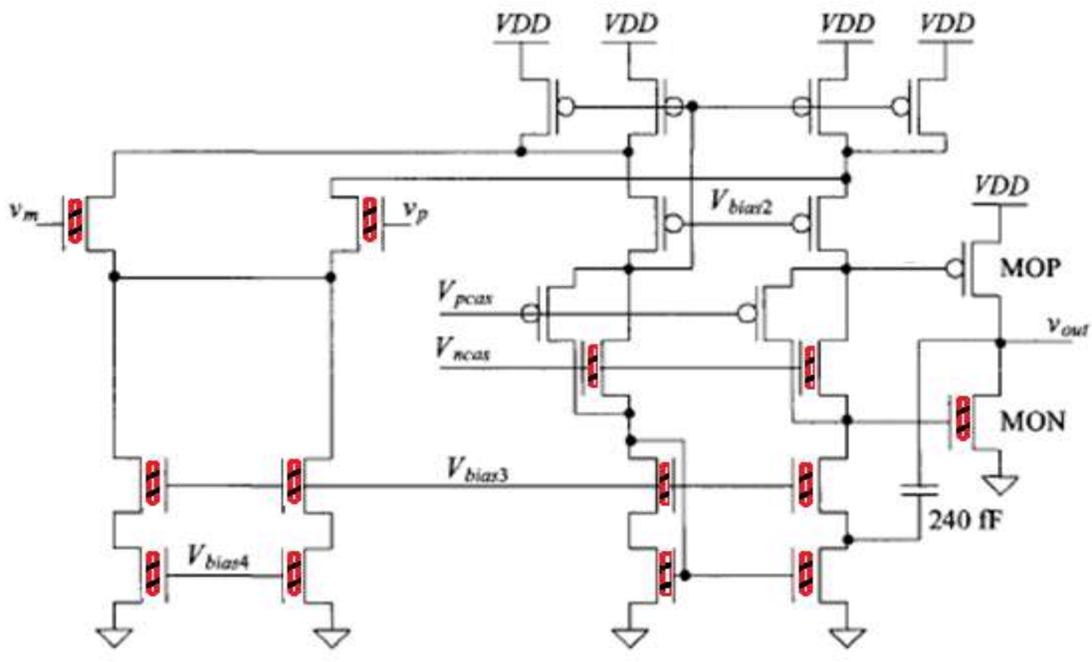


Fig. 4.4: Proposed PMOS-NCNT-FC-OP-AMP

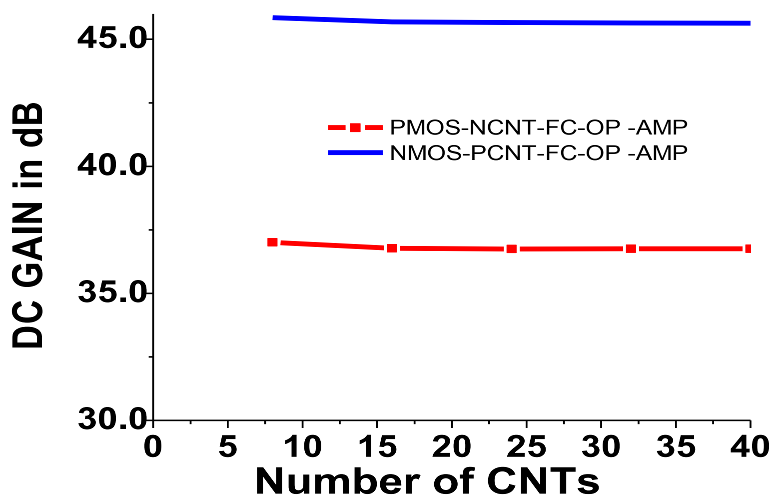


Fig. 4.5: No. of CNTs Versus DC gain

Additionally, current driving capability of CNTFET goes up with the large no. of CNTs that diminishes the o/p resistance as shown in figure 4.6, thereby allowing greater fan-out .The bandwidth increase with CNTs since output resistance decreases

as shown in figure 4.7, Also, the average power increases but it is still very small as shown in figure 4.8.

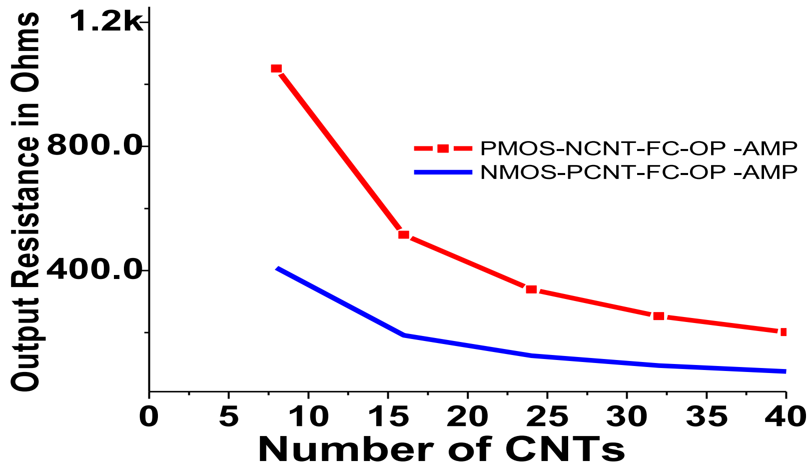


Fig. 4.6: No. of CNTs Versus Output resistance

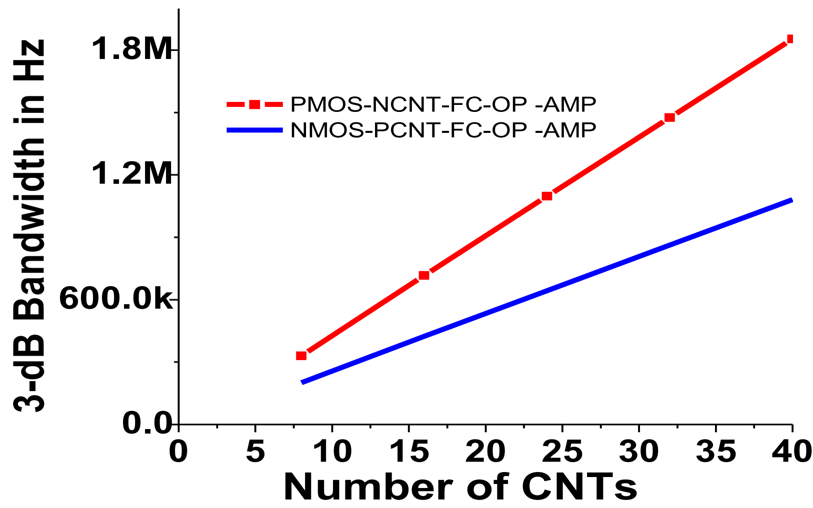


Fig. 4.7: No. of CNTs Versus 3dB B.W.

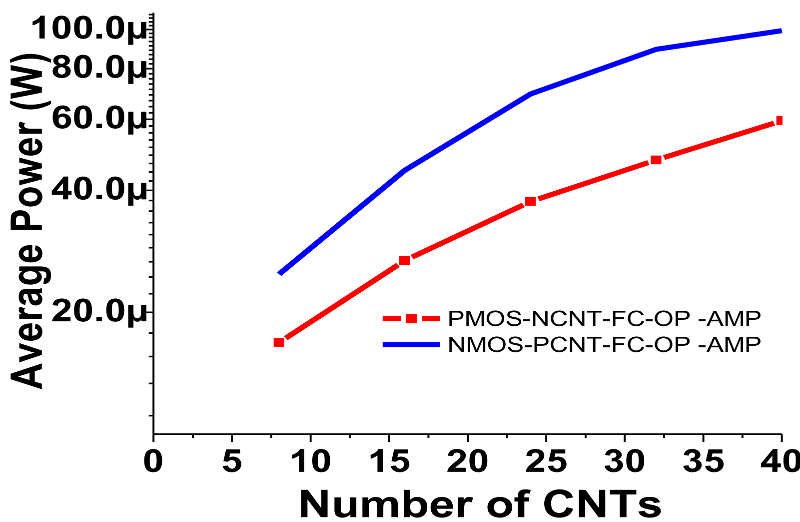


Fig. 4.8: No. of CNTs Versus Average Power

Table 4.1: Comparative analysis of FC-OP AMPs with C_L = 1 picofarad, V_{DD} = 0.9 volt@ 45nm tech., N = 24, S = 20 nanometer , D = 1.5nanometer.

S. No.	Parameter	CMOS-FC-OP AMP	PMOS-NCNT-FC-OP AMP	NMOS-PCNT-FC-OP AMP
1.	DC Gain in dB	32.3	36.8	45.7
2.	Average Power in μW	0.83	0.37	0.69
3.	Output Resistance in ohm	363.7	339	126
4.	Bandwidth in MHz	1.46	1.12	0.64

4.4 CONCLUDING REMARKS

In this research work, Simulation and Analysis of innovative folded cascode Operational Amplifier based on CNTs has been performed utilizing 45 nm node. DC voltage gain, avg. power, B.W. and o/p resistance have been calculated. CNT based folded cascode Op Amp results in high performance with the increase of CNTs. For e.g., the increase in DC gain is 41.48% in pCNT based folded cascode Operational Amplifier and 13.93% in nCNT based folded cascode Operational Amplifier; decrease in average power is by 16.86% in pCNT based Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS based folded cascode Operational Amplifier separately. However, the output

resistance has diminished in carbon nanotube based FC-OP AMP in comparison to traditional complementary metal oxide semiconductor based Folded Cascode OP AMP. The low o/p resistance has resulted in a little B.W. in carbon nanotube based FC-OP AMP. Furthermore, the simulation studies have uncovered that the performance of the CNT based folded cascode Op Amp can be enhanced optimized at various CNTs.

CHAPTER 5

TRANSIENT ANALYSIS OF N TYPE CARBON NANOTUBE BASED CUM CMOS BASED FOLDED CASCODE OPERATIONAL AMPLIFIER

Carbon Nanotube Field Effect Transistor (CNTFET) will play vital role in designing of combinational and sequential circuits which are back bone of digital computers. It is clear that CNT based FETs are the future of electronic circuit. This chapter also explores the analog applications of carbon nanotube based circuits for nanoelectronics. In this research paper, simulation of N Type CNFET based folded cascode Op Amp based on CNT has done at 45 nm technology. N Type CNT based FET based FC-OP-AMP is analyzed through Transient Response. In the Frequency Response of N Type CNTFET based Folded Cascode Op Amp, it is clear that the amplifier is efficiently working since the DC Gain is almost constant upto 1 MHz. It is also clear that the N Type CNTFET based Folded Cascode Op Amp is working as low pass filter, so it has applications in the low pass circuits. Further, it is clear from Phase response that it is stable amplifier. So, we can use it in robust conditions where stability is main concern. Furthermore, it is clear that the amplifier is power efficient since in all the conditions, the Transient Power is in nano watts.

5.1 INTRODUCTION

The historical backdrop of MOS based FET begins as right on time as 1964 while the first MOSFET is created and from that point forward, the semiconducting device has dominated in digital uses particularly associated to recent PCs. It isn't shocking since MOS based FET gives large reliability and small power utilization, plus this may also be packed in extensive numbers within a solitary IC because of its moderately small size. As Complementary MOS advancements advances well into short channel length, technologies evolve well into short channel length, there is decrease in supply voltage and decline in device characteristics. Due to these conditions Operational Amplifier is rigorous. Intrinsic gain of the transistor turns low due to inferior the device output impedance. Presently keeping in mind the end goal to guarantee advance change in Field Effect Transistor performance with managing Moore's Law, it is important to

find out the other technique such as CNT based FETs that gives the better performance than existing MOSFETs. There has been a plenty of work available in the writing on the digital usage of CNT based FET yet its analog applications have not been investigated [132,133]. Keeping the foregoing in mind, the paper examines in detail the performance of N Type CNTFET based folded cascode Op Amp based on CNT has done at 45 nm technology for Transient Analysis. There are a few impacts that show up as the MOS based FET size achieves nm scale and turns into the restricting factor which influence the performance of the MOS based FET itself. The variables are: (a) SCE (b) Tunnelling impact (c) Ballistic transport (d) Thickness of oxide (e) V_{th}. The other point of view of constraint components to scaling procedure of MOS based FET are (a) Conceptual boundary (b) Innovation boundary (c) Economical boundary.

In 1991 a Japanese researcher, Iijima, examined the carbon residue made by a direct current arc-discharge betwixt carbon electrodes, he found a range of particles that have been the aim of great logical research ever since. Utilizing a HRTEM, this is discovered that the long atoms comprising of a few coaxial cylinders of carbon. The revelation drives the exploration domain for CNT despite the fact that the planning of carbon fibers were at that point began in 1980's and 1970's via the synthesis of vapor grown carbon fibers.

CNTs are a standout amongst the most encouraging hopeful that may offer an answer for a portion of the issues said above. Carbon nanotubes are self-assembled 1-D macromolecular systems with some outstanding electronic attributes. CNTs may be metallic and semiconducting relying upon their structure, that proposes their capacity for very extraordinary nanoelectronic based applications. From one perspective the semiconducting carbon nanotubes, with their high current densities and the deficiency of interface states, in comparison with the Si and silicon dioxide interface, would be perfect possibility to supplant Si in future transistors. In actuality, this has just been exhibited that CNT based FETs may have a performance better than the most developed Si MOS based FETs [134-135]. For example, CNTs show thermal conductivities considerably bigger than that of diamond at room temperature. It is very fascinating, as heat dissemination is as of now a pivotal problem in the present integrated circuits. Furthermore, CNTs indicate extraordinary chemical and mechanical stability. Their modulus of elasticity may be as large as 1 TPa [136,137].

Inspired by the fullerene explore, various researchers hypothetically assumed a speculative carbon structure comprising of just a single sheet of graphene rolled in to a tube which resembles an extended fullerene atom–single wall nanotube[33,34,138]. Many shocking attributes were anticipated for single wall nanotubes, for example that SWNTs ought to be semiconducting and metallic and behave such as one dimensional conductor. Single wall carbon nanotube was found just a short time later, in 1993.

The cascode is a two-stage amplifier build out of a singular transconductance amplifier followed by a current follower. The improvement of the cascode setup comes from the position of an upper transistor as the load of the input transistor's output terminal. The upper transistor is referred to as the cascode device. As opposed to stacking the transistors one over another, that can decline or restrict the swing of accessible signal, this is beneficial to "fold" the cascode device. Folded cascode amplifier has the advantages like stability, better output swing than the telescopic amplifier and two stage amplifiers.

5.2 CNT- A NEWLY MATERIAL FOR SEMICONDUCTING DEVICES

Presently keeping in mind the end goal to guarantee advance change in FET performance with supporting Moore's Law, this is important to search for alternative such as CNT based FETs that guarantee to convey much superior performance over existing MOSFETs. CNT based FET innovation may also be effortlessly clubbed with bulk complementary metal oxide semiconductor innovation on a one chip and uses a similar infrastructure. A SWCNT is a 1-D conductor, which may be metallic and semiconducting relying on the arrangement of C atoms decided by their Chirality, whose magnitude and relationship with D_{CNT} is given by Eqs. (1) and (2) separately.

$$C_h = a \sqrt{(n^2{}_1 + n^2{}_2 + n_1 n_2)} \qquad (1)$$

$$D_{CNT} = C_h / \pi \qquad (2)$$

where ‘a’ is the graphene lattice constant (0.249 nanometer) and n_1, n_2 are positive integers which describe the chirality(C_h) of the tube [33,34,126,128,139]. D_{CNT} is the diameter of the carbon nanotube.

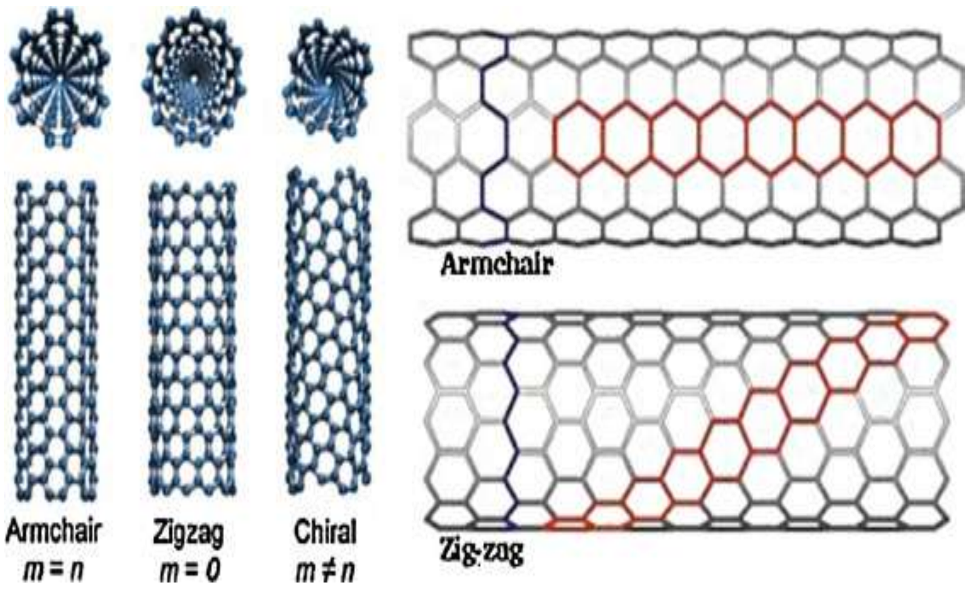


Fig. 5.1: Different types of Carbon NanoTubes

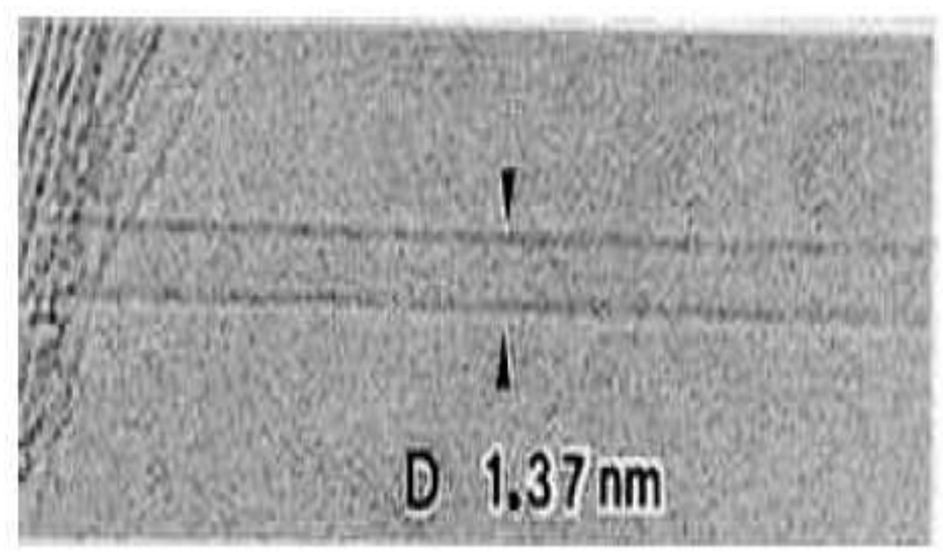


Fig. 5.2: Single wall carbon nanotube from Iijima et al. [140]

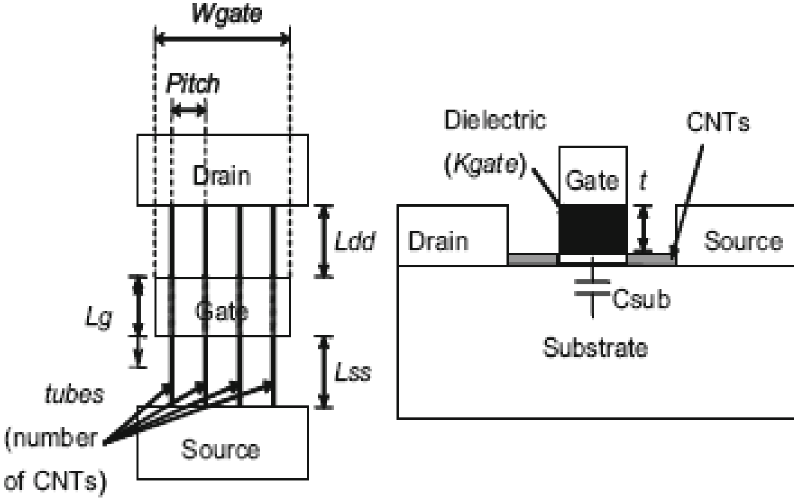


Fig. 5.3: Schematic CNTFET cross-section

5.3 DESIGN OF CNTFET BASED FOLDED CASCODE OPERATIONAL AMPLIFIER

The Figure 5.5 shows the schematic of a conventional FC-operational amplifier utilizing a class AB output buffer. In the frequency response of the operational amplifier, the load of the operational amplifier is a 1 picofarad capacitor. We have simulated N Type CNTFET based FC-OP AMPs and analyzed AC and Transient Response.

5.3.1 AC Analysis of N Type CNTFET Based Folded Cascode Operational Amplifier

The Frequency Response of N Type CNTFET based Folded Cascode Op Amp is shown in figure 5.6. In this response, it is clear that the amplifier is efficiently working since the DC Gain is almost constant upto 1 MHz. It is also clear that the N Type CNTFET based Folded Cascode Op Amp is working as low pass filter, so it has applications in the low pass circuits.

The Phase Response of N Type CNTFET based Folded Cascode Op Amp is shown in figure 5.7. Further, it is clear from Phase response that it is stable amplifier. So, we can use it in robust conditions where stability is main concern.

5.3.2 Transient Analysis of N Type CNTFET Based Folded Cascode Operational Amplifier

Power Variation of N Type CNTFET based Folded Cascode Op Amp is shown in figure 5.8. In this response, it is clear that the amplifier is power efficient since in all the conditions the Transient Power is in nano watts.

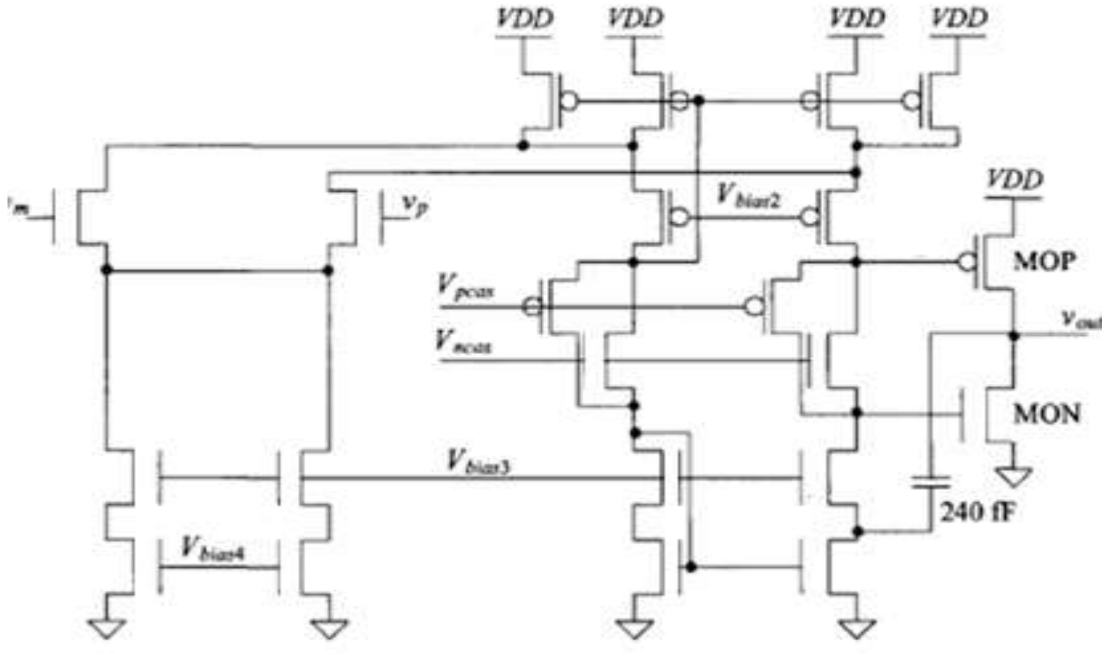


Fig. 5.4: Conventional FC-OP-AMP

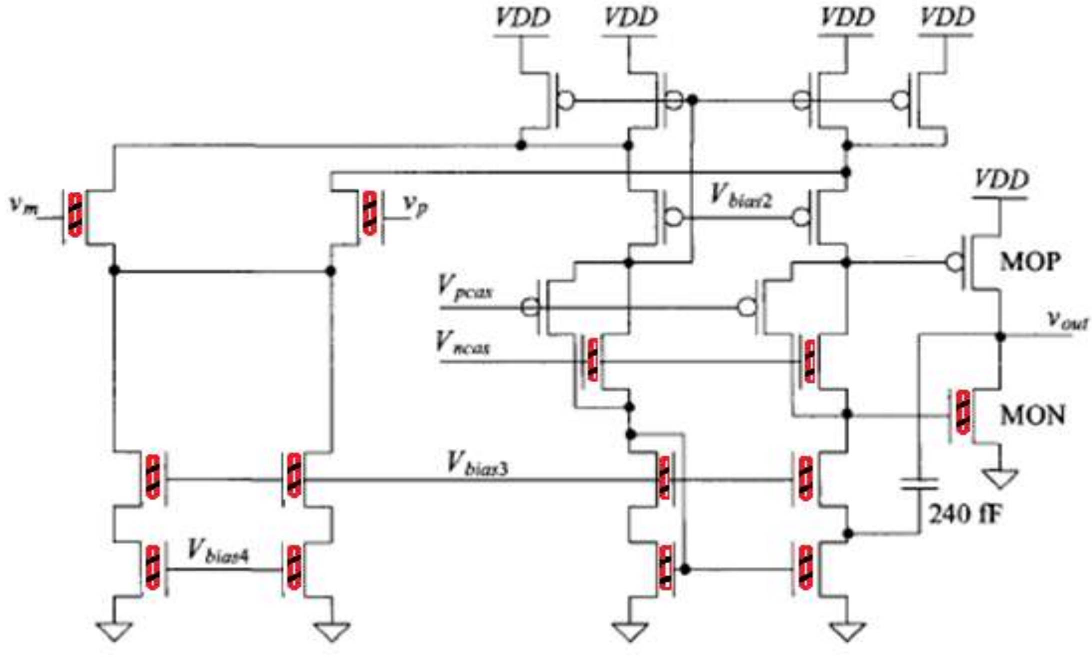


Fig. 5.5: Proposed PMOS-NCNT-FC-OP-AMP

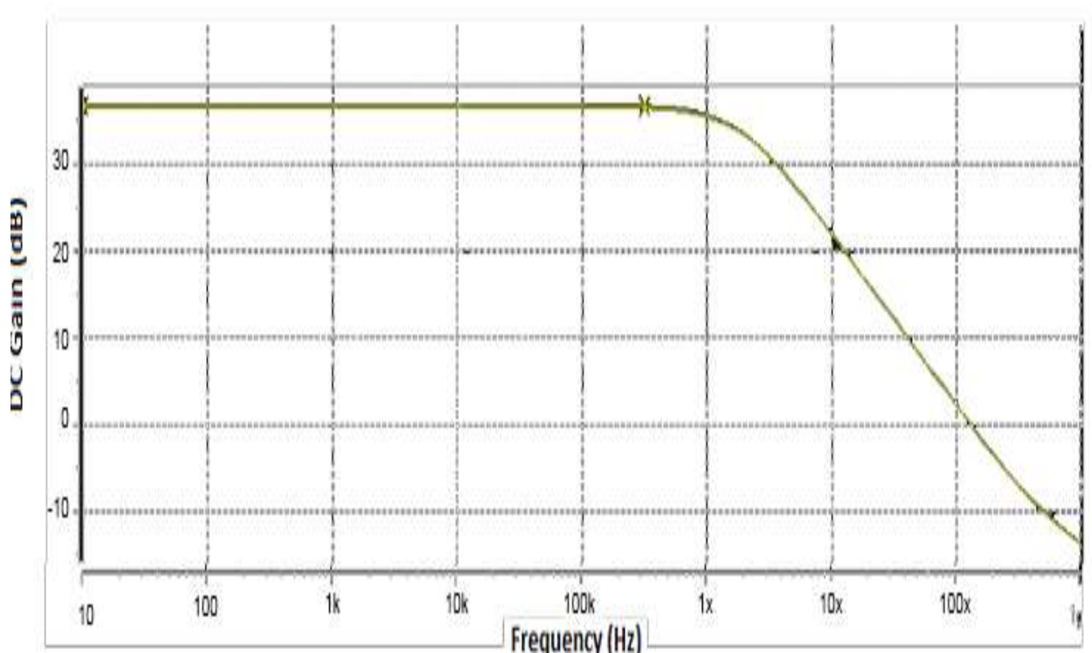


Fig. 5.6: Frequency Response of N Type CNTFET based Folded Cascode OpAmp (AC Analysis).

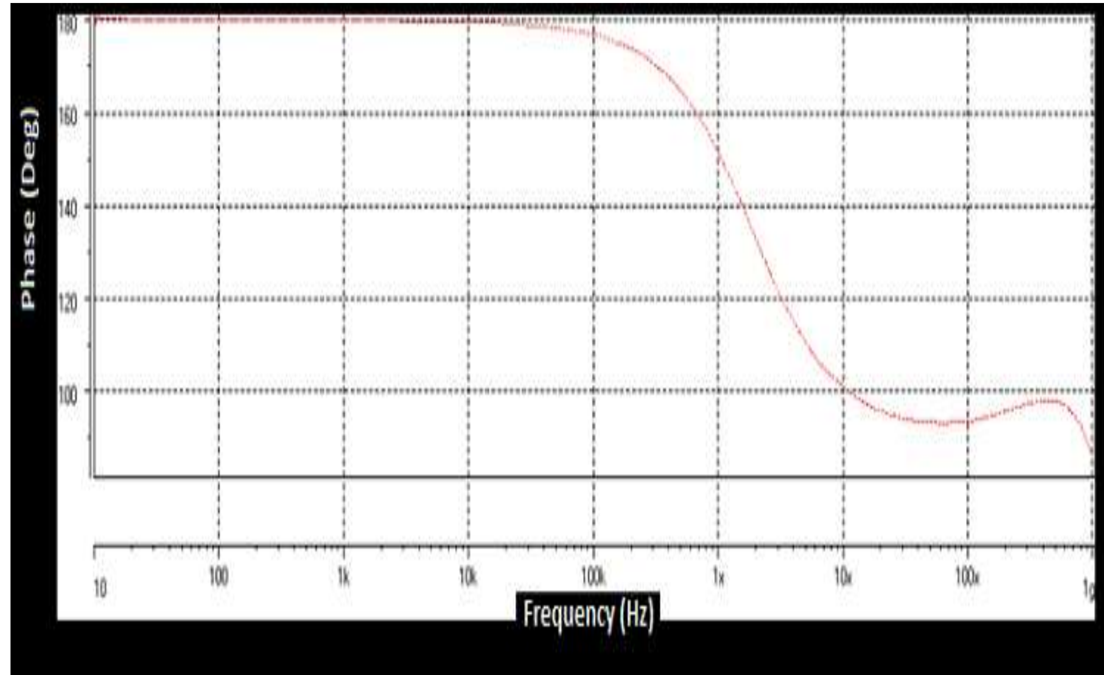


Fig. 5.7: Phase Response of N Type CNTFET based Folded Cascode Op Amp (AC Analysis)

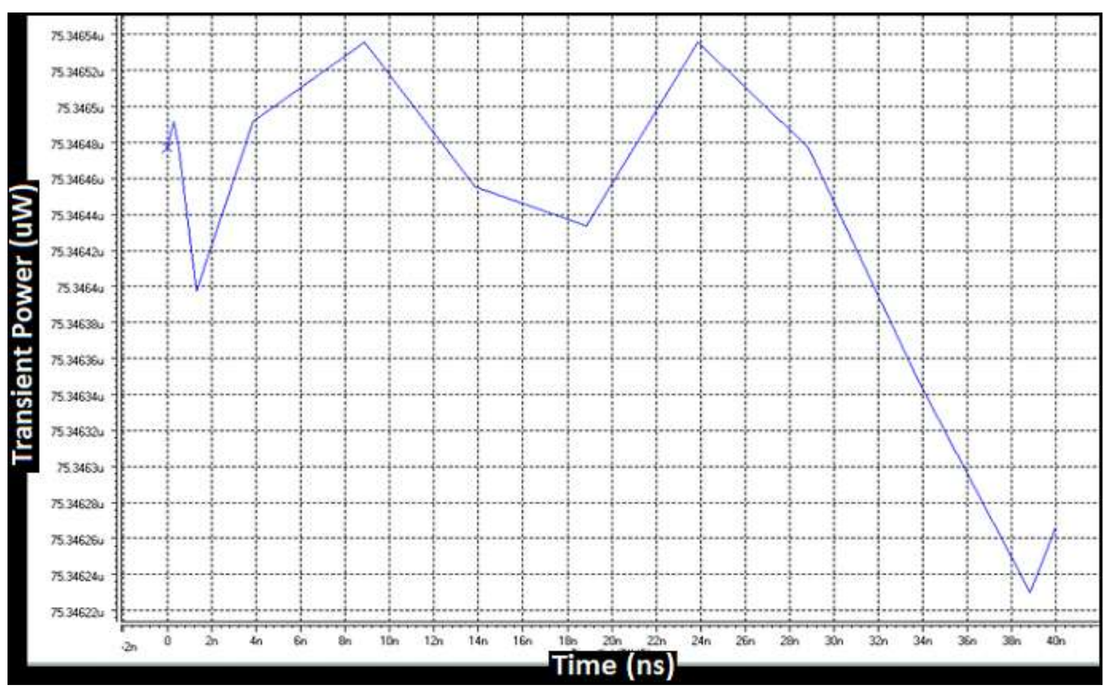


Fig. 5.8: Power Variation of N Type CNTFET based Folded Cascode OpAmp (Transient Analysis)

Static power is power consumed while there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input have active inputs (i.e., all inputs are "static" because they are at fixed dc levels). Dynamic power is power consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as the static component.

In this research work, active performance of proposed circuits is analysed so, transient Power, a type of active power is studied.

5.4 CONCLUDING REMARKS

In this research work, simulation of N Type CNTFET based folded cascode Op Amp based on carbon nanotubes (CNT) has done at 45 nm. We have simulated N Type CNTFET based FC-OP AMPs and analyzed Transient Response.

In the Frequency Response of N Type CNTFET based Folded Cascode Op Amp, it is clear that the amplifier is efficiently working since the DC Gain is almost

constant upto 1 MHz. It is also clear that the N Type CNTFET based Folded Cascode Op Amp is working as low pass filter, so it has applications in the low pass circuits. Further, it is clear from Phase response that it is stable amplifier. So, we can use it in robust conditions where stability is main concern. Furthermore, it is clear that the amplifier is power efficient since in all the conditions, the transient power is in nano watts.

This chapter also explores the analog applications of carbon nanotube based circuits for Nanoelectronics. It is clear that CNT based FETs are the future of electronic circuit. CNTFET will play vital role in designing of combinational and sequential circuits which are back bone of digital computers.

Further, role of CNT based cascode amplifier which is designed in this paper is having applications in various electronic circuits like filters, integrators, differentiators, ADC, DAC etc. The low voltage applications and lower dissipation at nano scale is a remarkable innovation in the work.

Furthermore, carbon nanotube has higher current carrying conductivity more transconductance and both semiconducting cum metallic behaviour. So, the proposed circuit is superior in terms of velocity, gain, power and durability. CMOS will be replaced by CNTFETs in near future due to better properties.

Finally, it is clear that the proposed N type CNTFET based cascode amplifiers are important building blocks in analog circuits design. This model is perfect for low VLSI applications. The proposed model explores compact design in which both CNTFET based circuits and interconnects are made up of carbon nanotubes.

CHAPTER 6
DESIGN AND SIMULATION OF CNTFET BASED LOW PASS FILTER

Signal processing is required in PC, mobile and electronic gadgets. Signal processing is as needed in the real world of day's analog in nature. So, complex signals are converted into digital form. Therefore, a fast and efficient signal processing required which consumed minimum power.In this chapter, simulation of low pass filter has done at 45 nm technology using HSPICE for low frequency applications. Design Parameters like technology node, Supply Voltage, Number of CNTs, CNT Pitch, CNT Diameter, Thickness of Oxide, Dielectric Constant and Gate Dielectric were chosen as per design requirements. Performance of the CNT based FET based LPF was analyzed.The simulation result of proposed CNT based FET based LPF show that the frequency response of Low Pass Filters are working satisfactory. It has applications in the low pass circuits. In electronics, these filters are widely used in many applications. Moreover, it is clear from the Phase response of CNT based FET based LPF that it is stable Filter. So, we can use it in powerful conditions where stability is main concern.

6.1 INTRODUCTION

The first MOSFET is invented as early as 1964 and since then, MOSFETs has prevailed in digital application particularly related to modern computers. Metal oxide silicon field effect transistor has been used widely in electronics industries. With the increasing technology, we are scaling down the channel length of MOS which may results in many short channel effects. Due to these conditions operational amplifier is rigorous. Intrinsic gain of the transistor is decreases because of the inferior device output impedance. There are many problems, which are facing by semiconductor industry at nano-range size. The challenges are power/performance optimization, fabrication of device and manage of process variation at nano-range and combination of different set of semiconducting materials and the devices on the selfsame chip.To get rid of all these drawbacks of conventional MOSFET performance for maintaining Moore's rule, this is compulsory to find out the other solution like CNTFETs that gives the better performance than existing MOSFETs. Carbon nanotube is the new

material which has ability to replace Si in the future. CNT has remarkable unique properties which build carbon nanotube a favourable material in coming years. CNT based FET is an important application of CNT. Carbon nanotube Field Effect Transistor will play important role in designing of sequential and combinational circuits which are the base of digital computers. Carbon Nanotube Field Effect Transistors have been supposed as accompaniment to, future electronic circuit because of the bigger current carrier mobility in carbon nanotubes compared to bulk Si.

CNTFET uses an arrangement of CNT material in place of Si in channel length which is used in MOSFETs. Due to its inert nature it can conduct at the maximum. In CNTFET the flow of electrons follows the ballistic transport and the leakage current is very low hence exhibiting excellent performance characteristics over conventional MOSFET. The path of technological advancements has been paved by the scaling down of devices. Size of distinct devices in an IC obeys Moore's rule. [16]. A large research work is available on the applications of digital field of CNT based FETs, still its much applications of analog field are not obtained. Remembering the prior, this chapter investigates in subtle element the execution of CNT based FET based low pass filter has done at 45 nm node technology for getting the frequency response of carbon nanotube field effect transistor based low pass filter. The simulation is being done by using hspice. In this research paper, simulation of Low Pass Filter has done at 45 nm technology. The simulation result of proposed CNT based FET based LPF show that the frequency response of Low Pass Filters are working satisfactory. Moreover, it is clear from Phase response of CNT based FET based LPF that it is stable Filter. So, we can use it in powerful conditions where stability is main concern [141].

Electric wave filters are networks having the property of separating betwixt alternating currents of various frequencies freely passing those within a specific range and completely suppress the other remaining frequencies. Filters were first investigated by G.A. Compbell and O.J. Lobel of the Bell Telephone Laboratories. The filter probably has its greatest uses in various applications like telemetering apparatus etc, depending on the requirements either attenuation or transmission of signal of particular bandwidth. Filters are termed as active or passive according to their component characteristics. The signals like biomedical, with low amplitude and frequencies are naturally given outer unsettling influence or noise like signals because

of interference. Voltages or currents that have a tendency to degenerate the primary signal, for example, exchanging noise in the system power supply ripple, tend to influence the information present in the signal. Consequently, low pass filters are utilized to expel the undesirable frequency components. By and by, there are various circumstances in which analog continuous time filters are a need. Analog filter circuits give band restricting of the signals before the signals can be sampled for further handling. A transconductance based low pass filter circuit is worked for this reason. MOS innovation is advantageous for executing OTAs in light of the fact that are intrinsically VCCS semiconducting devices. An assortment of MOS based OTAs along the various topologies is created for various motives. OTA based active filters are extremely famous attributable to their remarkable components, for example, the transconductance of OTAs are linear and flexible above extensive variety of I_{bias}, which give amazing amplifier's matching , and give high yield signal to noise ratio.

The word FC operational tranconductance amplifier is inferred through the overlaping down p type channel cascode active loads of a differential combine and varying the MOS based FETs to n-channels. We have decided on folded cascode operational transconductance amplifier for huge gain and large B.W. performance of FC-OTA, furthermore its great power supply rejection ratio contrasted with the two stage operational amplifier as operational transconductance amplifier is repaid along active loads. It has found an expansive use in filters, A/D converters in view of its diminished thermal noise, high gain and conceivable advancement of power utilization. In this area, framework and amusement of novel folded cascode OTAs based CNTs has been performed. CNT based folded cascode Op Amp results in high performance than conventional CMOS based folded cascade Op Amp in DC voltage gain, average power [142].

6.2 CNT BASED FET- A FUTURE ALTERNATIVE OF MOSFET

In 1991, Iijima first observed that a carbon nanotube assembles a macromolecular class with one of a kind thermal, mechanical and electricity properties. The nanotubes are a standout amongst almost all encouraging applicant which may give an answer for a portion of the issues specified previously. Carbon nanotubes may be metallic/semiconducting relying upon the position of the atoms of carbon determined by its chiral vector that recommends his probable as fairly diverse nanosize based advanced electronic applications. From one perspective the semiconducting carbon

nanotubes, with their high current densities and the deficiency of interface states, in comparison with the Si and silicon dioxide interface, would be perfect possibility to supplant Si in future transistors. In actuality, this has just been exhibited that CNT based FETs may have a performance better than the most developed Si MOS based FETs [16,143,144]. Inspired by the fullerene explore, various research groups hypothetically supposed a speculative C structure comprising of just a single sheet of graphene rolled in to a tube which resembles an extended fullerene atom– single wall nanotube [34, 72, 129, 138, 145]. Many shocking attributes were anticipated for SWCNTs, for example that they ought to be semiconducting/metallic and behave such as one dimentional conductors. Single Wall Carbon Nanotubes were invented after a short time, in 1993.

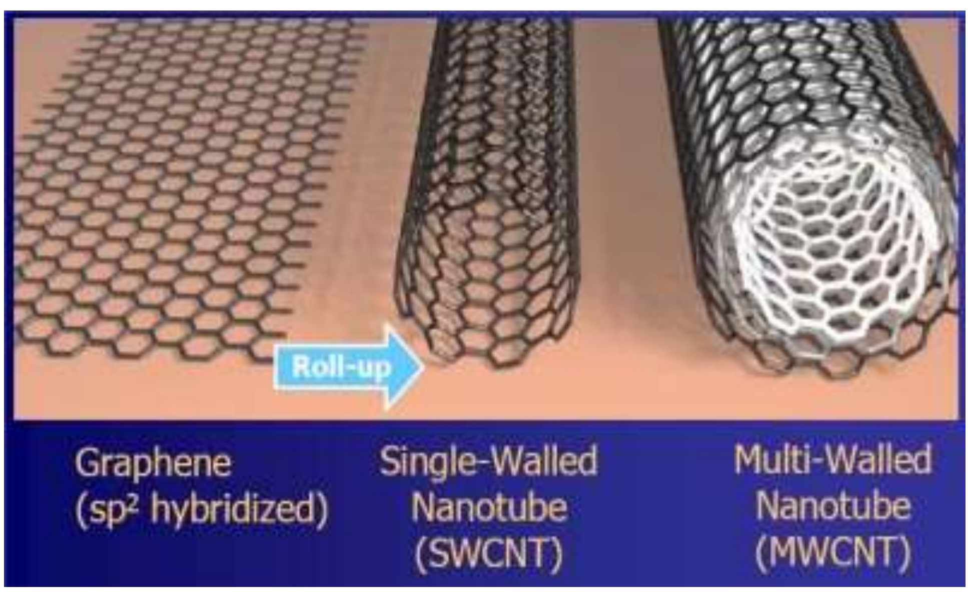


Fig. 6.1: Different types of Carbon NanoTubes

Now in order to ensure further development in Field Effect Transistor performance as per the Moore's Law, this is important to consider for alternative like CNT based FETs which promise to give much superior performance over existing MOS based FETs. Carbon Nanotube based Field Effect Transistor may also be effortlessly imparted to the bulk complementary metal oxide semiconductor innovation on a one chip and utilizes a selfsame structure. A SWCNT is a 1D conductor, which may be metallic/semiconducting relying upon the direction of carbon atoms decided by their Chirality, Ch. The magnitude and the relationship of Ch with D_{CNT} is given by Eqs.(1)

and (2) individually, where "a" is known as graphene lattice constant whose value is 0.249 nanometer and n_1, n_2 are positive numbers that determine the chirality of the tube [33,34,72,129,145,139,128,76]. D_{CNT} is the diameter of the carbon nanotube.

$$C_h = a \sqrt{(n_1^2 + n_2^2 + n_1 n_2)} \quad (1)$$

$$D_{CNT} = C_h / \pi \quad (2)$$

CNTFETs are favourable candidates as augmentation to Si complementary metal oxide semiconductor because of marvellous CV/I device performance [146,125]. CNTFETs may be classified as either SB controlled field effect transistor/ MOS based FET like field effect transistor [147, 148] according to the operation mechanism. Considering both the fabrication feasibility [150] and better device ac performance of the MOS based FET like CNT based FET, can be used, as compared to the Schotkky Barrier-controlled field effect transistor, MOS based FET like CNTFETs are used for the performance evaluation.

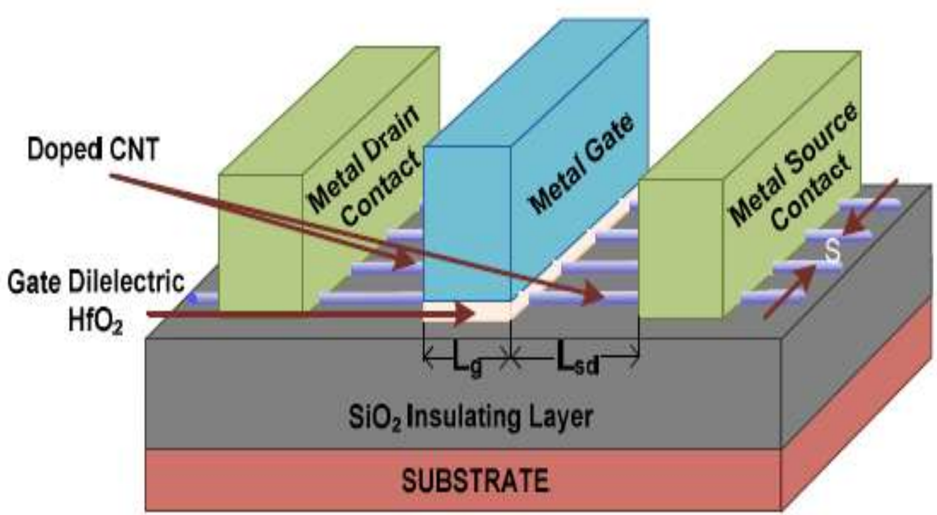


Fig. 6.2 : Physical structure of the CNFET with multiple tubes

6.3 DESIGN OF CNFET BASED LOW PASS FILTER

Folded OTA based first order active LPF are clarified utilizing the linearity of transconductance of operational transconductance amplifier with I_{bias}. We have decided on folded cascode topology because of its huge B.W. and high gain. One more explanation behind utilizing operational transconductance amplifier rather than operational amplifiers is that the frequency in the operational transconductance

amplifier may be shifted as per the I_{bias} which is controlled by the difference of input voltage. Though if there should arise an occurrence of operational amplifiers the frequency is changed by differing the capacitor's size that is the significant downside of operational amplifiers in large frequency applications when the size of the capacitor will increment and thus creating the circuit cumbersome.

The Figure 6.3 demonstrates the schematic of a conventional FC- operational-amplifier utilizing a class AB output buffer. The load of the operational - amplifier is a 1 picoarad capacitor, in the frequency response of the operational - amplifier. The Figure 6.4 & 6.5, describes the circuit diagram of CNT based FC-Op-Amp. CNT based folded cascode Op Amp results in high performance than conventional CMOS based folded cascade Op Amp in DC voltage gain, average power. [142]. We have analyzed CNFET based low pass filter's frequency response.

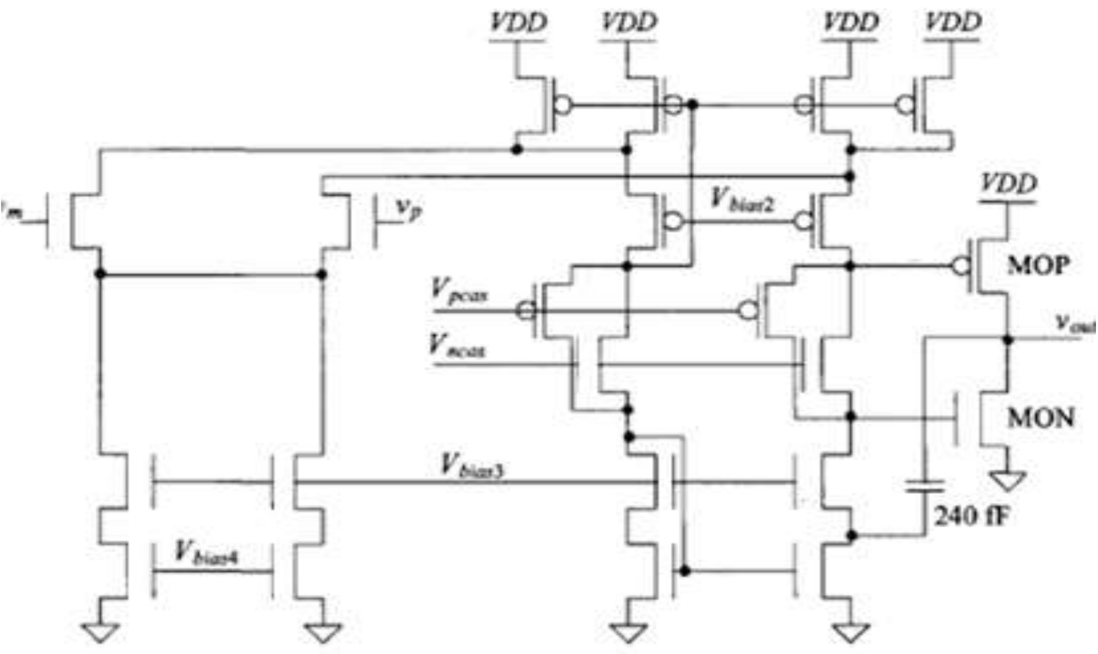


Fig. 6.3: Conventional Folded Cascode OP-AMP

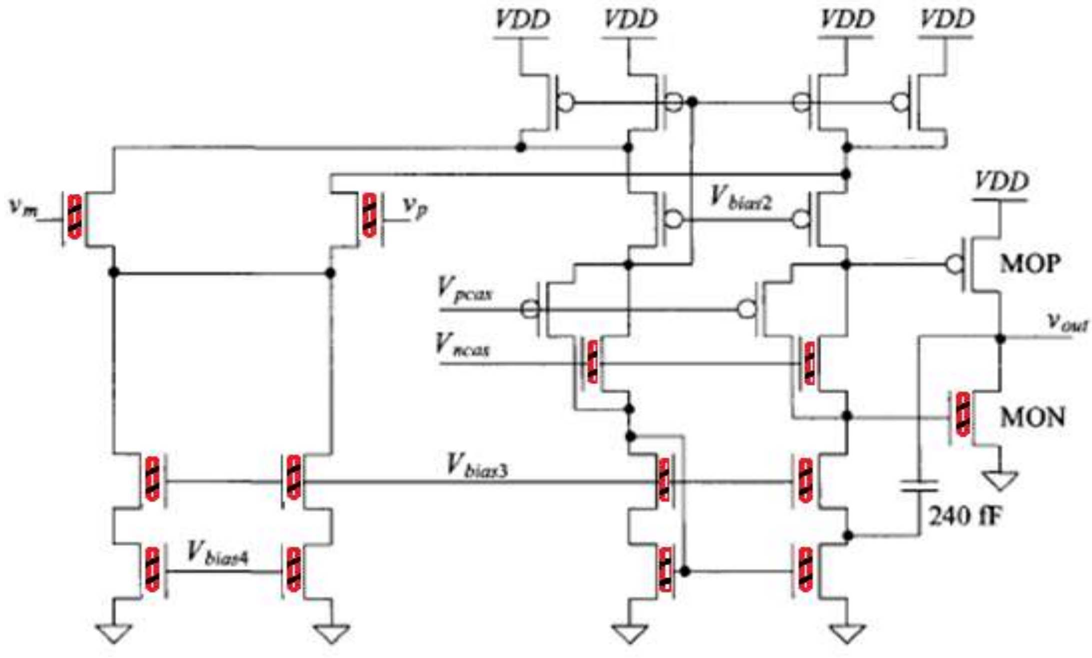


Fig. 6.4: Proposed PMOS-NCNT-FC-OP-AMP

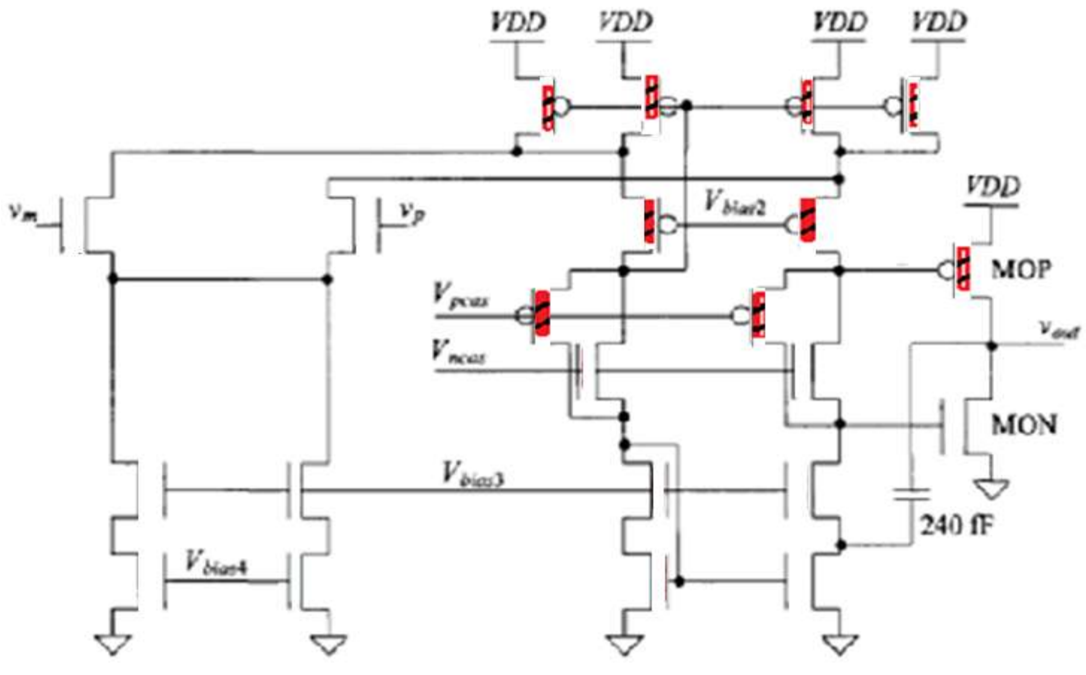


Fig. 6.5: Proposed NMOS-PCNT-FC-OP-AMP

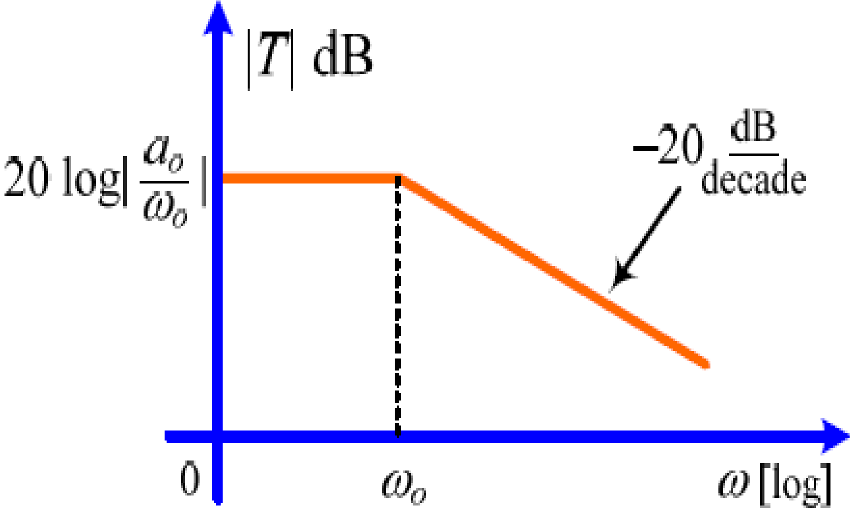


Fig. 6.6: First-order LPF-Bode plot

A first-order all pass channel is a signal handling filter which holds the amplitude of the signal consistent over the craved frequency range while the phase is ordinarily moved between 0° to - 180° or 180° to 0°. This may be connected to the electronic measurements, communications and automatic control. For instance, this utilized to adjust for other undesired phase shifts that emerge in the system. Different sorts of circuits like oscillators and high-Q band pass filters are additionally acknowledged by utilizing first-order all pass filters. Accordingly, some first-order all pass filters taking into account distinctive design methods has been proposed. All LPFs are assessed at a specific f_c. This cutoff frequency is the frequency over which the output voltage falls lower than 3dB of the input voltage. A LPF, appeared in Figure 6.7, permits signals of low frequency and suppresses the signals which have frequencies above the cutoff frequency of filters. LPFs are utilized at whatever point high frequency parts must be weakened from a signal [151-161].

The cutoff frequency of a basic capacitive low-pass filter in Hz is given by :

$$fc = 1/2\Pi RC$$

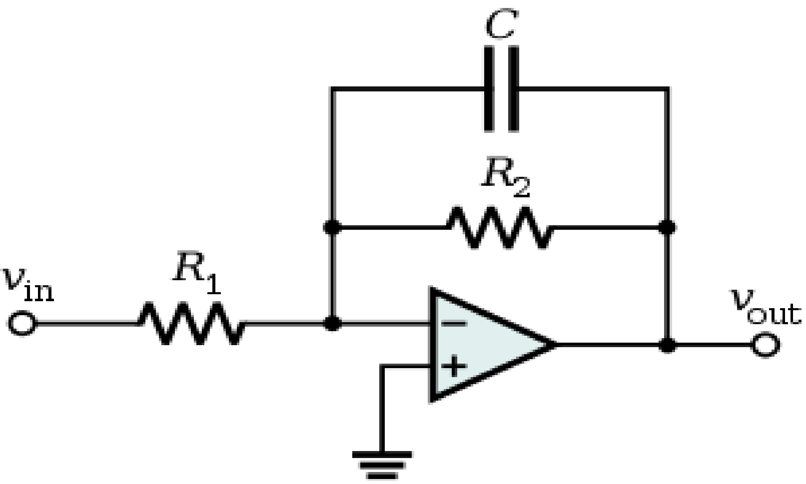


Fig. 6.7: Low Pass Filter

6.4 SIMULATION RESULT

Figure 6.8, displays the frequency responses of the proposed CNT based FET based LPF. The performance of the proposed CNT based FET based LPF is confirmed from hspice simulation results. It is clear the simulated results match the original characteristics of Low Pass Filters.

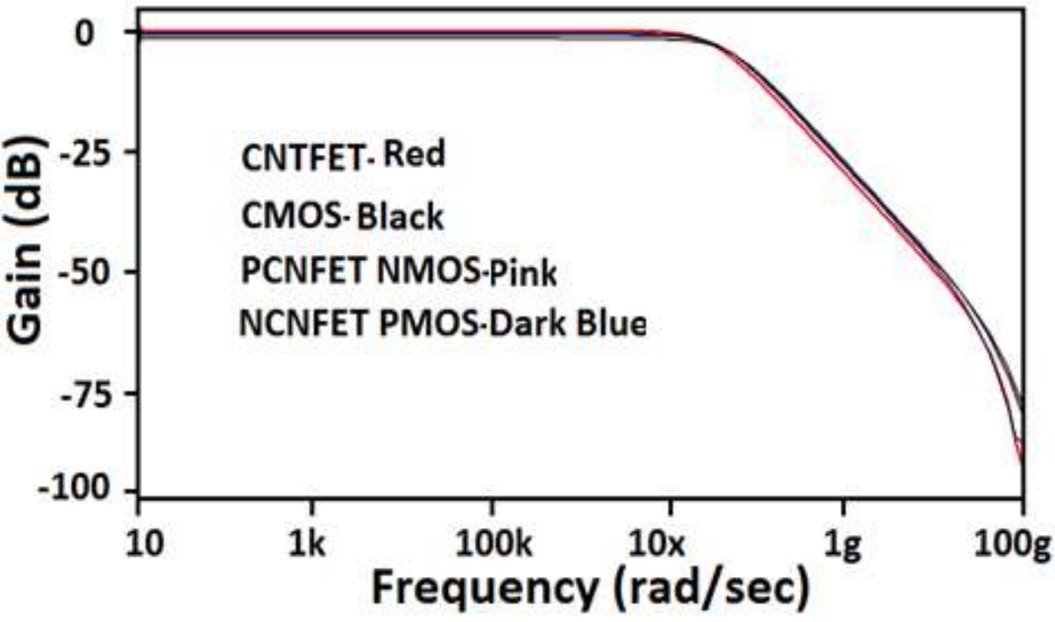


Fig. 6.8: Proposed Low Pass Filter Responses

Table 6.1: Device parameters and process assumptions for simulations

Variable Parameters	
S/ D Doping Level	0.59 eV – 0.75 eV (0.7% - 1.3%) Uniformly distributed*
D_{CNT}	1.2 nanometer to 1.8 nanometer Uniformly distributed*
Prob. of carbon nanotube to be Metallic	8% - 32%
Fixed Parameters	
Thickness of oxide	4 nm
K_{OX}	Hafnium dioxide(16)
Pitch of carbon nanotube	4 nm
Supply	0.9 V
MFP : Intrinsic Carbon nanotube	200 nm
MFP : Doped Carbon nanotube	15 nm
Length of Source, Gate, Drain (Carbon nanotube)	32 nm
Contact work function, φ_M	4.5 Ev
CNT work function, φ_{CNT}	4.5 Ev
Interconnect Capacitance	0.22 fF/ µm

6.5 CONCLUDING REMARKS

In this chapter, the performance of the CNT based FET based LPF is analyzed using hspice. The frequency response of CNT based FET based LPF is better than the conventional CMOS. It is clear the simulated results match the original characteristics of Low Pass Filters. It can be used in the low pass circuits applications. Moreover, Phase response of CNT based FET based LPF shows that it is stable Filter. So, we can use it in powerful conditions where stability is main concern. Moreover, it shows that power consumption is very low (in nano watts) in the CNT based FET based LPF. The performance is not degraded due to low power supply i.e. 0.9V. This chapter also investigates the analog applications of carbon nanotube based circuits for electronic circuits.

Moreover, role of Carbon Nanotube based Folded Cascode operational amplifier which is having applications in diverse electronic circuits such as filters, integrators, differentiators etc. The low voltage applications and lower dissipation at nano scale is a extraordinary revolution in the work.

CHAPTER 7

DESIGN AND SIMULATION STUDY OF CARBON NANOTUBE BASED HIGH PASS FILTER

A filter is an important building block of analog circuit. So a fast and efficient signal processing required, which consumed minimum power. The filter probably has its greatest uses in various applications like telemetering apparatus etc, depending on the requirements either attenuation or transmission of signal of particular bandwidth. In this chapter, simulation of CNT based High Pass Filter has done at 45 nm technology using HSPICE for high frequency applications. Design Parameters like technology node, Supply Voltage, Number of CNTs, CNT Pitch, CNT Diameter, Thickness of Oxide, Dielectric Constant and Gate Dielectric were chosen as per design requirements. Performance of the CNT based HPF was analyzed using hspice.

This research work mainly focuses on design and simulation study of CNT based HPFs. There are three latest categories of high pass filters which follows the model of CNT based FET and hspice have been used to design at 45nm technology node. Out of the three types of high pass filters, the first one makes use of N type CNT based FETs as sinks and P type CNT based FETs as sources and is named as pure CNTFET based operational transconductance amplifier. The next two sorts are hybrid technology based operational transconductance amplifier high pass filters. Between the two, one engages a combination of N type CNT based FETs as sinks and traditional P type MOS based FETs as sources known as N type CNT based FET- P type MOSFET - OTA amplifier - High pass filter. Later one is P type CNT based FET -N type MOSFET- OTA – High pass filter employing P type CNT based FETs as sources and traditional N type MOS based FETs as sinks. After the examination, enhancement in many of the performance calculating parameters is remarked in carbon nanotube based FET based operational transconductance amplifier high pass filters, primarily CNTFET based operational transconductance amplifier high pass filter. The comparison analysis of the proposed N type carbon nanotube based field effect transistor-P type MOSFET-OTA - High pass filter, P type CNT based FET-N type MOSFET- OTA– High pass filter and pure CNTFET based operational transconductance amplifier high pass filter with the traditional CMOS based

operational transconductance amplifier high pass filter has shown the increase in bandwidth of around 10% in hybrid and pure carbon nanotube based high pass filters, which is significant for the filter based device. Further, Bandwidth, Output Resistance, Average Power, Phase Margin and Unity Gain Frequency are computed at different voltage level of CMOS –OTA.

7.1 INTRODUCTION

OTA is the very important supreme and multifaceted active device utilized in the productive comprehension of analog ICs. Many benefits are involved with the usage of OTA like big dynamic range, no extra phase affairs, spacious B.W., when compared to an Op-Amp and can work constructively in numerous applications, mainly which have capacitive loads [162-164]. Along with this, the accessibility of an outer I_{bias} in an operational transconductance amplifier expands its versatility and tenability and is the biggest edge of an operational transconductance amplifier [165-167]. OTA suffers from low voltage swing, temperature dependence and hence poor linearity [168-170].

Analyzing equivalent circuit, it is clearly noticed that the output current varies proportionally with the transconductance of the OTA and the difference of the input voltage. The bias current (I_{ABC}) establishes the transconductance. Operational transconductance amplifier is a VCCS,

$$I_{OUT} = g_m (V_1 - V_2) \qquad (1)$$

There are various technologies making use of operational transconductance amplifiers. A high speed operational transconductance amplifier is an outcome of bipolar technology but, as anticipated big power expenditure is one of the prime cases. Moreover, bipolar technology can’t lead to the effective rise in demand of portable devices having large functionality. Under such circumstances, CMOS technology is the best alternative option available. The reason being, that CMOS renders small power, high NM and is wholly suitable for the realization of large combination level circuits. Although, the extension of downsizing of MOS based FET beneath 32 nano meter is especially tough because of SCEs[171-172], increment in leakage current and sensitivity to exercise alterations in integrated circuit manufacturing [132].Due to the above reasons, extremely strong complementary metal oxide semiconductor circuit simulation is becoming troublesome and vital when the size of device is in nano range [49,131,173-174].

A HPF transmits frequencies stop a designated cut-off frequency but attenuates frequencies beneath this. This is abbreviated as HPF. Real estimate of attenuation for each frequency varies from filter to filter. HPFs have many uses like blocking DC from circuits delicate to non-zero normal voltages or radio frequency devices. High pass filters are utilized in conjunction with a LPF to create BPF. The figure 7.1, demonstrates an active HPF.

The cutoff frequency of a basic capacitive high-pass filter is given by :

$$fc = 1/2\Pi R_1 C$$

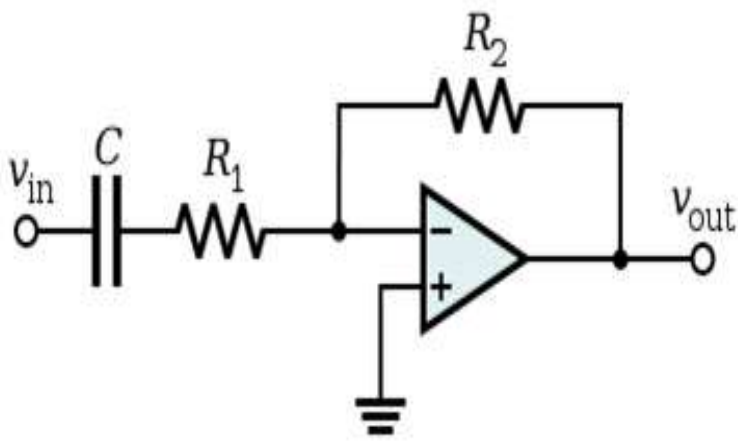


Fig. 7.1 : An active HPF

7.2 CNT BASED FET

The most important application of Carbon Nanotubes is the evolution of Carbon Nanotube based FET [125, 174-176]. Semiconducting type single wall carbon nanotubes are used betwixt S/D electrodes for the realization of channel in CNT based FET. The schematic and Vertex outlook of Carbon Nanotube based FET are given in Figure 7.1**.** Amount of CNTs in the channel is a key factor in resolving the comprehensive achievement and capability of the device, specially the drive current. Carbon Nanotube based FET is similar to that of conventional Metal Oxide Semiconductor FET in terms of working capabilities but it can prove to be a better design. Voltage of gate is responsible for turns ON/OFF of the device and it is capacitively coupled with the channel. Carbon nanotube based FET defeat the conventional metal oxide semiconductor based FET because of diverse benefits. The existence of one dimensional ballistic transfer of charge carriers has led to large

mobility and high drive current (three to four times greater than conventional MOS based FET) in a carbon nanotube based FET [72, 125, 145, 175, 177-182]. Carbon nanotube based FET is known for high g_m, less inherent capacitance, absolute inverse of subthreshold swing(S) and a powerful chemical bond i.e. covalent bond[125,146,181,182-183]. It is even noticed that achievement of CV/I of inherent carbon nanotube based FET is thirteen times superior than that of conventional metal oxide semiconductor based FET[72,174-175,177-181]. CNTs, when used in integrated circuits will mark remarkable augmentation in combination levels of integrated circuits and will feature the legitimacy of Moore's law.

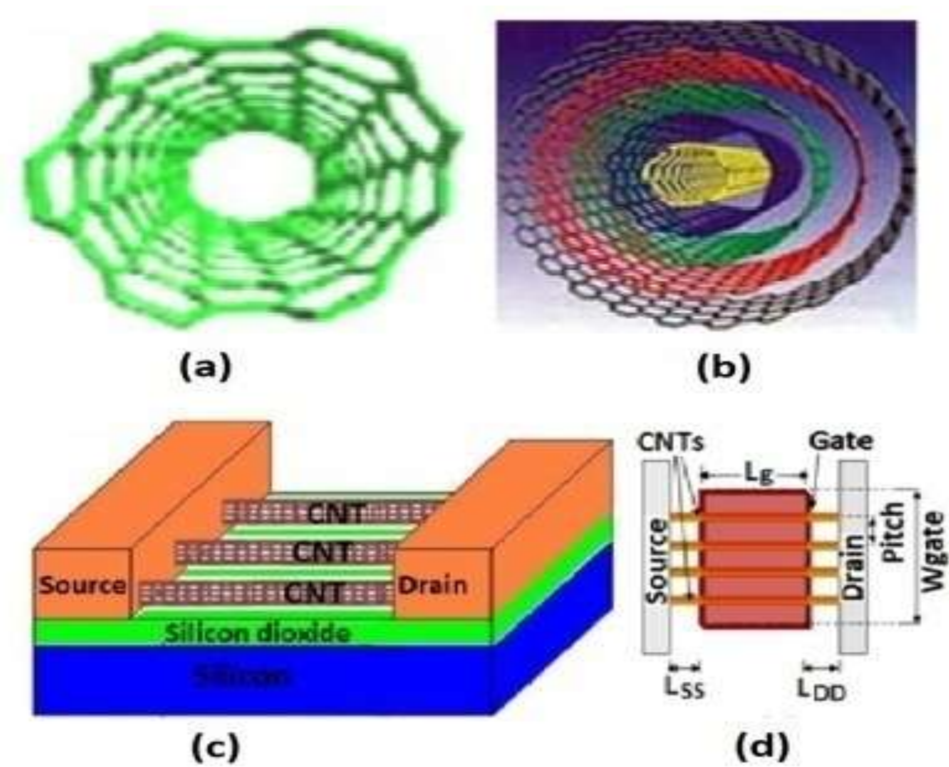
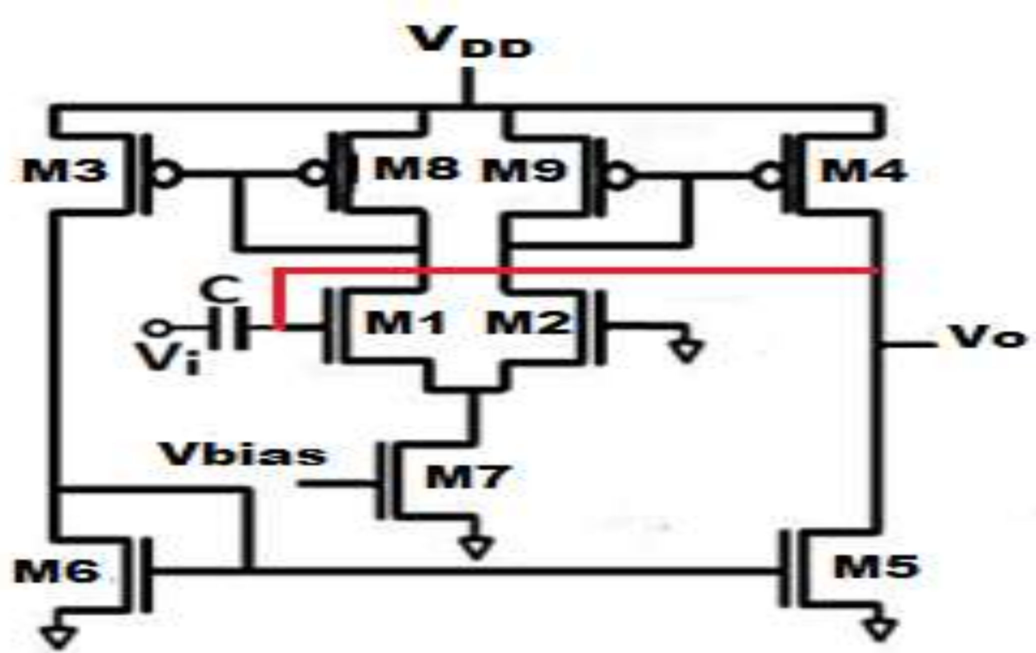


Fig.7.2 : (a) SWNT (b) MWNT (c) Schematic of a Carbon Nanotube based FET (d) Vertex outlook of Carbon Nanotube based FET describing different device variables

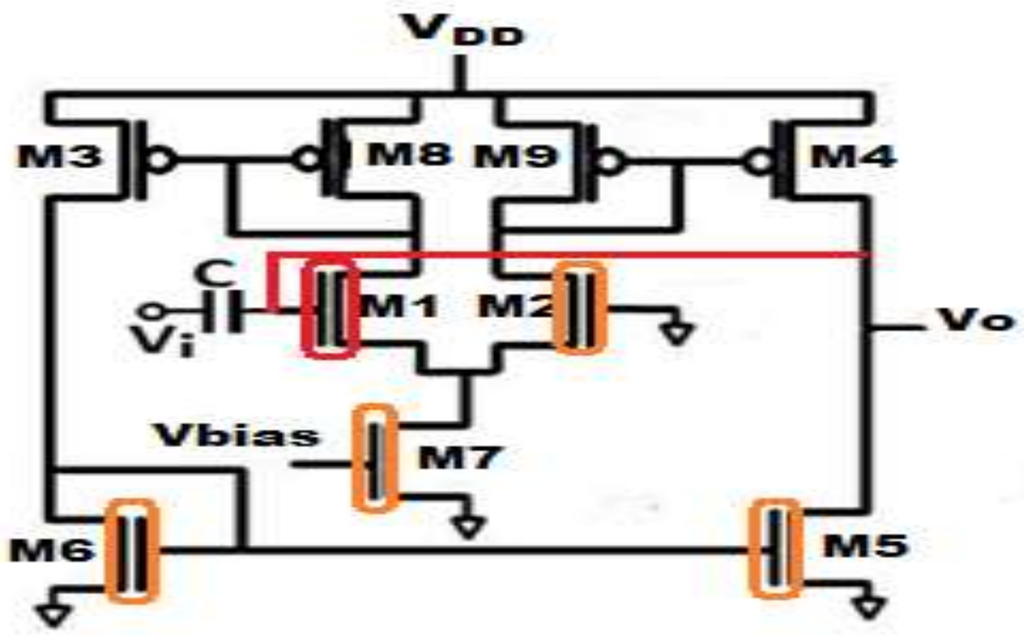
7.3 DESIGN AND SIMULATION STUDY OF CNT BASED HPF

In this research work, there are three latest categories of high pass filters which follow the model of CNT based FET and hspice have been used to design at 45nm technology node. Out of the three types of high pass filters, the first one makes use of N type CNT based FETs as sinks and P type CNT based FETs as sources and is named as pure CNTFET based operational transconductance amplifier. The next two

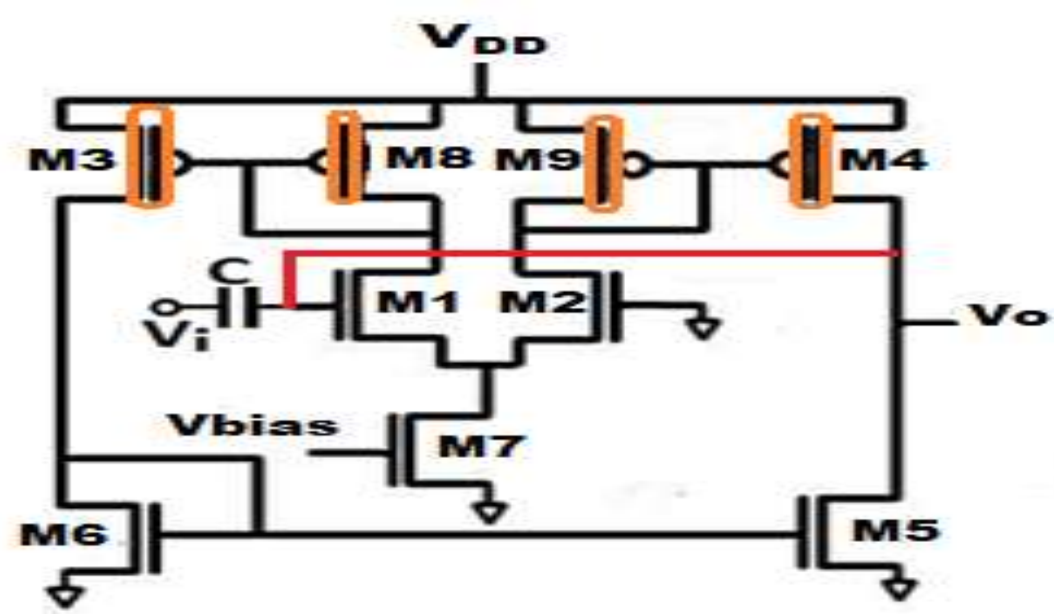
sorts are hybrid technology based operational transconductance amplifier high pass filters. Between the two, one engages a combination of N type CNT based FETs as sinks and traditional P type MOS based FETs as sources known as N type CNT based FET- P type MOSFET - OTA - High pass filter. Later one is P type CNT based FET- N type MOSFET- OTA– High pass filter employing P type CNT based FETs as sources and conventional N type MOSFET transistors as sinks. The comparison between pure CNTFET based operational transconductance amplifier, hybrid OTA-HPFs and conventionally used cmos technology based operational transconductance amplifier high pass filter is necessary. As the Carbon Nanotube innovation is new and another innovation must have clear points of interest over the present solution, must allow new applications and guarantee fundamentally minimal cost to be an effective innovation.



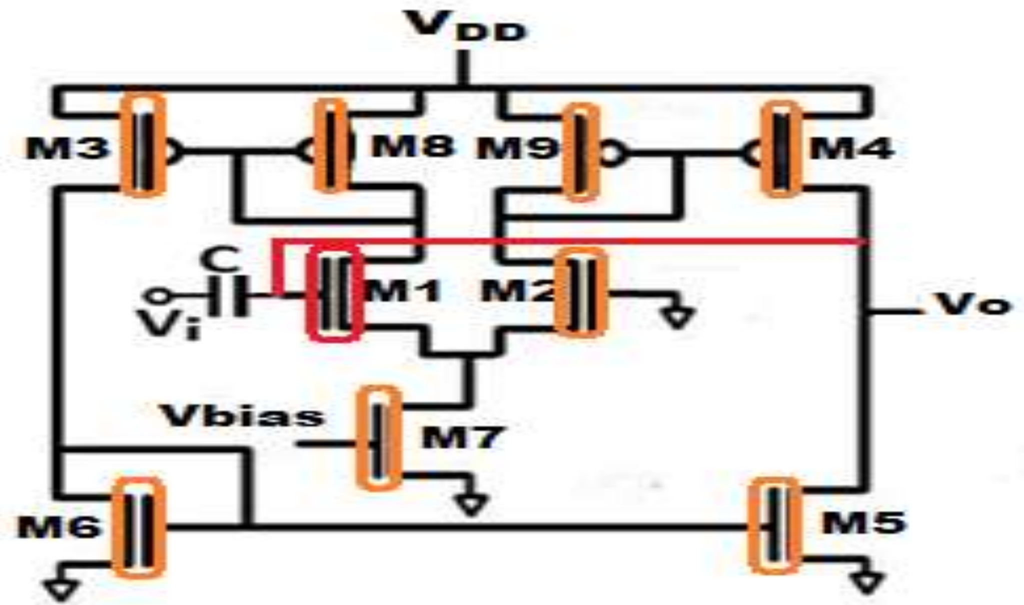
(a) Usual CMOS based operational transconductance amplifier HPF



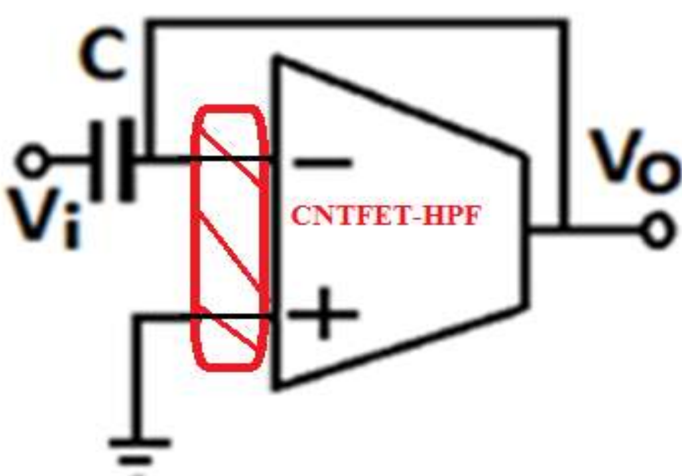
(b) N type CNT based FET-P type MOSFET-OTA-High pass filter



(c) P type CNT based FET-N type MOSFET-OTA–High pass filter



(d) Perfect CNTFET based OTA HPF



(e) Symbol of CNTFET-HPF

Fig.7.3: Different high pass filters using OTAs designed and simulated.

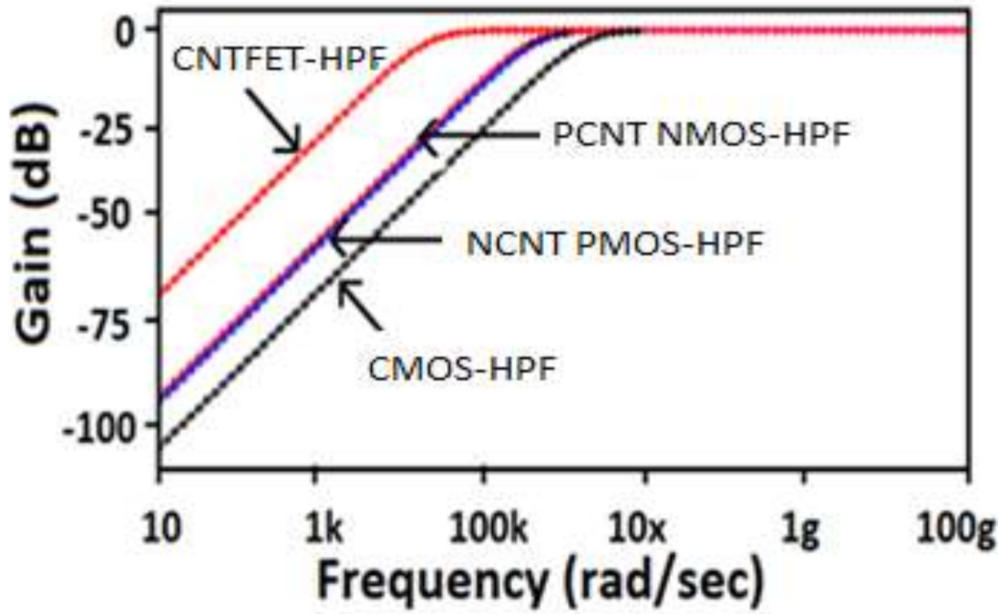


Fig. 7.4: Gain vs Frequency graphs for all Operational Transconductance Amplifier based High Pass Filters

Figure 7.4, shows the Gain vs Frequency graphs for all Operational Transconductance Amplifier based High Pass Filters i.e. CMOS based operational transconductance amplifier high pass filter, N type CNT based FET-P type MOSFET-OTA - High pass filter, P type CNT based FET-N type MOSFET- OTA– High pass filter and pure CNTFET based operational transconductance amplifier high pass filter. After the examination, enhancement in many of the performance calculating parameters is remarked in carbon nanotube based FET based operational transconductance amplifier high pass filters, primarily CNTFET based operational transconductance amplifier high pass filter. The low voltage applications and lower dissemination at nano scale is an astounding development in the work.

Table 7.1: Bandwidth of Conventional and proposed HPFs

S. No.	Parameters	CMOS-HPF	NCNT-PMOS-HPF	PCNT-NMOS-HPF	PURE CNT-HPF
1.	Bandwidth (in Hz)	9.9E+9	9.9E+10	9.9E+10	9.9E+10

The table 7.1 gives the bandwidth of the conventional and proposed high pass filters. The bandwidth of hybrid and pure CNTFET based high pass filter is 9.9×10^{10}Hz,

while for the CMOS based high pass filter, bandwidth is $9.9x10^{9}$Hz. The comparison analysis of the proposed N type carbon nanotube based field effect transistor-P type MOSFET-OTA-High pass filter, P type CNT based FET-N type MOSFET- OTA–High pass filter and pure CNTFET based operational transconductance amplifier high pass filter with the traditional CMOS based operational transconductance amplifier high pass filter has shown the increase in bandwidth of around 10% in hybrid and pure carbon nanotube based high pass filters, which is significant for the filter based device.

Table 7.2: Variation of CMOS- OTA Parameters with Voltage

S. No.	Parameters	0.9V	1V	1.2V	1.4V
1.	Bandwidth (in Hz)	3.3373E+07	7.4164E+07	3.7032E+08	8.8778E+08
2.	Output Resistance (in Ohm)	1.9966k	875.0498	191.4523	73.0815
3.	Average Power (in watt)	4.8323E-05	1.2881E-04	1.4293E-03	2.1660E-02
4.	Phase Margin (in degree)	1.7299E+02	1.6210E+02	1.6281E+02	1.4477E+02
5.	Unity Gain Frequency (in Hz)	6.0188E+06	2.3216E+07	1.1418E+08	5.9366E+08

Further in this research, variation of CMOS-OTA parameters with voltage is analyzed. Bandwidth, Output Resistance, Average Power, Phase Margin and Unity Gain Frequency of CMOS-OTA are computed at different voltage level shown in Table 7.2. This table shows that how the parameters of CMOS based OTA changed, when the supply voltage is 1.4V, 1.2V, 1V and 0.9V respectively. The bandwidth of CMOS-OTA decreases when supply voltage is reduces, which is the main issue of the device. The average power of CMOS-OTA increases, when the supply voltage diminishes.This is the other issue of CMOS-OTA. The output resistance and phase margin of CMOS-OTA also increases when supply voltage decreases. The unity gain frequeny is decreases, when voltage is low. All these parameters are important for the analysis of CMOS-OTA based devices on low supply voltage.

Table 7.3: CNTFET Device Parameter and Values Used

S. No.	Parameters	Default Value
1.	Length of Channel.	45 nm
2.	MFP in Carbon Nanotube channel.	200 nm
3.	Source-side extension.	32 nm
4.	Drain-side extension.	32 nm
5.	Fermi level of doped S/D tube.	0.6 eV
6.	Dielectric constant.	16
7.	Dielectric thickness.	4 nm
8.	Coupling capacitance.	20.0pF/m (for a 10µm thick SiO_2)

7.4 RESULT AND DISCUSSION

This work likewise investigates the analog applications of carbon nanotube based circuits for Nanoelectronics. Unmistakably CNT based FETs are the eventual fate of electronic circuit. CNTFET will assume fundamental part in planning of combinational and sequential circuits which are spine of digital computers.

Encourage, role of Carbon Nanotube based operational transconductance amplifiers High Pass Filters which is outlined in this chapter is having applications in different electronic circuits. The low voltage applications and lower dissemination at nano scale is an astounding development in the work.

Furthermore, carbon nanotube has higher current carrying conductivity more transconductance and both semiconducting cum metallic behavior. So, the proposed circuit is better as far as speed, gain and power. CMOS will be supplanted by CNTFETs in not so distant future because of better properties.

At last, obviously the proposed Carbon Nanotube based operational transconductance amplifiers High Pass Filters are critical building hinders in analog circuits design. This model is ideal for low VLSI applications. The proposed research investigates reduced design in which both CNTFET based circuits and interconnects are comprised of carbon nanotubes.

7.5 CONCLUDING REMARKS

This research work mainly focuses on design and simulation study of CNT based HPFs. There are three latest categories of high pass filters which follows the model of

CNT based FET and hospice have been used to design at 45nm technology node. Out of the three types of high pass filters, the first one makes use of N type CNT based FETs as sinks and P type CNT based FETs as sources and is named as pure CNTFET based operational transconductance amplifier. The next two sorts are hybrid technology based operational transconductance amplifier high pass filters. Between the two, one engages a combination of N type CNT based FETs as sinks and traditional P type MOS based FETs as sources known as N type CNT based FET - P type MOSFET - OTA - High pass filter. Later one is P type CNT based FET- N type MOSFET - OTA– High pass filter employing P type CNT based FETs as sources and traditional N type MOS based FETs as sinks. After the examination, enhancement in almost all of the performance calculating parameters is remarked in CNT based FET based operational transconductance amplifier high pass filters, primarily CNTFET based operational transconductance amplifier high pass filter.The comparison analysis of the proposed N type CNT based FET-P type MOSFET-OTA - High pass filter, P type CNT based FET-N type MOSFET- OTA– High pass filter and pure CNTFET based operational transconductance amplifier high pass filter with the traditional CMOS based operational transconductance amplifier high pass filter has shown the increase in bandwidth of around 10% in hybrid and pure carbon nanotube based high pass filters, which is significant for the filter based device. Further, Bandwidth, Output Resistance, Average Power, Phase Margin and Unity Gain Frequency are computed at different voltage level of CMOS –OTA.

CHAPTER 8
CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION OF THE THESIS

The different analog fundamental building blocks designed and developed in this thesis work incorporate folded cascode operational amplifier, folded cascade operational amplifier based low pass filter and operational transconductance amplifier based high pass filter, all utilizing carbon nanotube field effect transistors. It has been noticed that the CNT based design has many benefits in contrast with the conventional CMOS based designing, but, a few issues should be conveyed to expand the domain of CNT based designing.

In this research work, the benefits of carbon nanotubes and CNT based FETs have been exhibited at the circuitry level, by designing a few eminent signal processing analog circuits. As a considerable measure of CNT based FET based works has been done in the digital field and every single digital block have been composed utilizing CNT based FET, still, analog is nearly unexplored domain. Till date no much important carbon nanotube based designing of analog circuits has been performed.

This has roused us to work in the domain of designing of signal processing based analog circuits using CNT based FET. We began this postulation work with the analysis of CNTFETs. It was followed by the design and simulation of carbon nanotube based FC-Op-Amp. and their AC and Transient analysis. And finally, we have designed carbon nanotube based LPF and HPF in this proposal. The state-of-art work associated to the proposal, essential observations and outcomes from the simulation study have been arranged, in chapter 3 to chapter 7, in the thesis, followed by conclusion and future work in the present chapter.

The different analog fundamental building blocks designed and developed in this thesis work incorporate folded cascode operational amplifier, folded cascade operational amplifier based low pass filter and operational transconductance amplifier based high pass filter, all utilizing CNT based FETs. This has been noticed that the CNT based design has many benefits in contrast with the conventional CMOS based designing, but, a few issues should be conveyed to expand the domain of CNT based designing.

The introduction and motivation behind the thesis work has been given in Chapter 1. Literature review of CNT based nanoelectronic analog and digital applications are provided in chapter 2. The state of the art of CNTs, CNT based FETs and carbon nanotube based analog/digital circuits have been given in this chapter. Chapter 2 also talks about a few models associated with carbon nanotubes and CNT based FETs proposed by different researchers. Furthermore, the favorable circumstances and limitations of carbon nanotubes and CNT based FETs are discussed in detail. Moreover, it talks about the uses of carbon nanotubes in designing analog/digital signal processing circuitry.

Chapter 3 investigates the experiences of the most extraordinary utilization of CNT in electronic field, CNT based FET. The inspiration of research in CNT based FET is fuelled by the novel electrical attributes of CNT specially semiconducting feature. Furthermore, the continuous attempt to discover future nanoelectronic semiconducting device which may perform as magnificent as MOS based FET likewise push the exploration of CNT based FET to be more forceful. The initial segment describes an outline of the structure of CNT based FET followed by the clarification of CNT based FET operation as a semiconducting switching device. The following segment gives the comparison amongst CNT based FET and MOS based FET.In this chapter a comparison is being made between conventional MOSFET and different types of CNTFETs. And finally concluded a future replacement of MOSFET. The major difference in CNTFETs and MOSFET is that it has CNT in channel instead of Silicon. CNTFETs show improved characteristics with scaling of technology. Chirality and diameter of CNTFET directly affects its bandgap which is the biggest advantage over MOS based FETs. Study of various types of CNTFETs is made and a comparison is made in this chapter.

Chapter 4 is dedicated to simulation and analysis of innovative folded cascode Operational Amplifier based on CNTs has been performed utilizing 45 nm node. DC voltage gain, avg. power, B.W. and o/p resistance have been calculated. CNT based folded cascode Op Amp results in high performance with the increase of CNTs. For e.g., the increase in DC gain is 41.48% in pCNT based folded cascode Operational Amplifier and 13.93% in nCNT based folded cascode Operational Amplifier; decrease in average power is by 16.86% in pCNT based Operational Amplifier and 55.42% in nCNT based folded cascode Operational Amplifier in comparison to CMOS based folded cascode Operational Amplifier separately. However, the output

resistance has diminished in carbon nanotube based FC-OP AMP in comparison to traditional complementary metal oxide semiconductor based Folded Cascode OP AMP. The low o/p resistance has resulted in a little B.W. in carbon nanotube based FC-OP AMP. Furthermore, the simulation studies have uncovered that the performance of the CNT based folded cascode Op Amp can be enhanced optimized at various CNTs.

In the next work done in this thesis, that is Chapter 5, also explores the analog applications of carbon nanotube based circuits for Nanoelectronics. Carbon Nanotube Field Effect Transistor (CNTFET) will play vital role in designing of combinational and sequential circuits which are back bone of digital computers. It is clear that CNT based FETs are the future of electronic circuit. This chapter also explores the analog applications of carbon nanotube based circuits for nanoelectronics. In this research chapter, simulation of N Type CNFET based folded cascode Op Amp based on CNT has done at 45 nm technology. N Type CNT based FET based FC-OP-AMP is analyzed through Transient Response. In the Frequency Response of N Type CNTFET based Folded Cascode Op Amp, it is clear that the amplifier is efficiently working since the DC Gain is almost constant upto 1 MHz. It is also clear that the N Type CNTFET based Folded Cascode Op Amp is working as low pass filter, so it has applications in the low pass circuits. Further, it is clear from Phase response that it is stable amplifier. So, we can use it in robust conditions where stability is main concern. Furthermore, it is clear that the amplifier is power efficient since in all the conditions, the Transient Power is in nano watts.

Chapter 6 is dedicated to simulation of Low Pass Filter have done at 45 nm technology using hspice. The simulation result of proposed CNT based FET based LPF show that the frequency response of Low Pass Filters are working satisfactory. It has applications in the low pass circuits. In electronics, these filters are widely used in many applications. Moreover, it is clear from the Phase response of CNT based FET based LPF that it is stable Filter. So, we can use it in powerful conditions where stability is main concern.

In Chapter 7, focuses on design and simulation study of carbon nanotube based HPFs. There are three latest categories of high pass filters which follows the model of CNT based FET and hspice have been used to design at 45nm technology node. Out of the three types of high pass filters, the first one makes use of N type CNT based FETs as sinks and P type CNT based FETs as sources and is named as

pure CNTFET based operational transconductance amplifier. The next two sorts are hybrid technology based operational transconductance amplifier high pass filters. Between the two, one engages a combination of N type CNT based FETs as sinks and traditional P type MOS based FETs as sources known as N type CNT based FET- P type MOSFET - OTA amplifier - High pass filter. Later one is P type CNT based FET -N type MOSFET- OTA – High pass filter employing P type CNT based FETs as sources and traditional N type MOS based FETs as sinks. After the examination, enhancement in many of the performance calculating parameters is remarked in carbon nanotube based FET based operational transconductance amplifier high pass filters, primarily CNTFET based operational transconductance amplifier high pass filter. The comparison analysis of the proposed N type carbon nanotube based field effect transistor-P type MOSFET-OTA - High pass filter, P type CNT based FET-N type MOSFET- OTA– High pass filter and pure CNTFET based operational transconductance amplifier high pass filter with the traditional CMOS based operational transconductance amplifier high pass filter has shown the increase in bandwidth of around 10% in hybrid and pure carbon nanotube based high pass filters, which is significant for the filter based device. Further, Bandwidth, Output Resistance, Average Power, Phase Margin and Unity Gain Frequency are computed at different voltage level of CMOS –OTA.

At lastly, chapter 8 stops the thesis and gives the way for the upcoming work.

8.2 SCOPE FOR FUTURE WORK

The whole work done in the thesis is a simulation analysis. We have not created any of the proposed circuits. Along these lines, this work needs furthermore experimental authenticity. Typically, the real creation is utilized for approval of the simulated work to guarantee reproducibility and reliability of the semiconducting device. Along these lines the circuits proposed in this work ought to be truly created and the issues emerging out of the fabrication must be comprehended and tended to at the simulation and the creation levels. As our concentration in the thesis work was fundamentally on analog type building blocks such as CNT based FET based FC-Op Amp, LPF, HPF. This will be a huge commitment to analog domain circuits, if other building blocks will be designed and simulated utilizing CNT based FETs.

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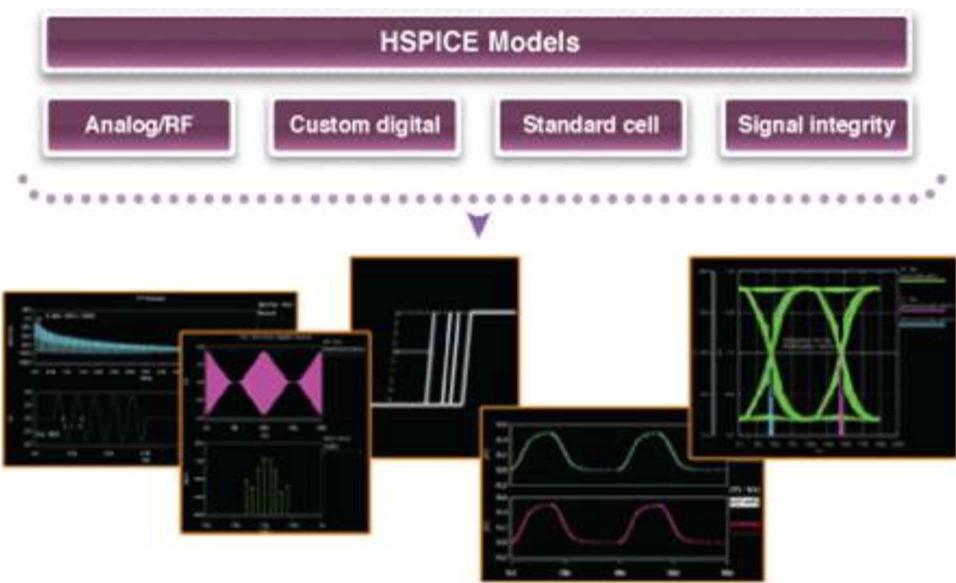
APPENDIX

HSPICE

Along the size of device measurements to accomplish high performance, the necessity of exact circuit simulators becomes salient to capture different impacts, mainly at nano-size. The semiconductor device designers and specialists require advanced and exact circuit simulators to definitely compute and predict the power utilization, timing, yield, functionality and noise etc. of the devices. Numerous circuit simulators have been evolved, such as PSICE, View SPICE, TSPICE, ZSPICE and forecast different performance calculating parameters. Although, HSPICE, the circuit test system evolved by Synopsys is found to be additional efficient and exact. This is being known as enterprises "gold standard" its exactness and proficiency. This has device foundry-authentic MOS based FET models along the state of the art simulation/analysis algorithms. Moreover, this has reasonably precise CNT based FET models that can be utilized for simulation of CNT based FET based circuit.



HSPICE models flow chart

Synopsys HSPICE is an enhancing analog based circuit simulator. We can utilize it to simulate circuits of electrical type in steady-state, transient and frequency area. HSPICE is unequalled for fast, correct circuit and behavioural recreation.

FET TOY

FETToy 2.0 is an arrangement of Matlab scripts which compute the ballistic current-voltage attributes for a traditional MOS based FETs, Nanowire based MOS based FETs and CNT based MOS based FETs. For conventional MOSFETs, FETToy accept a single/double gate geometry and for a NW and NT based MOS based FETs, this expect a cylindrical geometry. Only the lowest is considered, yet it is readily modifiable to incorporate numerous subbands. FETToy 2.0 is utilized for analyze the I-V attributes of CNT based FET in this thesis.

BRIEF PROFILE OF THE RESEARCH SCHOLAR

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LIST OF PUBLICATIONS

List of Published Papers

S. No.	Title of Paper	Name of Journal where published	ISBN / ISSN No.	Volume / Issue	Year	Pages
1.	A Comparative Study of CNFET and Conventional MOSFET	Proceeding of National Conference on “Design & Innovation” organized by Dialogue India held at IIT, Delhi.	81907 0985-2		2017	44-47
2.	A Review : Carbon Nanotube Structures, Properties, Growth and Applications	Nano Trends : A Journal of Nanotechnology and Its Applications (STM Journals)	0973-418X	Vol.-18, Issue 3,	2016	10-22
3.	Design and Simulation of Carbon Nanotube Field Effect Transistor based Low Pass Filter	International Journal of Signal Processing, Image Processing and Pattern Recognition (SERSC Publisher)	2207-970X	Vol.9 No. 10	2016	47-56

4.	Analysis of Carbon Nanotube Field-Effect Transistor	Journal on Circuits and Systems (i-manager's Journal)	2321-7502	Vol.-4. No. 2	2016	22-29
5.	AC and Transient Analysis of N Type Carbon Nanotube Based cum CMOS based Folded Cascode Operational Amplifier	International Journal of Engineering and Technical Research (ER Publications)	2321-0869	Vol.-5, Issue-1	2016	55-58
6.	Simulation and Analysis of Carbon Nanotube Based cum CMOS based Folded Cascode Op Amp	International Journal on Emerging Technologies (Research Trend Publisher)	2249-3255	Vol.- 6, Issue-1	2015	24-29

List of Communicated Paper

S. No.	Title of Paper	Name of Journal	Present Status	Year
1.	Design and Simulation Study of Carbon Nanotube Based High Pass Filter	International Journal of Advanced Science and Technology	Communicated	2019