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May 2024

BCA/BCA(DS) II SEMESTER

Digital Electronics-II (BCA-23-106)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) Which logic family supports maximum fan-out? (1.5)

(b) What is the purpose of a tri-state buffer in digital circuits? (1.5)

(c) How does a flip-flop differ from a latch? (1.5)

(d) Design a 2-bit carry-lookahead adder. (1.5)

(e) What is the significance of clock frequency in digital systems? (1.5)

(f) What is the advantage of state reduction in the design of sequential circuits? (1.5)

(g) Draw the diagram of a 3-bit binary counter. (1.5)

(h) Make a MOD-24 counter essentially using MOD-12 counter. How many JK flip-flop now it has in place? (1.5)

(i) How long will it take to digitize the full-scale signal in an 8-bit counter type A/D converter using a 100 KHz clock? (1.5)

(j) What is meant by quantization error? (1.5)

PART–B

2. (a) Draw NOR gate using CMOS Logic. (05)

   (b) Design a circuit to interface a CMOS output with a TTL input. (05)

   (c) Explain the operation of the parity check code for error detection. (05)

3. (a) Design a 4-bit magnitude comparator circuit and demonstrate its functionality with test cases. (08)

   (b) Explain the NOR gate Logic using of TTL Family, illustrating its merit over other family. (07)

4. (a) Minimize the following using Quine Mcluskey method :

   $f(A,B,C,D) = \pi M\ (1,2,3,8,9,8,10,11,14+d(7,15)$. (10)

   (b) With a truth table and logic diagrams, explain the operation of a four input priority encoder. (05)

5. Design MOD-11 Synchronous up counter. (15)

6. (a) Design a circuit that dedicatedly generates 1110. (10)

   (b) Explain the concept of race conditions in sequential circuits and how they can be resolved. (05)

7. (a) Explain the working of Successive approximation A/D converter, let the V_{ref} = 32 volt and 18.1 volt applied as input. How many clock cycles are needed for the conversion? (10)

   (b) For a voltage to frequency A/D converter, the range of analog input voltage is 0 to 10 V and the corresponding frequency range is 0 to 10 KHz. The A/D converter has a resolution of 8 bits. Find the digital output for the following input voltages :

   (i) 0 V

   (ii) 2.5 V

   (iii) 5V. (05)
