7. (a) Enlist all the steps required for designing a state machine. Explain with a suitable example. **7.5**

(b) A 4-bit ripple carry adder (*Ripple_Add*) contains four 1-bit full adders (FA). **7.5**

(i) Define the modules FA.

(ii) Define the module *Ripple_Add*. Instantiate four full adders of the type FA in the module *Ripple_Add* and call them *fa0, fal, fa2* and *fa3*.

Roll No. ..... Total Pages : 06

015405

May 2024

B. Tech. (ENC) (Fourth Semester)

Digital System Design and Applications

(ECP-405)

Time : 3 *Hours*] [*Maximum Marks :* 75

Note : It is compulsory to answer all the questions (1.5 marks each) of Part A in short. Answer any *four* questions from Part B in detail. Different sub-parts of a question are to be attempted adjacent to each other. Assume data wherever required.

Part A

1. (a) Discuss briefly the concept of Moore and Mealy state machines. Provide examples illustrating the differences between them. **1.5**

(b) Declare three signals, each signal is a *std_logic_vector* with a descending range ending in '0'. The number of elements in the vectors are 14, 8 and 16, respectively. **1.5**

(c) Give a brief description of the evolution of CAD tools. **1.5**

(d) What will be the output of the following Verilog code ? Illustrate the meaning of each statement : 1.5

```
reg [3:0] a = 4'b1010;
reg [3:0] b = 4'b0111;
reg [3:0] result;
always@* begin
result = a & b;
end
initial begin
$display ("Result: %b", result);
end
```

(e) What are the main differences between Wire and Reg ? Give suitable examples. 1.5

(f) If the initial values of A, B, C and D are respectively 10, 20, 30 and 40. After the execution of the following Verilog code, what will be the values for A, B, C and D : 1.5

```
always @(posedge clk)
begin
B <= A;
C <= B;
D <= C;
end;
```


(g) Explain positional and named associations for binding actuals with component locals. 1.5

(h) What is the role of a sensitivity list in behavioral and data flow modeling ? Define its location in both cases. 1.5

(i) Write a procedure that produces the sum, difference and product of two integers, NUMBER1 and NUMBER2. 1.5

(j) Derive the Boolean equation for x from the following architecture body : 1.5

```
architecture ex of ex is
begin
x <= not (not (a or b) or c);
end ex;
```

Part B

2. (a) What are the various design steps for a digital system ? Discuss the role of simulation and synthesis tools in the design. 7.5

(b) What function do the following Verilog modules implement, mention and explain the type of modelling employed in both modules : 7.5

(i)
```
module first (f, a, b, c);
Input a, b, c; output f,
```

wire t;

assign t = (a^ b);

assign f = t & c;

end module

(ii) module second (f, a, b, c);

Input a, b, c; output f,

wire t1, t2;

nand #1 G1(t1, a, b);

or #1 G2(t2, b, c);

nor #1 G3(f, t1, t2); end module

3. (a) Explain the differences between combinational and sequential logic circuits. Provide examples of each type of circuit and discuss their applications in digital design. **7.5**

(b) In a pure combinational circuit, is it necessary to mention all the inputs in the sensitivity list ? If yes, then why ? Write a Verilog code for D-Latch in behavioral modeling. **7.5**

4. Write VHDL code for the 4-bit synchronous and asynchronous decade counter using any modeling. Give complete design procedure for both the counters. **15**

5. (a) What is the significance of delta delay in the simulation process ? Explain different types of delays employed in signal assignment statements. Draw the driver for the signal Z. **7.5**

Process

begin

Z< = 32 after 15 ns;

Wait for 35ns;

Z<= reject 15 ns inertial 22 after 20 ns;

Wait for 45 ns;

Z<= 33 after 15 ns;

Wait;

end process;

(b) Explain operators used in VERILOG with suitable examples. **7.5**

6. (a) Design a four-bit combinational 2's complement circuit. (The output generates the 2's complement of the input binary number). Construct the circuit using XOR gates. Use any HDL for coding. **7.5**

(b) Write a structural style of VHDL code for F=AB+CD. **7.5**