(b) Explain lambda-based design rules for layout designing with neat diagrams. **7.5**

7. (a) What is BiCMOS inverter, explain using clear diagram ? How BiCMOS inverter is different from CMOS inverter ? **7.5**

(b) What is dynamic CMOS logic ? Design NAND gate using dynamic CMOS logic. What are the various issues due to which this style of making circuit is not preferred ? Explain how this issue can be resolved. **7.5**

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009604

May 2024

B.Tech. (EIC) (Sixth Semester)

VLSI Design (EIEL-611)

Time : 3 *Hours*] [*Maximum Marks :* 75

Note : It is compulsory to answer all the questions (1.5 marks each) of Part A in short. Answer any *four* questions from Part B in detail. Different sub-parts of a question are to be attempted adjacent to each other.

Part A

1. (a) Explain the latch up issue in CMOS inverter in brief. **1.5**

(b) What do you understand by the term inverter delay ? How does it affect the performance of the circuit ? **1.5**

(c) What is threshold voltage of a MOSFET ? **1.5**

(d) Why PMOS logic is preferred in Pull Up Network ? **1.5**

(e) What is the difference in two types of power dissipation in CMOS Circuit ? **1.5**

(f) What is Pseudo N-MOSFET ? **1.5**

(g) Why the layout of a circuit is prepared ? **1.5**

(h) What is noise margin for a CMOS inverter ? **1.5**

(i) What is the meaning of 'Sheet Resistance' ? **1.5**

(j) Why do we need a circuit where power dissipation is low ? **1.5**

Part B

2. (a) What is VLSI design flow process ? Explain in detail using flow chart. **7.5**

(b) Explain the design of incrementer/ decrementer using suitable block diagram. **7.5**

3. (a) Describe N well process for fabrication of the CMOS inverter with neat sketches of each step. **7.5**

(b) What do you understand by the scaling of MOS devices ? What are different types of scaling and what are its effects on differen device characteristics ? **7.5**

4. (a) What is drain current ? Derive the expression for the drain current for NMOS in all the regions of operations. Draw the I_{ds} *vs.* V_{as} characteristics curve for NMOS and explain all the region of operation. **7.5**

(b) Using CMOS combinational logic designs draw circuit and stick diagram for $F = AB + C$. **7.5**

5. (a) What is an inverter ? Explain the static and dynamic characteristics of CMOS inverter. Explain the advantages and disadvantages of inverter having different form of pull ups. **7.5**

(b) What do you mean by second order effects in MOSFET ? Explain channel length modulation and sub-threshold conduction in MOSFETs in detail. **7.5**

6. (a) What is transmission gate ? Why is it preferred over NMOS/PMOS switch ? Design half adder using transmission gates. **7.5**