8/12 (90)

Roll No..... Sr. No 017702

December 2023

B.Tech. (EE IOT)- VII SEMESTER

Hardware Description Language for VLSI (EEN-EL4-701)

Time: 3 Hours Max. Marks: 75

Instructions:
1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART -A

Q1 (a) State two features of VHDL. (1.5)

(b) Differentiate between top-down and bottom-up design methodology. Also, state the advantages of each design methodology. (1.5)

(c) State the need of configuration in VHDL. (1.5)

(d) What is sensitivity list. Give its location in behavior and dataflow modeling with example. (1.5)

(e) Explain the need of resolution function. (1.5)

(f) What do you understand by nets in Verilog. Give example. (1.5)

(g) Explain the concept of delta delay in VHDL. (1.5)

(h) List the various components of a Verilog module. (1.5)

(i) State the application of FPGAs and ASICs. (1.5)

(j) Write a wait statement that suspends a process until signal 'ready' changes to 0 or until a maximum of 5ms has elapsed. (1.5)

PART -B

Q2 (a) Compare VHDL and Verilog. (5)

(b) Neatly draw the Y-chart and explain its various domains. Also discuss the capabilities of HDL. (10)

Q3 (a) How the package is shared by other design units. What is the need of package body. (7)

(b) Discuss inertial and transport delay with waveforms. Consider the assignment below, executed at simulation time 100 ns, form the driver for the signal S: (8)

S <= 8 after 20 ns, 2 after 40 ns, 5 after 30 ns, 5 after 65 ns, 10 after 100 ns;

S <= reject 55 ns inertial 5 after 90 ns;

Q4 (a) Explain the data types available in Verilog HDL. Discuss them with necessary syntax and examples. (8)

(b) Discuss system tasks and compiler directives in Verilog (7)

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Q5 (a) Give a gate level description of half adder with relevant block/logic diagram and Verilog HDL source code. (7.5)

(b) Using any modeling style, write a VHDL code for T-flip flop. (7.5)

Q6 (a) What are PLD's. Implement 3-bit Binary to Gray code converter using PROM and PLA. (10)

(b) Explain the architecture of FPGA in detail. (5)

Q7 (a) Compare: (10)

1. Structural, behavioral and dataflow modeling in HDL.
2. Concurrent and sequential statement
3. Exit and next statement
4. Array and record data type in VHDL
5. Simulation and synthesis

(b) Write a HDL source code for MOD-9 asynchronous counter with relevant logic diagram. (5)

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