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015504

December 2023

B.Tech. (ENC) – V SEMESTER

Integrated Circuit Design (ECP–502)

Time : 3 Hours] [Maximum Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any **four** questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) Implement XNOR gate using pass transistors (1.5)

   (b) Discuss the photolithographic process with the help of an example. (1.5)

   (c) Explain accumulation region in MOS transistor with the help of diagram. (1.5)

   (d) What is the minimum amount of voltage required to operate MOSFET? Write the boundary conditions for linear and saturation region. (1.5)

   (e) Discuss the advantages & disadvantages of NORA CMOS logic circuits. (1.5)

(f) At $V_{GS} = 0$, what happens to the channel of Depletion MOSFETs? (1.5)

(g) What is Noise Margin? Explain the method to determine Noise Margin. (1.5)

(h) What happens when the PMOS and NMOS are interchanged with one another in an inverter? (1.5)

(i) With the help of band diagram, explain the concept of surface inversion. (1.5)

(j) Differentiate between pass transistor and transmission gate. (1.5)

PART–B

2. (a) Implement the transistor level circuit for NMOS Full Adder and draw its stick diagram. (8)

(b) Discuss the various short channel effects in detail. (7)

3. (a) Implement the following logic:

$$Y = A\overline{B} + B\overline{C}D + ABC$$

using (i) Complementary CMOS Logic (ii) Domino CMOS Logic. Also mention number of transistor required. (8)

(b) Discuss the VTC characteristics of a resistive load inverter in detail. (7)

4. (a) Consider a CMOS inverter circuit with the following parameters:

$V_{DD} = 4$ V, $V_{T0,n} = 1.5$ V, $V_{T0,p} = -1.5$ V, $k_n = 290$ $\mu A/V^2$ kp = 140 $\mu A/V^2$. Calculate the low noise margin of the circuit. (8)

(b) For 50μm MOS technology, two CMOS inverters are cascaded having equal & minimum feature size of load & driver transistors. Find the power dissipation of a CMOS inverter with $C_L = 0.5$fF. (7)

5. (a) Calculate the delay of a NMOS inverter having feature size:

Stage 1 : $(W/L)_{Load} = 2\lambda/4\lambda$, $(W/L)_{driver} = 2\lambda/2\lambda$
Stage 2 : $(W/L)_{Load} = 2\lambda/8\lambda$, $(W/L)_{driver} = 2\lambda/2\lambda$. (8)

(b) Derive the drain current equation with channel length modulation effect. (7)

6. (a) For an enhancement type MOS transistor the following parameters were measured: $V_{TO} = 1.5$V, K' = 80 $\mu A/V^2$, $V_{GS} = 3.2$V, $V_{DS} = 5$V, $V_{BS} = 0$V, $I_D = 0.48$mA. Find W/L. (8)

(b) Define depletion region charge density. Derive it and explain its importance in terms of threshold voltage. (7)

7. Discuss the various steps to fabricate the p type depletion transistor in detail. (15)
