7. (a) Implement the following using 3:8 line decoder and 4:1 multiplexer:

(i) $Y(A,B,C) = \Sigma m(2,3,4,6)$.

(ii) Full subtracter. (7.5)

(b) What is the function of a sequence generator? Design the same to generate the given sequence 10011100. (7.5)

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December 2023

B.Tech. (ENC) – III SEMESTER

Digital Electronics & Computer Organization

(ECP–301)

Time : 3 Hours] [Maximum Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any **four** questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Assume data wherever required.*

PART–A

1. (a) Simplify :

$$(B+C')(B'+C)+(A'+B+C'). \quad (1.5)$$

(b) Generate hamming code for data 10110 with odd parity. (1.5)

(c) Perform the following conversions:

(i) $(12.0625) = (\ )_2$

(ii) $(1101101111)2 = (\ )_8$

(iii) $(2AC5.D) = (\ )_2$. (1.5)

(d) Construct a 16X1 multiplexer with two 8X1 and one 2X1 multiplexers. Write truth-table for the same. (1.5)

(e) The contents of a four-bit register are initially 0110. The register is shifted six times to the right with the serial input being 1011100 (inputs are applied from right to left). What is the content of the register after each shift? (1.5)

(f) Differentiate RISC and CISC based systems. (1.5)

(g) For converting S-R Flip-Flop to T Flip-Flop, give the values of S and R. (1.5)

(h) Implement the following expression using 8:1 multiplexer:

$$F(A,B,C,D) = \Sigma m(2,4,5,6,9,12,13,14).$$ (1.5)

(i) A 5 bit binary counter starts count from 00000. What will be its count after 145 pulses? (1.5)

(j) How many address lines and data lines are needed, when the memory units have been specified by the number of words times the number of bits per word.

(a) 64K X 8 (b) 2048 X 16. (1.5)

PART–B

2. (a) What is the race-around condition? How does it get eliminated in a Master-slave J-K Flip-flop? What are other possible solutions? (7.5)

(b) What is instruction cycle? Draw and discuss flowchart for (fetch-decode-execute) instruction cycle. Give classification of instructions (with suitable examples) on the basis of operation performed by them. (7.5)

3. (a) Design the circuit of BCD subtracter and explain its operation with suitable examples. (7.5)

(b) Simplify the given Boolean function using K-map or Tabular method:

$$Y = \Sigma m(0,4,8,12,16,18,20,22) + \Sigma d(24,26,28,30,31).$$ (7.5)

4. Design Mod-9 asynchronous and synchronous counters using J-K flip-flop. Explain complete design procedure. (15)

5. (a) An instruction is stored at location 800 with its address field at location 801. The address field has the value 500. A processor register R1 contains the number 900. Evaluate the effective address if the addressing mode the instruction is:

(i) Direct (ii) Immediate (iii) Relative (iv) Register indirect (v) Index with R1 as the index register. (7.5)

(b) Explain the working of CPU and all associated registers. Discuss stored program concept in detail with the help of examples. (7.5)

6. (a) What is an instruction? Classify instructions on the basis of addressing modes, operation performed and number of address fields. (7.5)

(b) Design a 4-bit gray-to-binary converter using truth table, K-maps and logic circuits. (7.5)