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008506

December 2023

B.Tech. (ECE) - V SEMESTER

CMOS Design (ECEL-501)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) What is channel length modulation? (1.5)

(b) Differentiate NMOS and PMOS. (1.5)

(c) What do you mean by threshold voltage of MOSFET? (1.5)

(d) What is sub threshold conduction? (1.5)

(e) How a layout is different from stick diagrams? (1.5)

(f) Why current gets saturated after channel pinch off? (1.5)

(g) What are the advantages and disadvantages of using MOSFET over BJT based ICs? (1.5)

(h) How the depletion MOSFET connected as load in NMOS inverter circuits always remains on? (1.5)

(i) Draw the small signal equivalent model of MOSFET. (1.5)

(j) Enlist the 3 reasons, why power dissipation of portable devices should be minimum. (1.5)

PART–B

2. (a) Explain the different types of IC technology presently used. Also explain the VLSI design flow using suitable flow chart. (8)

(b) Explain the working of enhancement MOSFET with the neat sketches. Also explain shape of the channel of MOSFET for each region -of operation. Derive the equation for the drain current in the all region of operation for NMOS. (7)

3. (a) Describe twin tub process for fabrication of the CMOS inverter circuit. (8)

(b) Explain the different types of inverter configuration. What are the different issues faced with these configurations? Explain how CMOS inverter is offering advantages over other configurations. (7)

4. (a) Explain pseudo NMOS logic and transmission gate logic for inverter circuit. Design 4×1 multiplexer using transmission gate logic. (8)

(b) Draw and explain the static and dynamic characteristics of CMOS inverter. Discuss the effects of W/L ratio of pull up network to pull down network on transfer characteristics. What are the issues of latchup in CMOS inverter? Explain with neat sketches. (7)

5. (a) Enlist the various steps involve in designing a CMOS flip flop circuit logic. (8)

(b) Explain linear and RC delay models. What is logical path effort for MOS circuit? (7)

6. (a) Draw circuit and stick diagram for $F = AB + \overline{A}C$ using CMOS combinational logic design. (8)

(b) Explain how CMOS dynamic logic works and its advantages over static logic circuits. Explain the issue in dynamic logic circuit and how this issue is addressed by Domino logic circuits? (7)

7. (a) Explain power dissipation in CMOS circuits. (5)

(b) Explain design rules for layout makings. (5)

(c) Implement the 2 input XOR gate using NMOS convention. (5)