Roll No. ..... Total Pages : 3

008302

December 2023

B.Tech (ECE)- IIIrd SEMESTER

Digital System Design (EC-302)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) What is radix? Discuss with example. (1.5)

(b) State the De-Morgan's theorem. (1.5)

(c) Convert $(11101101)_2 = (\text{---------})_{\text{gray code}}$. (1.5)

(d) Write the complete expression and logic circuit for the minterm designation $Y = \Sigma m\ (1,3,5,7)$.

(e) Add two BCD numbers, $(0101) + (0110) = (-)_{BCD}$. (1.5)

(f) What are the applications of Multiplexer (MUX)? (1.5)

(g) What are the differences between latch and flip-flop circuits? (1.5)

(h) What are the major differences between register and counter circuits? (1.5)

(i) Define Fan-in and Fan-out? (1.5)

(j) Define VHDL and its uses in digital system. (1.5)

PART–B

2. (a) Design a combinational circuit that generates the 9's compliment of BCD inputs. (10)

(b) Implement the following function using NAND gates only. (5)

$$F = A (B + CD) + BC'.$$

3. (a) Implement a full adder circuit with 3×8 decoder and two OR gates. (5)

(b) Simplify the following expression using K-map.

$$F (A, B, C, D, E) = \Sigma m (0,2,5,7,8,10,16,21,23,24,27,31).$$

(10)

4. Design a synchronous counter for count the sequence 4, 6, 7, 3, 1, 4... avoid lockout condition and use JK flip-flop. (15)

5. (a) What is the race around condition? And how it can be eliminated, discuss through diagram? (5)

(b) Convert the SR to JK flip-flop with the circuit diagram and verify the final circuit through justification. (10)

6. (a) Compare ECL and TTL families on Noise margin, Propagation delay, fan-in, fan-out with minimum 10 points. (10)

(b) Draw TTL with Totem-Pole configuration and explain its working in details. (5)

7. Explain Data types and objects, Dataflow, Behavioural and Structural Modelling, Synthesis in VHDL. Write a program for half adder execution in VHDL. (15)