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008404

May 2023

B. Tech. (ECE) 4th Semester

Computer Architecture (EC-404)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Assume suitable data, if necessary.*

PART–A

1. (a) Draw the basic structure of the computer system. (1.5)

(b) Write down the steps of instruction execution. (1.5)

(c) Convert $(1010.01101)_2$ into hexadecimal number. (1.5)

(d) What is the shared memory multiprocessor system? (1.5)

(e) Why edge triggered clocking always preferred over level-triggered clocking? (1.5)

(f) Perform X-Y using 2's complement arithmetic for the given two binary numbers : X=11011 and Y=10010. (1.5)

(g) Differentiate between RAM and ROM. (1.5)

(h) Explain Arithmetic and Logical Units. (1.5)

(i) Draw the structure of the memory hierarchy. (1.5)

(j) What do you mean by parallel processing and interconnect network? (1.5)

PART–B

2. (a) Explain how information is represented in a computer system and also, explain how representing information in number format is always preferred. (7.5)

(b) Explain Processor organization in detail. (7.5)

3. What do you mean by interrupts? Also, write the steps involved in handling an interrupt request from a peripheral device connected to it. (15)

4. What do you mean by Stack and Queue? Explain the operations associated with Stack and Queue. Also, write an algorithm to add and delete an item in a Stack and Queue. (15)

5. (a) Draw and explain the hardwired control unit organization and encoding function. (7.5)

(b) Draw the microinstruction-sequencing organization of the next-address field and explain it. (7.5)

6. (a) What is meant by Direct Memory Access? Explain the use of DMA controllers in computer systems. (7.5)

(b) Define the locality of reference and explain the use of cache memory and direct-mapped cache. (7.5)

7. Write a short notes on :

(a) Pipelining. (7.5)

(b) Memory Management. (7.5)