CHARACTERIZATION OF GATE ALL AROUND MOSFET

THESIS

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by

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DECLARATION

I hereby declare that this thesis entitled "**CHARACTERIZATION OF GATE ALL AROUND MOSFET**" by **TARUN KUMAR SACHDEVA**, being submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under Faculty of Engineering & Technology, J.C. Bose University of Science & Technology, YMCA Faridabad, during the academic year 2022-2023, is a bona fide record of my original work carried out under the guidance and supervision of **Dr. S. K. Agarwal**, Professor, Electronics Engineering Department, J.C. Bose University of Science & Technology, YMCA Faridabad and **Dr. A. K. Kushwaha** , Professor & Senior Scientific Researcher, The University of Adelaide, South Australia and has not been presented elsewhere.

I further declare that the thesis does not contain any part of any work which has been submitted for the award of any degree either in this university or in any other university.
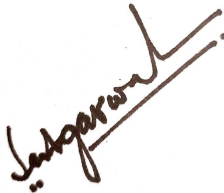
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CERTIFICATE

This is to certify that this thesis entitled "**CHARACTERIZATION OF GATE ALL AROUND MOSFET**" by **TARUN KUMAR SACHDEVA**, submitted in fulfillment of the requirement for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under Faculty of Engineering and Technology, J.C. Bose University of Science & Technology, YMCA Faridabad, during the academic year 2022-2023, is a bonafide record of work carried out under our guidance and supervision.

We further declare that to the best of our knowledge, the thesis does not contain any part of any work which has been submitted for the award of any degree, either in this university or in any other university.

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ABSTRACT

The sustained growth in CMOS VLSI technology is powered by a continuous shrinking of transistors to ever-smaller dimensions. The benefits of miniaturization are high packing density, high circuit speed and lower power dissipation. The downscaling of the device allows the planar transistors to undergo undesired short channel effects, most prominently Drain Induced Barrier Lowering (DIBL) and OFF state leakage current, which increases the power consumption of the device. Several alternative solutions have been proposed to minimize the Short Channel Effects (SCEs). Multi Gate devices are the solution to predict future roadmaps due to their enhanced electrostatic control over the gate and ability to suppress the SCEs. The reduction in channel width and thickness further increases the effectiveness of the gate control. Therefore, the Gate All Around MOSFET (GAA) structure combined with the ultra-narrow body is deemed to be a promising choice for extreme CMOS scaling and replacement of conventional MOSFETs.

This device design demonstrates the effects of several device design factors, such as silicon film thickness and gate work-function, on various device performance parameters, such as threshold voltage, ON current, and OFF current. The metal gate work-function is adjusted to achieve a lower sub-threshold current. The GAA has shown better electrostatic performance with excellent improvement in DIBL and Sub-threshold Slope (SS) however the drive current has to be sacrificed to some extent. During the simulation, it has been observed that the threshold voltage can be adjusted to the desired value by varying the metal gate work-function. Gate All Around MOSFET has been designed to minimize the SCEs and hence improved device performance.

Device thickness is becoming a crucial parameter as more devices can be built on thin film and can integrate multi-gate MOSFETs. This proposed model can achieve a lesser sub-threshold leakage swing which is very much desirable for low-power high-frequency analog integrated circuit applications. It has been observed that threshold voltage increases with an increase in silicon thickness and therefore an improvement has been observed in sub-threshold current. Also, as the silicon thickness reduces, an improvement in Sub-threshold Slope (SS), DIBL, ON/OFF current ratio has been observed. The potential distribution is also estimated analytically in this thesis and various parameters such as electron current density, conduction band, valence band profiles and donor concentration are obtained.

The semiconductor industry has been struggling to maintain the performance of the chip. The first GAA, a vertical nanowire GAAFET known as a Surrounding Gate Transistor, was introduced by Toshiba in 1988. GAA is believed to be the successor to the existing transistors, as it provides better device performance at smaller sizes such as below 7 nm. These transistors are innovative next-generation transistor devices that

have been widely adopted by the industry.

The Cylindrical GAA device is explored in this work and the performance evaluations are carried out with extensive device simulation using SILVACO ATLAS tool. Various electrical characteristics like threshold voltage, ON current, OFF state leakage current, ON/OFF current ratio, DIBL and Sub-threshold Slope(SS) have been extracted and compared with analytical results and the literature work. This work presents a comparative study of 45nm GAA and 30nm GAA to analyse the various parameters affecting the performance of the device.

Dual Material Gate All Around (DMGAA) MOSFET is a novel structure that is designed to combine the benefits of both Gate All Around MOSFET and Dual Material Gate (DMG) structure. Single-material and dual-material CGAA MOSFETs are compared to investigate the impact of the dual material on the device. The DM-CGAA shows a better drive current as compared to a single material. OFF state leakage current is significantly improved in dual material as compared to the single material gate.

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LIST OF SYMBOLS AND ABBREVIATIONS

Symbols	Full Form
I_{on}	ON current
I_{off}	OFF current
L_G	Gate length
N	Doping concentration
Si	Silicon
SiO_2	Silicon Dioxide
t_{ox}	Gate Oxide thickness
Si_3N_4	Silicon Nitride
V_{DD}	Supply voltage
V_{DS}	Drain to Source voltage
V_{GS}	Gate to Source voltage
V_{T0}	Threshold voltage at zero substrate bias
ϕ_f	Work-function
t_{si}	Silicon film thickness
ρ	Charge density
ε	Permittivity
n	Electrons
q	Electron charge
μ_n	Electron mobility
I_D	Drain current
2D	Two dimensional
3D	Three dimensional
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GAA	Gate All Around
CGAA	Cylindrical Gate All Around
CMOS	Complementary Metal Oxide Semiconductor
DIBL	Drain Induced Barrier Lowering
SS	Subthreshold Slope
EOT	Equivalent Oxide Thickness
ITRS	International Technology Roadmap for Semiconductors
TCAD	Technology Computer Aided Design
SCE	Short Channel Effects
NEGF	Non Equilibrium Green's Function
SOI	Silicon on Insulator
FDSOI	Fully Depleted Silicon on Insulator

CHAPTER 1

INTRODUCTION

1.1   INTEGRATED CIRCUIT EVOLVEMENT

The electronics industry has indeed made remarkable progress over the years. The integration of technological advancements, such as the miniaturization of electronic components, the development of more powerful processors, and the advancement of materials science, has enabled the creation of larger and more complex devices, as well as smaller and more efficient ones [1]. The supported development in VLSI innovation is fulfilled by reducing the size of transistors to smaller dimensions [2]. These advancements have enabled the development of technologies such as smartphones, laptops, and other mobile devices and complex systems that are more powerful, compact, and energy-efficient than ever before. Gordon Moore observed in 1965 that the number of transistors on a microchip doubles approximately every two years and held true for several decades and has been a driving force behind the rapid progress of the electronics industry. [3, 4].

1.1.1   MOSFET Scaling Technology

The rapid decrease in the cost of electronic devices has been a major factor in driving the development of new applications and gadgets. By miniaturization, more circuits can be placed on every silicon wafer and consequently each circuit cost decreases [5]. The speed and power consumption of electronic devices can be improved by dimension downscaling. MOSFET scaling theory refers to the principles and considerations involved in scaling down Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) as a means of improving their performance and integration density. In semiconductor scaling, every time feature size of the device is decreased, a

1

new technology node has been innovated [6], for example the term 30nm device refers to a device that has been fabricated using a technology node with a nominal feature size (typically gate length) of approximately 30 nanometers. Scaling theory guides the design and fabrication of MOSFETs by addressing various physical and electrical effects that arise when transistor dimensions are reduced [7]. The primary benefit of new technology node is that the circuit size decreases by 2 [8]. Since with every novel technology node innovation, almost double the number of circuits can be placed, therefore devices become less expensive. Scaling is the factor that pushes down the cost of the appliance [9, 10].

1.1.2 Types of Scaling

There are mainly two different types of scaling alternatives:

I. Constant Field Scaling

II. Constant Voltage Scaling

I. Constant Field Scaling

In this scaling method, the physical measurements of a MOS transistor are scaled down by a scaling factor $(S > 1)$. Constant-field scaling is designed in such a way, that the MOSFET's electric field remains steady [1]. Table 1.1 shows potentials, device sizes and doping concentration details in constant-field scaling theory.

Table 1.1: MOSFET scaling factors of constant field

	Before Scaling	**Constant Field Scaling**
Channel Length	L	L' = L/S
Channel Width	W	W' = W/S
Channel Area	A	A' = A/S
Gate Oxide Thickness	t_{ox}	$t'_{ox} = t_{ox}/S$
Supply Voltage	V_{DD}	$V'_{DD} = V_{DD}/S$
Gate to Source Voltage	V_{GS}	$V'_{GS} = V_{GS}/S$
Drain to Source Voltage	V_{DS}	$V'_{DS} = V_{DS}/S$
Threshold Voltage	V_{th}	$V'_{th} = V_{th}/S$
Doping Densities	N_A	$N'_A = N_A \times S$
	N_D	$N'_D = N_D \times S$

The constant field theory, which assumes that a strong electrical field is negligible and the electrical characteristics of the MOSFET is not damaged as a result of device shrinkage. By downscaling using the constant-field theory, the propagation delay reduces, which results in fast switching operations [11]. Since more components are placed on-chip to make the circuit more efficient, there can be a heating problem. But in this theory, as the power density remains constant, so cooling of circuits is not a concern. However, it needs a drop in the supply voltage with device downscaling [12]

Now, the impact of constant field theory on various device performance parameters like ON current, Gate oxide capacitance, Trans-conductance, Power dissipation, and Power density has been calculated as below.

$$\text{Gate oxide capacitance, } C'_{ox} = \frac{\varepsilon_{ox}}{t'_{ox}} = S.\frac{\varepsilon_{ox}}{t_{ox}} = S.C_{ox} \tag{1.1}$$

$$\text{Trans-conductance, } k_n' = \mu_n.C_{ox}'.\frac{W'}{L} = S.k_n \tag{1.2}$$

$$\text{Drain current, } I'_D(\text{lin}) = \frac{k'_n}{2} \cdot \left[2 \cdot \left(V'_{GS} - V'_{th} \right) V'_{DS} - V'^2_{DS} \right]$$

$$= S \cdot \frac{k_n}{2} \cdot \frac{1}{S^2} \cdot \left[2 \cdot \left(V_{GS} - V_{th} \right) V_{DS} - V^2_{DS} \right]$$

Therefore

$$I'_D(\text{lin}) = \frac{I_D(\text{lin})}{S} \tag{1.3}$$

$$I'_D(\text{sat}) = \frac{k'_n}{2} \cdot \left(V'_{GS} - V'th \right)^2$$

$$= S \cdot \frac{k_n}{2} \cdot \frac{1}{S^2} \cdot \left(V_{GS} - V_{th} \right)^2$$

Hence

$$I'_D(\text{sat}) = \frac{I_D(\text{sat})}{S} \tag{1.4}$$

Static Power dissipation,

$$P' = V'_{DS} \cdot I'_{DS} = \frac{1}{S^2} \cdot V_{DS} \cdot I_{DS}$$

Hence

$$P' = P/S^2 \tag{1.5}$$

Power dissipation density,

$$P'_d = \frac{P'}{(W' \cdot L')} = P_d \tag{1.6}$$

II. Constant Voltage Scaling

Constant voltage scaling has been chosen over constant field scaling mostly since it might be a practical solution for existing appliances. But in this theory, as the device geometry shrinks, the electric field increases which leads to velocity saturation, V_t roll-off, increased OFF current, mobility degradation etc. Now, we can calculate the impact of constant voltage theory on various device performance parameters like ON current, Gate oxide capacitance, Trans-conductance, Power dissipation and Power density as below.

$$\text{Gate oxide capacitance, } C'_{ox} = \frac{\varepsilon_{ox}}{t'_{ox}} = S \cdot \frac{\varepsilon_{ox}}{t_{ox}} = S.C_{ox} \tag{1.7}$$

$$\text{Trans-conductance, } k'_n = \mu_n \cdot C'_{ox} \cdot \frac{W'}{L'} = S \cdot k_n \tag{1.8}$$

$$\text{Drain current, } I'_D(\text{lin}) = \frac{k'_n}{2} \cdot \left[2 \cdot \left(V'_{GS} - V'_{th} \right) V'_{DS} - V'^2_{DS} \right]$$

$$= S \cdot \frac{k_n}{2} \cdot \left[2 \cdot \left(V_{GS} - V_{th} \right) V_{DS} - V^2_{DS} \right]$$

Therefore

$$I'_D(\text{lin}) = S.I_D(\text{lin}) \tag{1.9}$$

$$I'_D(\text{sat}) = \frac{k'_n}{2} \cdot \left(V'_{GS} - V'\text{th} \right)^2$$

$$= S \cdot \frac{k_n}{2} \cdot \left(V_{GS} - V_{th} \right)^2$$

Hence

$$I'_D(\text{sat}) = S.I_D(\text{sat}) \tag{1.10}$$

Static Power dissipation,

$$P' = V'_{DS} \cdot I'_{DS} = V_{DS}.S.I_{DS}$$

Hence

$$P' = S. P \tag{1.11}$$

Power dissipation density,

$$P_d' = \frac{P'}{(W' \cdot L')} = S^3 \cdot P_d \tag{1.12}$$

Table 1.2 shows details of the constant voltage scaling theory

Table 1.2: MOSFET scaling factors of constant voltage

	Before Scaling	Constant Voltage Scaling
Channel Length	L	L' = L/S
Channel Width	W	W' = W/S
Channel Area	A	A' = A/S
Gate Oxide Thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Supply Voltage	V_{DD}	$V_{DD}' = V_{DD}$
Gate to Source Voltage	V_{GS}	$V_{GS}' = V_{GS}$
Drain to Source Voltage	V_{DS}	$V_{DS}' = V_{DS}$
Threshold Voltage	V_{th}	$V_{th}' = V_{th}$
Doping Densities	N_A	$N_A' = N_A \times S^2$
	N_D	$N_D' = N_D \times S^2$

1.1.3   CMOS Power Consumption

A complementary MOSFET circuit consists of two MOSFETs as shown in Figure 1.1 The pull-up network comprises of p-type MOSFET and the pull-down network comprises of n-type MOSFET. Gates of both MOSFETs are joined together to the input.
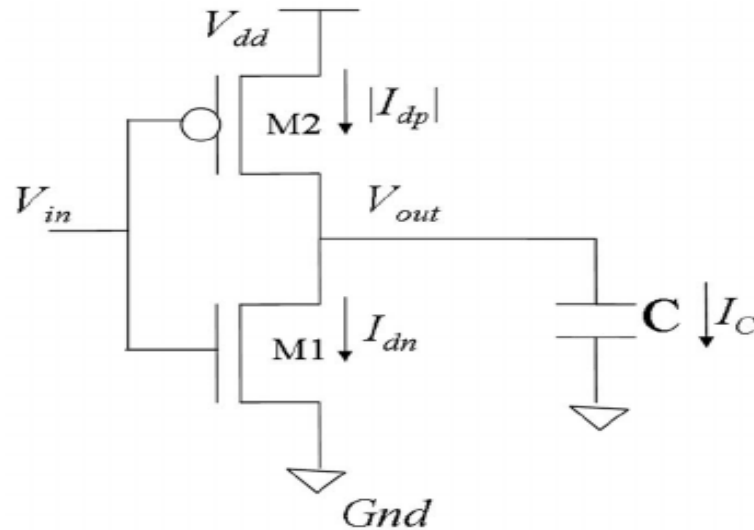
Figure 1.1: Schematic diagram of CMOS inverter.

In complementary MOSFET, at steady-state one transistor is at on state while the other is at off state. Thus, only the off state leakage current is effective at a steady state. When input shifts, the load capacitance (C_L) of the next stage is charged completely. Therefore, a decrease in off state leakage current is very essential for the decrease of static power consumption.

As the gate length reduces, the clock frequency of integrated circuits also increases which results in an increase in dynamic power consumption. On the other hand, sub-threshold leakage current and oxide leakage current exponentially increased. The oxide thickness is reduced to increase the gate electrostatic controllability which results in the flow of oxide leakage current in the device. An alternate solution to reduce oxide leakage current is to use high k oxide material [13].

1.1.4 Various Short Channel Effects

The short channel effects (SCE) appears as the gate length of MOSFET decreases. Threshold voltage of MOSFET decrease as the gate length decreases, which is a roll-off of the threshold voltage.Also as channel length decreases short channel effects yields to sub-threshold leakage current. Two physical phenomena are directly related to short channel effects: Constraints carried out on electric drift characteristics in the channel and changes in threshold voltage owing to the shortening length of the channel.The various short channel effects are given below:

1. Velocity Saturation

2. Surface Scattering

3. Drain-Induced Barrier Lowering & Punch Through

4. Impact Ionization

5. Hot Electrons

1. **Velocity Saturation**

   As the device size reduces, the electric field invariably increases and the carrier is transported into the channel with enhanced velocity. As electrical field along the channel reaches a critical value the velocity of carriers tends to saturate and the mobility degrades.This velocity saturation is affected by the enhanced scattering speed of extremely active electrons. As shown in Figure 1.2 the electric field in the material is increased, the electrons will accelerate and reach a maximum

velocity, after which they will no longer accelerate even if the electric field is increased further. This maximum velocity is known as the saturation velocity.
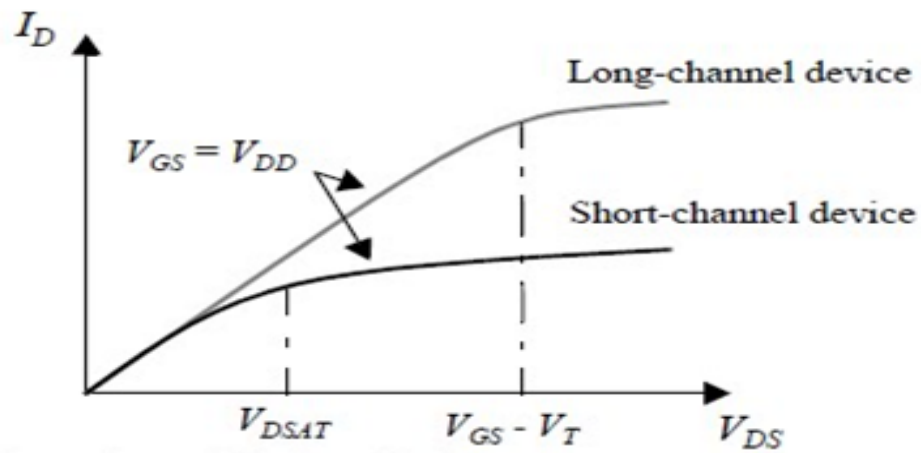
Figure 1.2: Velocity saturation effect.

2. **Surface Scattering** Surface scattering is a phenomenon that occurs in short channel devices, where the distance between the source and drain regions is relatively small.As the channel length decreases (due to the adjacent expansion of the depletion layer into the channel region), the longitudinal electric field component increases and surface mobility becomes field-dependent. The surface scattering effect is shown in Figure 1.3.
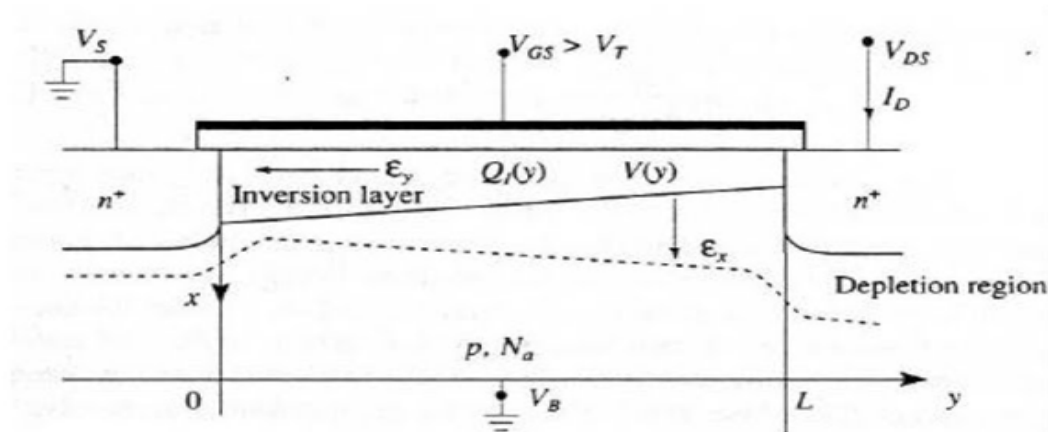
Figure 1.3: Surface scattering

In short channel devices, the electrons flowing through the channel can interact with the surface of the semiconductor material, which can cause scattering and lead to a decrease in the device's performance.

3. **Drain-Induced Barrier Lowering & Punch-Through**

In short-channel MOSFETs, both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS} controls the potential barrier. When the drain voltage is increased, the barrier height of the channel is reduced even more, ultimately allowing electron flow between source and drain, even if the voltage from the gate to the source is smaller than the threshold voltage. This leads the threshold voltage to drop even further. Eventually, when the gate completely loses channel control, the punch-through condition occurs and a high drain current exists independent of gate voltage. The DIBL effect is shown in Figure 1.4
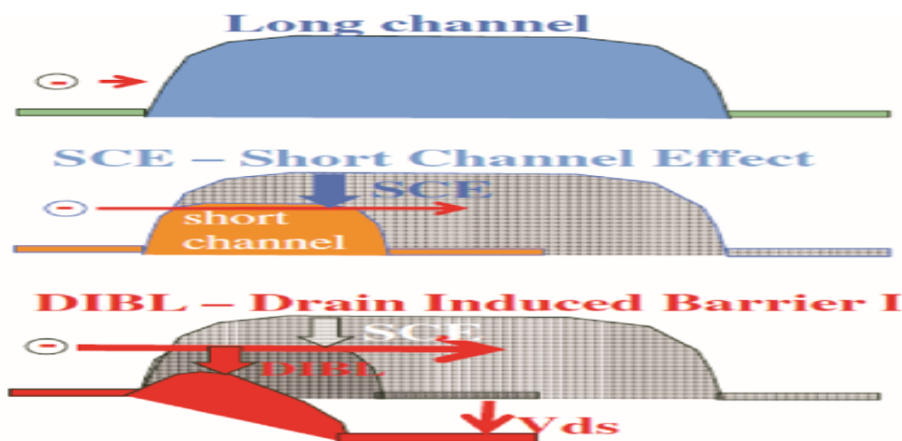
Figure 1.4: DIBL effect

4. **Impact Ionization**

Impact ionization is the process in a material that allows one energy carrier to lose energy by creating other charging carriers. In semiconductors, an electron (or hole) with sufficient kinetic energy can push a bound electron from the valence band and remote it to the conduction band, creating an electron-hole pair. If this happens in a high electric field region, it may result in avalanche breakdown.

5. **Hot Electrons**

As the device size reduces, the hot electron effect is perceived owing to the presence of the high transverse and lateral electric field. The resulting increase in the electric field intensity leads the electrons to raise their velocity. Few high-energy electrons can leave the silicon body and tunnel into the gate oxide. During

the motion, some of the electrons may be trapped into the oxide which leads to a high threshold voltage. A minimum electric field of 10^4 V/cm is required for an electron to become a hot electron. The devices having channel length around or below 1μm, this condition is readily encountered [14].

An alternative way for short channel effects like V_t roll-off and DIBL is to improve electrostatic control of the channel. Electrostatic control of the channel can be improved by:

    I. Improving efficient carrier mobility while maintaining the gate length

   II. Improving the MOSFET's gate capacitance

  III. Implementing three-dimensional design architecture

However, alternatives I and II have achieved the limit of downscaling the device. Therefore, alternative III is the best & last option to adopt.

1.1.5   ON/OFF Current Ratio Optimization

A certain quantity of charge must be transmitted with each CMOS circuit node during input switching based on the load capacitance at the node. The value of drive current has a significant impact on how fast the input data is transferred to the output. Therefore, a high ON current and a low OFF current are required. However, ON current and OFF current depend on each other which implies neither of them can be set independently. However, if the threshold voltage is lowered to increase the ON current, the leakage current will also increase. So the optimal ratio of ON current and OFF state leakage current is required.

1.2   SINGLE GATE TO MULTI GATE MOSFET ARCHITECTURES

1.2.1   Introduction of Multi-gate Structures

In Fully depleted Silicon On Insulator (SOI), MOS is placed over an ultra-thin oxide layer which isolates the cell from the body [15]. A very thin silicon layer is deposited on top of the oxide layer that functions as a channel [16]. It has less junction capacitance due to the buried oxide layer under the source and drain regions which leads to a decrease in load capacitance.

In this technology, a junction interface exists at the surface of the source/drain junction. Thus, source/drain junction region is smaller than the bulk CMOS devices which leads to a decrease in various leakage currents like Gate Tunneling current, Gate Induced Drain Leakage (GIDL) etc. Although since the electric field from the drain side penetrates the buried oxide layer and impacts channel potential, therefore too dense & too thin buried oxide layer is not beneficial for smaller geometry [17]. Therefore to reduce short channel effects, a multi-gate structure is needed. In multi-gate architecture more than a single gate is used to suppress short channel effects and OFF state leakage current [18].

1.2.2 Double Gate MOSFET

Double gate MOSFET was the first multi-gate MOSFET as shown in Figure 1.5. In double gate MOSFET, short channel effects can be suppressed considerably due to better electrostatic control of the channel by sandwiching a fully depleted SOI device between two linked gate electrodes [19]. The voltage applied to the gate terminal regulates the electric field, which defines the amount of channel current flow [20, 21].
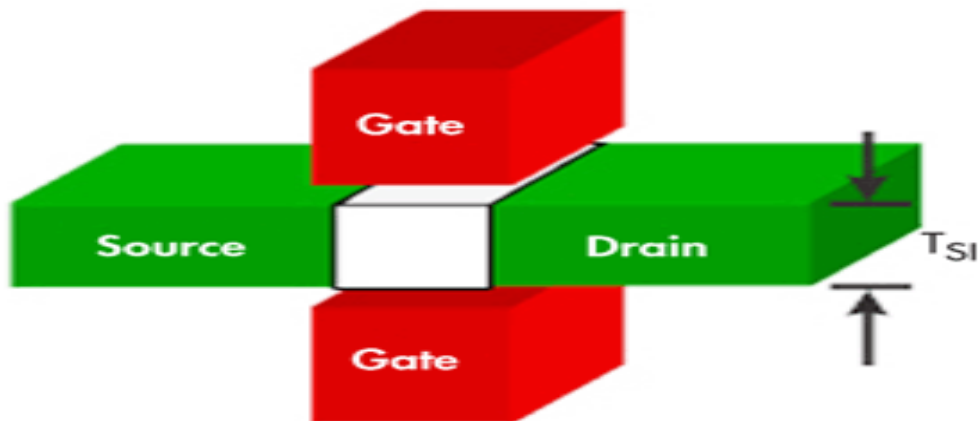
Figure 1.5: Structue of Double gate MOSFET

The advantages of Double gate MOSFET are:

- Suppression of short channel effects

- High I_{on}/I_{off} current ratio

- Easy fabrication

- Better electrical characteristics

1.2.3   FinFET

FinFET is a non-planar, nano-scale field-effect transistor (FinFET) is a three-dimensional (3D) structure, having conducting channel elevated so the gate can surround it on three sides[22, 23]. The structure of the FinFET is shown in Figure 1.6. It has significant advantages over the planar MOSFET.
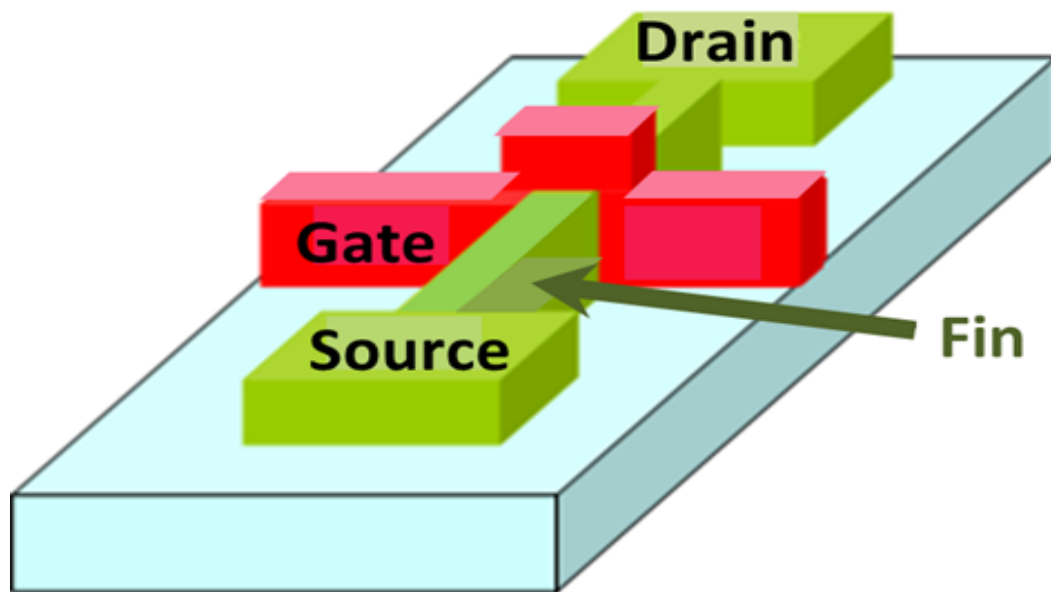
Figure 1.6: Structure of FinFET transistor

- Higher drive current

- The device offers high switching speed and low power consumption due to lower capacitance

- High I_{on}/I_{off} current ratio

- It helps to reduce short channel effects due to higher electrostatic channel control[24]

1.2.4   Gate All Around MOSFET

Gate All Around MOSFET is a better device than FinFET due to its gate coupling that controls the channel more correctly and efficiently, also having a better sub-threshold leakage current [18].

The structure of the Gate All Around MOSFET is shown in Figure 1.7. The design of Gate All Around achieves the above criterion by using the smallest gate length having the same silicon thickness [25].
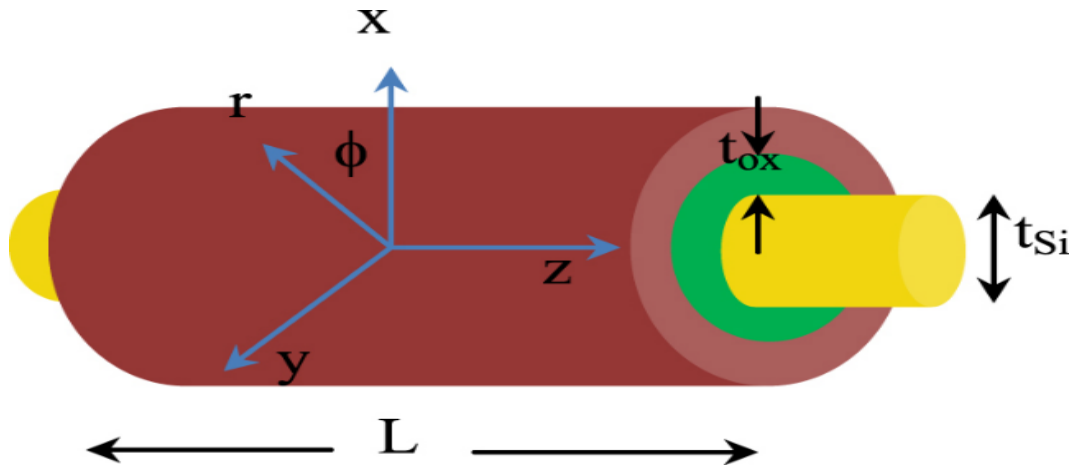
Figure 1.7: Structure of Gate All Around MOSFET

On the other side, it is permitted to accomplish the criterion at the same gate length by having the largest silicon body thickness. Therefore GAA MOSFET structure is a promising solution to suppress short channel effects.

Figure 1.8 indicates that the lower gate length for the criterion is permitted as the thickness of the silicon body reduces [26]. Thus GAA FET, which has a narrow silicon channel diameter, has the greatest advantage.
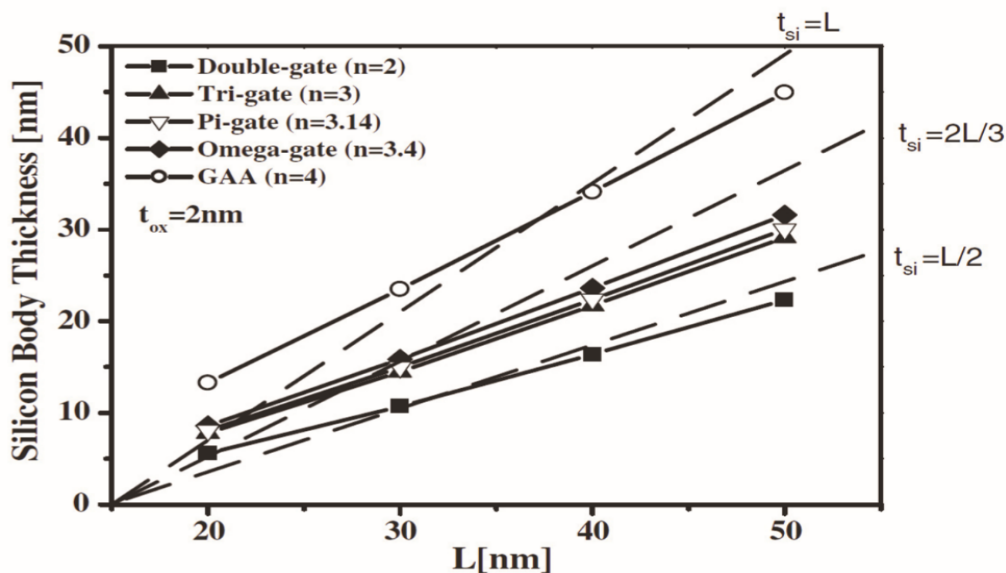
Figure 1.8: Criteria to achieve Sub-threshold Swing less than 75mV/dec and DIBL less than 50mV/V

1.3   OBJECTIVES

The main aim of the proposed work is to carry out research contributions leading to innovating future devices, keeping the silicon technology as the base technology by overcoming the short channel effect. The goal will be achieved by breaking the work into the following objectives.

- To study & design Cylindrical Gate All Around MOSFET

- To simulate & analyse the extraction of various characteristics like Threshold voltage, Current-Voltage characteristics, Drain current, Sub-threshold leakage current, I_{on}/I_{off} ratio, DIBL & Sub-threshold Swing etc.

- To analyse the effect of various device parameters like gate work function, silicon film thickness etc.

- To study the effect of dual material Gate All Around MOSFET & its comparison with single material Gate All Around MOSFET

1.4   OVERVIEW OF THE THESIS

The overall thesis is divided into the following chapters.

Chapter 1- Introduction

A detailed review of scaling theory, the evolution of integrated circuits with scaling technology and the introduction of multi-gate devices are presented. The primary thought is to discuss the existing problems focusing on threshold voltage, ON current, OFF current, ON/OFF current ratio, DIBL & Sub-threshold Slope of the device. The expectation of Gate All Around MOSFETs is described keeping previous research in mind. In this chapter, the objectives of the thesis are also discussed.

Chapter 2- Literature Review

This chapter provides a survey of existing MOSFET scaling and short channel effects research and on-going problems. This chapter along with the scaling theory also describes the physics behind the issue. The main sources of variation will then be discussed outlining their impacts on device and circuit efficiency. It presents the conventional existing MOSFET structures, enhancement techniques and recent trends to enhance the performance of the device.

Chapter 3- Device Fabrication and TCAD Simulation

In this chapter, various fabrication approaches of Gate All Around MOSFETs are reviewed. Also, describe the device design guidelines as per the International Technology Roadmap for Semiconductor (ITRS). Process modeling in TCAD gives an approach to predicting the impact of process parameters on circuit characteristics.

Chapter 4- Electrical Characteristics of Gate All Around MOSFET

In this chapter, the drain characteristics of 45nm and 30nm Cylindrical Gate All Around (CGAA) are explored and the performance evaluation is carried out with an extensive device simulator. Various electrical characteristics have been extracted i.e. Drain current (I_{on}), Sub-threshold current (I_{off}), DIBL, Sub-threshold slope, I_{on}/I_{off} ratio after the simulation of the device in ATLAS. Also, the output (I_D–V_{DS}) and transfer (I_D–V_{GS}) characteristics of GAA FET have been plotted.

Chapter 5- Impact Analysis of various design parameters

In this chapter, 45 nm Gate All Around devices have been designed with different gate work functions ranging from 4.4 eV to 4.6 eV. The sensitivity of gate work function on various performance parameters like threshold voltage, ON current, OFF current, ON/OFF current ratio, DIBL etc. of Cylindrical Gate All Around MOSFETs are evaluated & analyzed. Also, short channel characteristics of 45nm, Cylindrical Gate All Around MOSFETs with variation in silicon film thickness ranging from 2.5 nm to 10 nm are extracted and evaluated. The effects of the silicon film thickness of Cylindrical Gate All Around MOSFETs on various performance parameters like threshold voltage, ON current, OFF current, ON/OFF current ratio, DIBL etc. are evaluated & analyzed.

Chapter 6- Dual Material Gate All Around MOSFET

In this chapter, an analysis of the performance dependency of dual material on device geometry variation has been presented. Dual material Gate All Around MOSFET uses two materials having different work functions for the gate region. Various performance parameters like ON current, OFF current, ON/OFF current ratio, DIBL etc. are evaluated, analyzed & compared with a single material All Around MOSFET.

Chapter 7- Conclusion & Future Scope

In this chapter conclusion & outcome of the thesis work are covered with future scope.

CHAPTER 2

LITERATURE REVIEW

2.1 MOSFET SCALING TRENDS AND CHALLENGES

MOSFET scaling refers to the process of reducing the size of MOSFET transistors in integrated circuits in order to increase their performance and functionality. Over the past few decades, MOSFET scaling has been the primary driver of the rapid advancements in microelectronics technology. However, as MOSFETs are scaled down to smaller and smaller sizes, new challenges arise that can limit their performance and functionality [27,28]. Here are some of the current trends and challenges in MOSFET scaling:

- Short channel effects: As MOSFETs are scaled down, the channel length of the transistors becomes shorter. This can cause the drain and source regions to become closer together, which can lead to increased leakage current and reduced transistor performance.

- Gate leakage: As the gate oxide thickness is reduced in scaled-down MOSFETs, gate leakage current can become a significant issue. This can lead to increased power consumption and decreased reliability.

- Mobility degradation: As MOSFETs are scaled down, the mobility of the electrons in the channel region can decrease due to increased scattering caused by lattice defects and impurities.

- Variability: As MOSFETs are scaled down, the variability in transistor performance due to manufacturing variations becomes more significant. This can lead to increased power consumption and reduced performance.

- Heat dissipation: As MOSFETs are scaled down, their power density increases, which can make it challenging to dissipate heat generated by the transistors. This can lead to reduced reliability and lifespan.

- Material challenges: As MOSFETs are scaled down to smaller sizes, new materials and processes are required to fabricate them. This can lead to challenges in finding suitable materials that are compatible with the manufacturing process and can meet the performance requirements.

- Economic challenges: As MOSFET scaling becomes more difficult, the cost of developing and manufacturing advanced MOSFET technology increases. This can lead to challenges in keeping up with Moore's Law, which states that the number of transistors on a chip doubles every 18-24 months [29].

The International Technology Roadmap for Semiconductors (ITRS) is a collaborative effort among semiconductor industry experts and researchers from around the world to identify the technology requirements and challenges facing the industry over the next 15 years [30,31]. The ITRS provides a roadmap for semiconductor technology development and serves as a guide for industry investment in research and development. The ITRS was initiated in 1998 and has been updated every two years until 2015. The roadmap includes projections for the scaling of CMOS (Complementary Metal-Oxide-Semiconductor) technology, as well as emerging technologies such as non-volatile memory, compound semiconductors, and advanced packaging techniques. To handle MOSFET scaling challenges, the ITRS has recommended several strategies that include:

- Alternative device architectures: Researchers have proposed various alternative device architectures that can address short-channel effects and enhance MOSFET performance. Examples include FinFETs, Gate All Around (GAA) devices, and Nanowire FETs.

- New materials: The ITRS has recommended the development of new materials that can replace traditional silicon and provide better MOSFET performance. Examples of new materials include III-V semiconductors, graphene, and carbon nanotubes.

- Advanced process technologies: The ITRS has recommended the use of advanced process technologies, such as extreme ultraviolet (EUV) lithography, to enable the production of smaller and more complex MOSFETs.

- Advanced packaging technologies: The ITRS has recommended the development of advanced packaging technologies that can help to reduce power consumption and enhance MOSFET performance. Examples include 3D chip stacking and wafer-level packaging.

- New device modeling and simulation tools: The ITRS has recommended the development of new device modeling and simulation tools that can accurately predict the performance of MOSFETs in advanced technology nodes.

- Collaboration between industry and academia: The ITRS has emphasized the need for collaboration between industry and academia to address the challenges of MOSFET scaling. Collaborative efforts can help to accelerate the development of new materials, devices, and process technologies.

The ITRS has played an important role in guiding the semiconductor industry over the past two decades and has helped to ensure that the industry continues to make rapid advancements in technology.

2.2   REDUCING SHORT CHANNEL EFFECTS

In the previous chapter, we can see that the lack of efficient electrostatic gate-to-channel coupling causes less gate control over the channel formation as the device structure reduces in size and SCEs start to appear. Hence, to counter the SCEs, we need to reinstate the gate with the dominant control of the channel formation. This can be done through the methods, but not limited to, discussed below in sub-sections 2.2.1 to 2.2.6.

2.2.1   Fully Depleted (FD) Silicon on Insulator (SOI)

Since FDSOI is a planar technology, therefore the process complexity is less in contrast to 3D technology. It also provides the advantages of reduced silicon structure, including power and speed, and by allowing substrate bias, it offers extra features. Figure 2.1 illustrates the FDSOI architecture. It is, as mentioned, a planar design on top of a buried oxide layer with a very fine layer of silicon (channel). Since the thin silicon channel layer is fully depleted, therefore it increases the gate control over the channel and eventually turns it off once the MOSFET is off. The source and drain regions are isolated from each other with the help of buried oxide that enhances the reduction of Drain Induced Barrier Lowering (DIBL) and reduces power dissipation by allowing

lower operating voltage. However, FD-SOI design offers significant benefits over the traditional bulk-Si designs. Owing to its improved electrostatics gate control, the key benefit is the trade-off between power and speed. Since it offers the opportunity to work at lower voltages to SRAM designers, has minimized instability due to spontaneous doping fluctuations and offers exceptional protection against Soft Error Rate (SER).
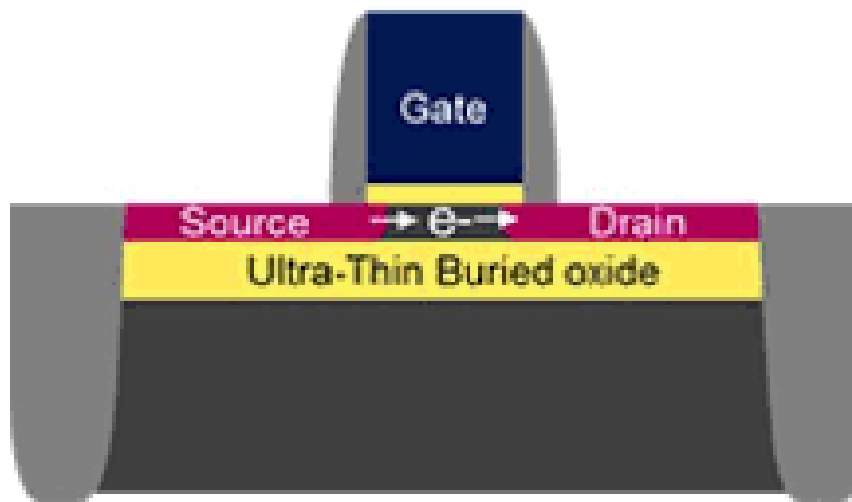
Figure 2.1: Fully depleted SOI

Due to its complete dielectric isolation, which removes any possibility of latch-up, along with a lack of silicon channel and compartment doping, that decreases noise coupling and enhances gain, FDSOI even provides advantages for RF and analog systems. However, the FD-SOI technology also has some drawbacks such as carrier mobility reduction due to the inefficient heat removal caused by the buried oxide beneath the thin Si body [27] and enhanced drain leakage currents due to impact ionization and band-to-band tunneling in FDSOI MOSFETs with slight spacer width variations and lateral doping profiles[28].

2.2.2 Reducing Gate Oxide Thickness (t_{ox})

The second method to overcome SCEs is to reduce the gate oxide thickness (t_{ox}) and thus enhancing the gate oxide capacitance (C_{ox}) which will enhance the gate-to-channel electrostatic coupling. A decrease in gate oxide thickness (t_{ox}) in proportion to gate length is required to control threshold voltage.It also helps to significantly increase drain saturation current and control the DIBL effect. However, if the gate oxide thickness is lowered below 2nm, then there are substantial challenges. There are circuit

vulnerabilities and significant power dissipation due to gate leakage current. Dopant penetration can still happen via gate oxide. To combat the negative effects of oxide thickness beyond 2 nm, thicker gate insulators which is having a high dielectric constant than the oxide are employed. This goes a long way in reducing the gate tunneling current through an insulator.

2.2.3   High-K Dielectric

Continued device size scaling requires the gate dielectric thickness to be continuously decreased. This necessity emerges from two separate factors: regulating the effect of the short channel and achieving a high drive current by sustaining the significant amount of charge induced in the channel as the power-supply voltage reduces. On the contrary side, the tunneling current increases exponentially through the gate dielectric as the gate dielectric physical thickness reduces. There is a significant impact of tunneling current on device standby power which bounds the pushing limit of gate dielectric physical thickness. Even among high-performance devices, tunneling currents resulting from silicon dioxides (SiO_2) smaller than 0.8 nm are usually not acceptable. By introducing new materials: high dielectric-constant gate dielectrics and metal gate electrodes, solutions need to be explored that can minimize the gate tunneling current and degradation of gate capacitance owing to polysilicon depletion. A gate dielectric having a significantly greater dielectric constant (k) than that of SiO_2 (k_{ox}) achieves a smaller comparable electrical thickness (t_{eq}) than SiO_2, however with a physical thickness (t_{phys}) greater than that of SiO_2 (t_{ox}): The specifications for a new oxide are mentioned below [29, 30]:

1. It must have enough high-K value for a sufficient number of scaling nodes to be used commercially.

2. It should be chemically stable with Si because due to its proximity with the Si channel.

3. It must serve as an insulator to reduce carrier intrusion into its bands by providing band offsets with Si of over 1eV.

4. It should be thermodynamically stable and suitable for processing at 1000 ^{0}C.

5. It has to establish an excellent electrical interface with Si.

It is not as easy as it might seem to substitute the SiO_2 with a new material which is having a different dielectric constant. The bulk and interface characteristics of the material must be identical to those of SiO_2 that is exceptionally strong. Some crucial examples include basic properties like chemically stability, thermal expansion and low diffusion coefficients that must match with silicon. Moreover, in SiO_2 and closely linked oxynitrides, interface traps of the order of $10^{10}cm^{-2}\ eV^{-1}$ and bulk traps of the order of $10^{10}cm^{-2}$ are very common [31, 32]. Gate dielectric stability and charge trapping are highly significant factors to consider.

2.2.4 Thermodynamic Stability

This necessity emerges from the situation that the oxide does not interact with Si to form SiO_2 or silicide. Since Equivalent Oxide Thickness (EOT) is increased by the SiO_2 layer and the impact of the new oxide is negated, although the silicides formed are metallic, the channel will be shortened. As noted by Hubbard and Schlom [33] and Schlom and Haeni [34], this requirement needs that new oxide has higher heat formation than SiO_2, which are observed in columns II, III and IV of the Periodic Table, which limits the option to very few oxides. Al_2O_3, Y_2O_3, BaO, SrO, CaO, ZrO_2, HfO_2, Al_2O_3 and lanthanides are those oxides. Several useful oxides like TiO_2, $SrTiO_3$, Ta_2O_5, $BaTiO_3$ and titanates are excluded. As oxides found in group II like SrO etc have very low K values, so they are less useful. Therefore, HfO_2, ZrO_2, Al_2O_3, La_2O_3, Sc_2O_3, Y_2O_3 and few lanthanides like Lu_2O_3, Gd_2O_3 and Pr_2O_3 are left with us.

Thermal stability concerning silicon is a significant factor because high-temperature anneals are typically used to trigger dopants in the polysilicon gate as well as the source/drain regions. Over the last decade, the interface between HfO_2 and the Si substrate has undergone tremendous scrutiny. Thermodynamically, HfO_2 is supposed to be compatible with Si contact, but the interface can be changed by kinetic effects, potentially leading to a compositionally-graded layer typically like a silicate [29]. Over the years, the structure of any such interface has created much confusion, with some suggesting that the interface is solely SiO_2 [35, 36, 37, 38] after HfO_2 deposition, while others indicate the existence of a considerable amount of Hf close to interface [39, 40, 41, 42] based on the thermal treatment and deposition details.

These materials have a dielectric constant typically ranges between 10 and 40, which is greater than SiO_2 by a factor of about 3 to 10. Compared to SiO_2 with the same electrical thickness, leakage current reduction from 10^3x to 10^6x is typically achieved experimentally in the case of high-K gate dielectrics [33]. Due to the existence of two-

dimensional electrical fringing fields from the drain via a physically thicker dielectric gate, the advantages of using a very strong dielectric-constant material to substitute SiO_2 for the same electrical thickness are restricted[34, 43].

The drain fringing effect reduces the source-to-channel potential barrier and similarly reduces the threshold voltage to the Drain Induced Barrier Lowering (DIBL) in which the drain region controls the source-to-channel potential barrier by connecting via the silicon substrate. Consequently, high-K materials used must be balanced with the simultaneous decrease of electrical thickness.

2.2.5   Band Offsets

The high-K oxide material is used as an insulator in MOS devices. To limit the conduction of charge carriers (electrons or holes) into the gate oxide bands through the schottky emission bands, the potential barrier at every band must be higher than 1 eV. SiO_2 has a wide bandgap of 9 eV, so for both electrons and holes, it has large barriers. Fortunately, for oxides with a lower bandgap such as $SrTiO_3$ (3.3 eV), their bands must be approximately symmetrically matched with Si for both barriers to reach 1 eV. Significantly, those are the only oxides that move through the thermal stability criterion. High formation heat correlates with a broad bandgap as the explanation behind it. On the other hand, $SrTiO_3$ has an appropriate offset of zero conduction band, so this oxide is unacceptable. Consequently, not only does the high-K material have a wide bandgap, but also a band orientation that leads to a significant barrier height. There are relatively low band offsets and smaller band gaps in most high-K materials that have other necessary properties. A particular material that has a similar bandgap and band alignment to SiO_2 is probably an Aluminium oxide Al_2O_3.

Although high-K dielectric is a feasible solution for reducing the problem of IGS, it is not compatible with the use of poly-silicon as the high-K material can easily react within the gate oxide with poly-silicon to form metal silicides. Electrical shortage between the gate electrode and the Si substrate can be caused due to it. Also, there is an interfacial reaction between the polysilicon and high-K material, which induces an interfacial layer under the high-K material [36, 44, 45] and the Equivalent Oxide Thickness (EOT) of high-K material will increase, decreasing the gate oxide capacitance. Hence, a high-K dielectric is always used with metal gate stacks such as TiN [46, 47, 48] and TaN [49]

2.2.6 Metal Gate

In CMOS, the gate electrode is intended to shift the fermi level EF of the channel surface to the other edge of the band to invert the transistor. A low-work gate function electrode (4.05 eV) will move the fermi level of the surface from the Si valence band to the conduction band, inverting the channel. Similarly, there is an n-doped Si channel for a PMOS device, and a gate with a 5.15 eV work function transfers its EF to its valence band, reversing the channel. This induces a shift of 1.1 eV in the work function, the Si bandgap. The work functions of metals are formulated by Michaelson. Earlier, the gate electrodes of the MOSFET are fabricated using polycrystalline Si either with heavily doped n-type or with p-type for NMOS and PMOS MOSFET respectively. This offers work functions of 4.05 and 5.15 eV respectively [50] Poly-Si has the advantage of being a refractory material, easy to deposit and compatible with SiO_2 and its related process flows. The doped poly-Si gate electrode has a small carrier density, so it incorporates a depletion length of 3Å. Real metals have degradation lengths of less than 0.5Å, so the use of these reduces ECT by 3-4Å.

The criteria for replacing the two metal gates with doped poly-Si is that they must be able to swing EF over the 1.1 eV work function range. The key aspect is that SiO_2 is essentially a perfect insulator so that the work function on the Si: SiO_2 interface is the same as the work function applied on the top of a thin SiO_2 sheet. For numerous reasons, this is not usually the case for metals on thin HfO_2.

2.3 HISTORY OF MULTI-GATE MOSFET

In the year 1984, T. Sekigawa and Y. Hayashi have reported the first paper on the Double Gate MOS (DGMOS) transistor [49]. This paper shows that a large reduction in short-channel effects can be accomplished by sandwiching a completely depleted SOI system between two attached gate electrodes. This design provides better control of the channel depletion region especially in contrast to the 'standard' SOI MOSFET and, in specific, reduces the impact of the drain electric field on the channel, thereby minimizing the short-channel effect.

2.3.1 Double Gate MOSFET

The concept of a Double Gate MOSFET (DGFET) is to get a small silicon channel width and gate contacts connected to both sides of the channel to manage the Si channel.

The double gate concept can be extracted from the fully depleted (FD) SOI structures. The ground plane function as a second gate if the buried oxide thickness is minimized to that of the gate dielectrics and if the ground plane is attached directly to the gate of the MOSFET. The double-gate structure consists of a conducting channel on either side, normally undoped, surrounded by gate electrodes. Switching both gates concurrently is the most popular method of operation. The second mode is to switch only the front gate and apply supply voltage to the back gate.

As compared to planar CMOS circuits, the double gate MOSFET greatly improves the efficiency of transistors even after the scaling of the device parameters. The channel connecting gate is doubled and SCE's are therefore easily eliminated. In DGFETs, very poorly doped or even undoped channels may be used. It offers excellent carrier mobility and therefore better intrinsic switching time even after the device is scaling down. Figure 2.2 shows the variation of DIBL and Subthreshold Slope with channel length.
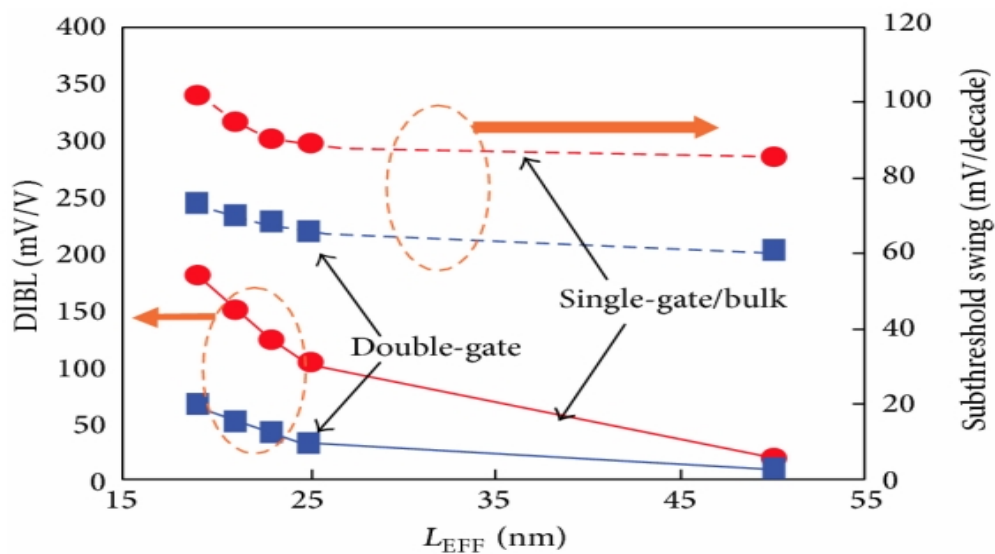
Figure 2.2: DIBL and Subthreshold Slope variations with channel length.

There is a decrease in sub-threshold leakage current or OFF state current. The current driving capacity of DGFETs is double that of planar CMOS, so it is possible to run DGFET at very smaller input and threshold voltages. This gives an ideal Sub-threshold Slope (SS) for suitable sub-threshold operation. DGFETs can therefore be operated at much lower voltages. The drain current rises to raise the gate voltage, so the contact resistance decreases, raising the cut-off frequency. Consequently, for the RF switch, where the control voltage should be lesser and then the drain current flow will

be lower, the rise in the number of gate-fingers will give rise to contact resistance[51]. So gate finger of the device can be increased to be used as an RF switch. Although the RF switch operating frequencies are in the GHz range, it is very convenient for wireless communication applications.

In electrostatic integrity, the challenge is significantly poorer than with double gate structures, specifically in the channel areas. A suitable self-alignment between the upper and lower gates is the key challenge in manufacturing such structures.

2.3.2 FinFET/Trigate Devices

In the past few years, FinFET/Trigate devices have been widely investigated. A variety of research papers that illustrate the enhanced short-channel actions of these devices over traditional bulk MOSFETs have been written[52, 53]. Hisamato et al. produced a double gate Silicon on Insulator device in 1989, which they named a fully depleted thin channel transistor (DELTA)[54]. It was the first recorded development of a FinFET-like structure. Over the past few years, because of the deteriorating short-channel behavior of planar MOSFETs, FinFETs have drawn extensive attention. If the MOSFET planar channel is horizontal, the vertical is the FinFET channel (often called fin). Figure 2.3 shows the structure of planar & FinFET MOSFET.
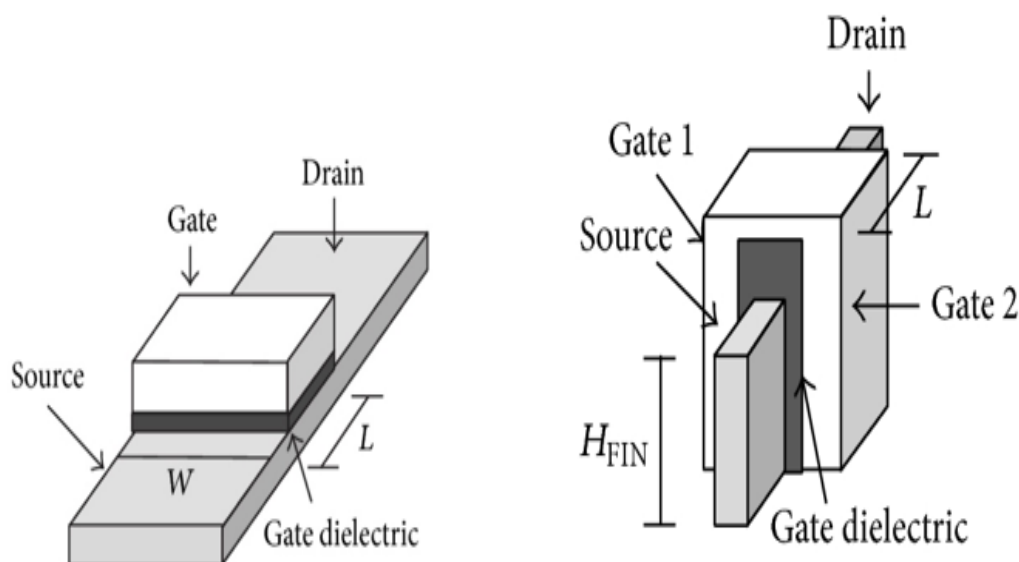
Figure 2.3: Conventional planar MOSFET and a FinFET.

The channel height, therefore, determines the width of the FinFET. This gives rise to a unique ability known as width quantization for FinFETs. This property states that using multiple fins, the FinFET width has to be numerous, that is, widths can be

enhanced. Arbitrarily defined FinFET widths are, therefore, not feasible. Even though smaller fin heights provide greater flexibility, they result in multiple fins, leading to a greater silicon area in turn. Taller fins, on the other side, give rise to less silicon footprint but may lead to structural instability as well. The fin height is generally estimated by process engineers and is kept below four times the thickness of the fin [55, 56]. Trigate FETs are modified version of FinFETs, linked to synonymously as FinFETs, with the third gate on top of the fin. A Trigate FET including a FinFET are shown in Figure 2.4.
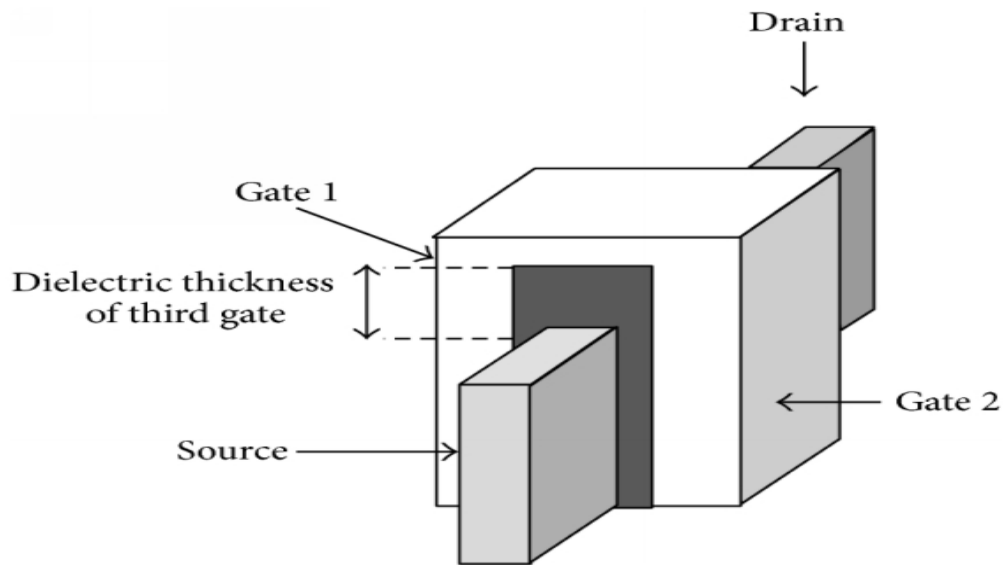
Figure 2.4: Tri-gate MOSFET

An additional precise etching process of the hard mask is included in Trigate FETs to generate the third gate on top of the channel. While this third gate introduces more complexity to the process, it also gives rise to some benefits, such as decreased fringe capacitances and extensive width of transistors [57]. In Trigate FETs, to generate the third gate, the thickness of the dielectric on top of the fin is decreased. The thickness of the fin also contributes to the channel width due to the existence of the third gate. Therefore, over FinFETs, Trigate FETs benefit from a small width advantage. Due to significant current conduction at the upper surface, Trigate FETs also have less gate-source capacitance particularly in comparison to FinFETs, but this benefit is reduced by higher parasitic resistance.

Comparing Trigate FETs and FinFETs, Yang and Fossum concluded that in the coming years, FinFETs are better than Trigate FETs. They demonstrated that while undoped Trigate FETs may have more relaxed body thickness, FinFETs in short channel

effects metrics is not comparable with them [58]. Trigate FETs end up losing the scaling benefit and suffering from a major layout area limitation when attempting to achieve corresponding SCE metrics. However, it is also early to announce a definite choice among FinFETs and Trigate FETs, similar to the bulk versus SOI controversy. As the channel length is scaled, it tends to flow leakage current and smaller devices cannot attain significant performance goals.

2.3.3 Gate All Around MOSFET

The FinFET's special design and the decreasing range of each gate pose challenges to the production process. The latest development of FinFET technology, Gate All Around (GAA) technology, has thus captured the attention of people. The GAA structure was first discovered by the Toshiba ULSI Research Laboratory in 1988. A Surrounding Gate Transistor (SGT) configuration with a gate surrounding the channel was suggested by Takato, clarified its advantages over the planar structure [59]. Due to the existence of two additional inversion channels (at the top and bottom of the silicon fin) and the existence of heavy density inversion region, the Gate All Around (GAA) MOSFETs in which the gate oxide and the gate electrodes wrap around the channel region demonstrate high transconductance and short-channel behavior [60].The ratio of fin width to gate length will increase in GAA MOSFETs.

The Gate All Around layout increases the electrostatic control and therefore the scalability of the gate length. It also allows the use of an undoped channel, which, leading to decreased random dopant variations, can decrease threshold voltage variance. Carrier mobility in Si nanowire MOSFETs is, however, not completely understood. The nanowire sidewalls are supposed to affect carrier transport because of the various crystal surface orientations. Sidewall roughness can also deteriorate the travel of the carrier due to improper lithography and etching processes. Even after the VLSI evolution methodology (bottom-up approach), and the sidewall spacer understanding, two types of Silicon Nanowires (SiNWs) are processed without requiring expensive lithographic tools (top-down approach). Typically there are two main approaches to synthesize nanowires: (a) bottom-up approach and (b) top-down approach. Each of these approaches has its pros and cons. The following two sections are dedicated to the discussion of both approaches.

2.4 BOTTOM-UP APPROACH

Several research groups have published many methods for realized nanowires using the bottom-up approach. These techniques are, in general, composed of: (a) Template-directed growth[61, 62, 63, 64, 65] , (b) Vapor-Liquid-Solid (VLS) synthesis [66, 67, 68, 69], (c) Vapor-Solid (VS) growth [70], (d) Laser-Ablation (LA) [71] and (e) Electrochemical Deposition(ED) [72]. Only VLS growth will be presented in the coming section since it is a well-studied technique for nanowire synthesis. Nanowires are grown on clean and defect-free semiconductor substrates or insulators such as sapphire or glass in the VLS growth technique. To significantly minimize contamination concerns, the process usually takes place in a vacuum chamber. The VLS process begins by depositing a metal catalyst layer (for example, Au) on the Si substrate. The substrate is then heated so that the temperature is higher than the eutectic point of the Au-Si system, which can be deferred from the binary phase diagram so that on the surface of the Si substrate, Au-Si liquid alloy droplets are formed.

The precursor gas containing Si atoms is then flown into the chamber and the Si atoms are dissolved in the droplets. The activation energy of normal vapor-solid growth is decreased by these droplets and they are thus energetically preferred sites for the incoming Si atoms. The alloy droplet adsorption of Si atoms continues even when a super-saturated state of Si in Au is achieved. After that, at the liquid alloy/solid Si interface, Si atoms will begin to precipitate from the Au-Si alloy. The Si nanowire increases in height with both the progression of adsorption and precipitation of Si atoms at the liquid / solid interface.

Metal catalyst plays an important role in VLS synthesis process. Even, before the success of the VLS synthesis process, the option to choose a metals catalyst must meet certain criteria. Firstly, to be grown at nanowire growth temperature it must be able to form a liquid solution with the solid crystalline material. Secondly, catalyzing agent solubility must be less in the solid phase than that in the liquid phase so that liquid alloy can easily form with less contamination. Thirdly, the catalyst's equilibrium vapor pressure over the liquid alloy must be less so that the droplet does not vaporize, shrink in volume (and thus radius) and decrease the growing nanowire radius before growth is finally terminated. Fourthly, the metal catalyst must be non-reacting so that no reaction products are formed during the growth process.

VLS synthesis process has the advantage of

   i. A simple method for the growth of nanostructured materials at a temperature just above the metal catalyst's melting point.

  ii. The nanowire size is defined by the size of the droplet of the alloy shaped on the starting substrate. The droplet size is measured by the initially deposited metal catalyst layer thickness[73].

 iii. It is possible to achieve atomically abrupt junctions by changing gas sources [74, 75].

Besides that, this VLS synthesis process in the bottom-up approach is free from photo-lithography and photo-masks. This would make it possible for the VLS process to be highly cost-effective and achieve a high economy of scale. The significant aspect raised by this approach is to explore a reliable way to incorporate synthesized nanowires into large-scale functional integrated circuits (ICs) successfully. In particular, the synthesized nanowires are scattered randomly over the substrate wafer because there is no control over the place where the alloy droplet is shaped and complex techniques are also needed to arrange the nanowires into precise device architectures to achieve a functional Integrated circuit. Several researchers have used other techniques like the evaporation of electron beams to grow nanowires. But these techniques have low throughput & lack of repeatability which are critical requirements in bulk production. Consequently, the nanowires produced by the bottom-up method have very few opportunities to be commercialized.

2.5   TOP-DOWN APPROACH

Currently, the top-down method is primarily used for fabrication in the semiconductor production unit, where metal oxide semiconductor field-effect transistor (MOSFET) characteristics are engraved on a silicon wafer using a photolithography technique[76]. Figure 2.5 shows the steps involved in photolithography process. The process is created on a projection printing process that is carried out in a device called a stepper, where the characteristics of the transistors are projected onto a silicon wafer via a photomask that has been repined using UV light with a photoresist material which is a light-sensitive material. It involves many techniques used by the semiconductor industry to convert a bulk wafer or crystal into nanostructures, such as photolithography, chemical etching,

and oxidation steps. Lithography, which is widely used in the semiconductor industry, is one of the most common top-down techniques for nanostructures. In general, to achieve nanowires, there are four steps involved in the top-down approach. First, this method involves the deposition of a resist material on a Si wafer, which works like a photographic film to create a pattern using a patterned mask after exposure and lastly developed. To achieve a smaller PR dimension, optional Reactive Ion Etch (RIE) trimming of the PR is carried out.
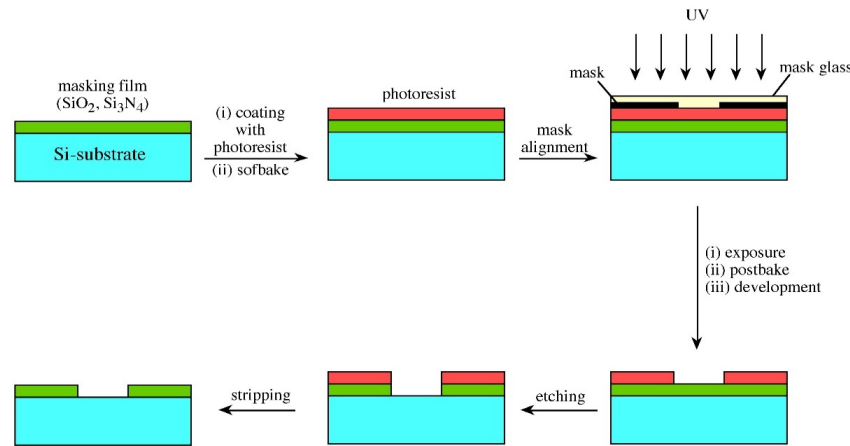
Figure 2.5: Photolithography process

The photoresist areas subjected to UV light become soluble to a specific forming solvent and are wiped away during the production process in the case of positive photoresist, creating a pattern of raised characteristics on the wafer close to the dark areas on the mask. On the other side, the areas of the photoresist exposed to UV light remain insoluble to a particular forming solvent in the case of negative photoresist, and during the design process, only the unexposed areas are wiped away, leaving a pattern of raised features on the wafer close to the clear regions on the mask.

Secondly, nanowires can then be developed from the wafer by etching the unnecessary material. Physical dry or wet etching of Si is performed to eliminate the unwanted Si regions using photoresist as the hard-mask, and a lateral Si fin or a vertical Si pillar is obtained depending on the initial mask layout. Third, to decrease the size of the vertical Si pillar or lateral fin, thermal oxidation is performed. Finally, the removal of the SiO_2 shell (from the previous step) by dipping the wafer into diluted hydro-fluoric (DHF) acid is accomplished to obtained vertical nanowires.

Figure 2.6 shows the positive and negative photoresists. Due to the ease, the Top-down fabrication technique is attractive in ordered to construct arrays of nanowires. This enables the electrical contact to nanowires so that they can integrate into large-
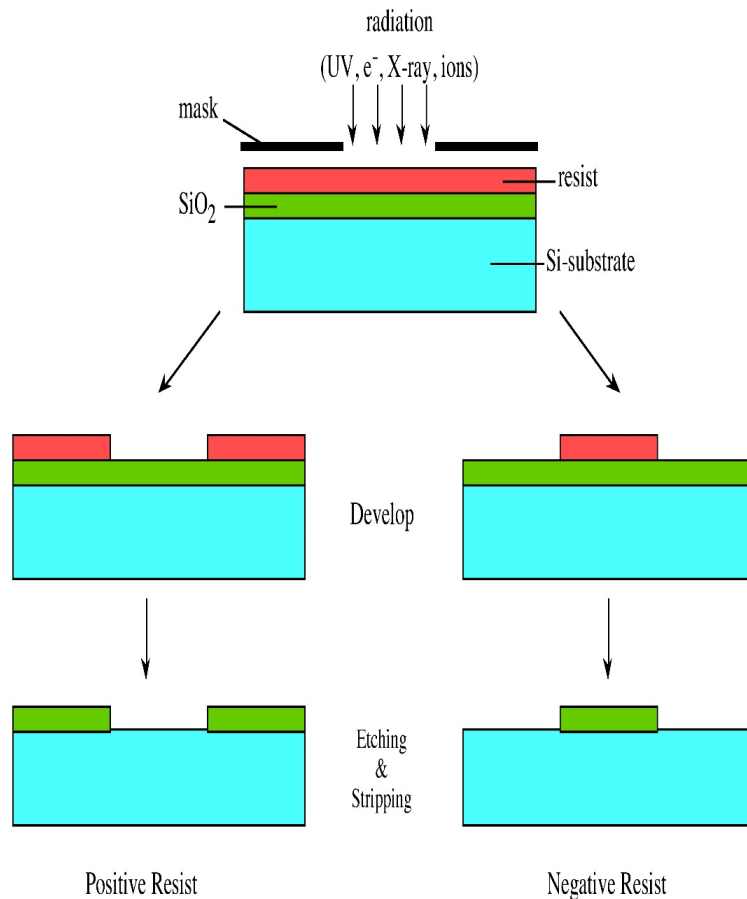
Figure 2.6: Positive and negative photoresists

scale devices. Furthermore, mostly these techniques follow standard industry processes, enabling their scale-up. There are some disadvantages of top-down fabrication. As the desired length scales down, the applicability of photolithography to these processes decreases, implementation of more advanced methods are required such as Extreme UltraViolet (EUV) lithography. Also, the photo-lithography involves high cost.

2.6 CONCLUSION

The background history and related short-channel effects (SCE) theories were explored, along with the options for the suppression of SCEs. To synthesize nanomaterials of the desired scale, shape and orientation, a variety of methods have been explored. These technical approaches can be categorized broadly as Bottom-up and Top-down approaches. Both methods play very important roles and have their own merits and demerits in the semiconductor industry.

CHAPTER 3

DEVICE FABRICATION AND TCAD SIMULATION

3.1 INTRODUCTION to ATLAS

The ATLAS device framework based on two and three-dimensional MOSFET simulation is a flexible and powerful framework. It predicts the electrical behavior of specified semiconductor structures and provides an understanding of the internal physical processes resulting from the operation of the chip. ATLAS offers a detailed collection of computational methods such as:

- DC, AC small –signal, and transient simulations

- Drift-diffusion transport models

- Energy balance and Hydrodynamic transport models

- Fermi-Dirac and Boltzman statistics

- Advanced mobility models

- Ohmic, Schottky, and insulating contacts

- Quantum transport models etc

The simulator for the Silicon device is included in the ATLAS package [77]. ATLAS simulates devices, which can either be virtually fabricated or analytically defined by Athena. The first approach allows the virtual fabrication of virtual IC chips/devices, including checking all the silicon processes and analyzing their effect on the operation of the device. The ATLAS source file contains device structure information collected by

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the process simulator i.e ATHENA. The Solution files stores 2D and 3D data solutions for different device variables using Tony Plot and the Log Files stores descriptions of electrical output data. ATLAS can be started as the default simulator (Deck build) or from an existing input file (deck build <input filename>) via Deck builder. It can be accessed from examples mentioned in the main control menu. These examples are described by type/application technology and device type. A user can select an example from Deck build examples and run accordingly.

A device can be virtually fabricated using commands by specifying a mesh and device materials/regions and then the deck build file can be simulated using ATLAS simulator [77]. Then the electrical characteristics can be extracted to estimate the parameters of the device. For physically-oriented two-dimensional (2D) and three-dimensional (3D) simulations of semiconductor devices, Atlas provides extensive functionality. It estimates the electrical characteristics of the semiconductor structures specified and gives insight into the internal quantum phenomena related to the operation of the chip. The various inputs and outputs of the ATLAS device simulator are shown in Figure 3.1. The inputs to the device simulator can be structure-based or command-based. One input can be a text file comprising commands to be executed by ATLAS and the other one can be a structure file that defines the simulated structure.
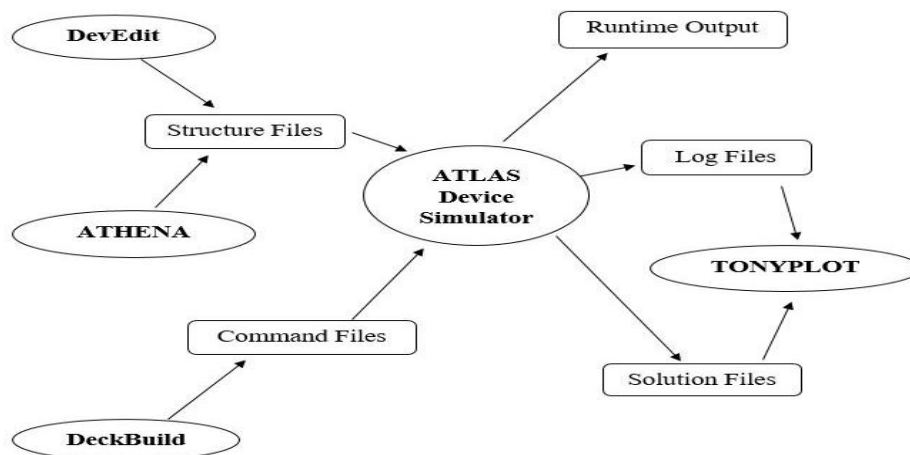
Figure 3.1: ATLAS device simulator

Three kinds of output files are created by the ATLAS device simulator. The first kind of output file is the run-time output, which provides you development and sends error notifications as the simulation goes on. A log file, containing all terminal voltages and solid modeling drain currents, is the second type of output file type. The third output file form is the solution file that offers 2D and 3D data linked to the values of the solution variables of the device. A significant characteristic of ATLAS and ATHENA is the

EXTRACT command, which permits the defined variables to be extracted depending on the simulation performed. The extraction results will be shown in the run-time output and stored in the file "results".

The GRAPH feature text fields can be used to plot these results in the Tony Plot. For estimation of the device parameters, the device can be simulated at a specific bias point and the solution files can be plotted. Material parameters such as the concentration of dopant and its ionization, working mechanism, and transport properties of the carrier (lifetime and mobility described by different physical models and parameters), etc. For any given physical structure, selected device parameters (or multiple parameters) can be simulated. For ATLAS calculations, mathematical methods used to obtain simulation results can be chosen and the results can be in the form of DC, AC small-signal, or transient characteristics.

The original solution (SOLVE INIT) assumes a zero bias situation and is monitored by two small voltage steps integrated into the initial guess that enhances convergence. Oxidation, Ion Implantation, Photolithography Annealing, Diffusion, Etching, and Deposition are processes used for device processing [78]. A particular model is defined to simulate a particular device available in the library of the software. The processing conditions, such as source/drain implantation and processes of annealing/oxidation needed for particular device structures and the oxidation process i.e LOCOS can be observed. The design flow of ATLAS is shown in Figure 3.2.
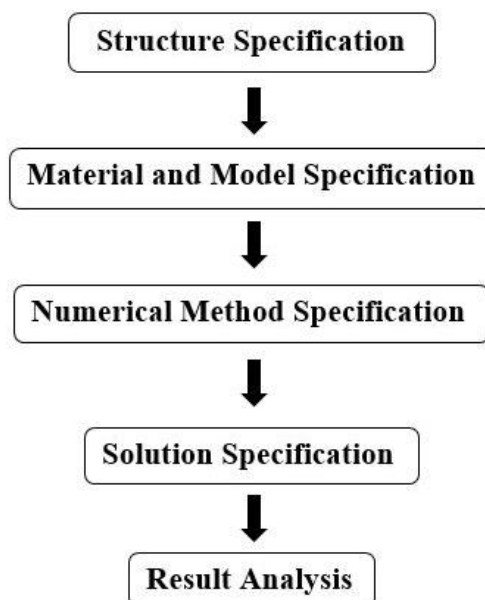

Figure 3.2: ATLAS design flow

3.2   DEVICE SIMULATION AND EXTRACTION

ATHENA and ATLAS are complicated and effective methods for simulation. Numerical models used in both Athena and Atlas simulators can be chosen from simplistic ones that only assume basic features to state-of-the-art representations that incorporate the latest developments in processing physics as well as computational physics. The programs use user-specified parameters to solve differential equations that explain different processor and system operations. The mesh (or grid), often user-defined, helps to regulate the accuracy of the 2D simulation, particularly for scaled devices that fit larger curvatures and thus need more densely spaced grid points.

To implement the different necessary steps for the Silicon device simulation, there are several sub-packages in SILVACO [93]. These are ATHENA Deck Build (for device design using commands), Dev Edit (for specifying the geometric features of the structure and mesh formatting), ATLAS (a device simulator tool used for simulation after written commands in ATHENA) and Tony Plot (used to visualize the waveforms). To simulate the device currents, the capacitance between different electrodes and transient signal analysis, these sub-packages are used. Also, to replicate the actual measurements on devices, several outside circuit elements such as resistor, inductor and capacitor may be attached to the electrodes of the device. In ATLAS, the setup is planned and simulated [79].

3.2.1   Potential Analysis

The electric potential between the surface of a particle and some point in the suspension is the surface potential [80]. Assuming uniform impurity concentration in the channel region and ignoring the effect of charge carriers on the electrostatics of the channel, the silicon thin- film potential distribution can be ascertained before the strong inversion.[81]

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}(\phi(r,y))\right) + \frac{\partial^2 \phi(r,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \quad \text{for} \quad 0 < r < \frac{t_{si}}{2}, 0 < y < L \quad (3.1)$$

where N_A, N_D are doping distributions, q is the electron charge, ε_{Si} is silicon dielectric constant, L is the length of the channel, r is the radius and t_{Si} is silicon thickness [82]. The analytical solution to find $\phi(r,y)$ uses a procedure that includes two-dimensional Poisson's equation into a one-dimensional equation using boundary

conditions [83]. The simple parabolic equation can be estimated the potential $\phi(r,y)$

$$\phi(r,y) = C_0(y) + C_1(y)r + C_2(y)r^2 \tag{3.2}$$

Where C_0, C_1 and C_2 are arbitrary constant and function of y only. Equation (3.1) can be explained by the below boundary conditions [84].

1. The potential at the source end i.e. at $y = 0$ is given by

$$\phi(0,0) = V_{bi} \tag{3.3}$$

2. The potential at the drain end i.e. at $y = L$ is given by

$$\phi(0,L) = \phi_s(L) = V_{bi} + V_{DS} \tag{3.4}$$

   Where V_{bi} is the built-in potential and given by

   $$V_{bi} = \frac{KT}{q} \ln\left(\frac{N_A N_D}{ni^2}\right)$$

   Where K is Boltzmann constant

3. The surface potential at the center of the device

$$\phi(r,y)|_{r=0} = \phi_c(y) \tag{3.5}$$

4. Electric flux at the silicon-oxide interface is given by

$$\begin{aligned}
\left.\frac{\partial \phi(r,y)}{\partial r}\right|_{r=\frac{t_{si}}{2}} &= \frac{C_{ox}}{\varepsilon_{Si}}\left[V_{GS} - V_{fb} - \phi_c(r,y)\right] \\
&= \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\left[V_{GS} - V_{fb} - \phi_c(r,y)\right]}{t_{ox}}
\end{aligned} \tag{3.6}$$

Where, ε_{ox} is dielectric constant, t_{ox} is the oxide thickness, V_{GS} is the gate to source voltage and V_{fb} is the flat band voltage.

$$V_{fb} = \phi_m - \phi_s \tag{3.7}$$

$$\phi_s = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + V_t \ln\left[\left(\frac{N_A}{n_i}\right)\bigg|_{y=0}\right]$$

$$V_{fb} = \phi_m - \frac{\chi_{Si}}{q} - \frac{E_g}{2q} - V_t \ln\left[\left(\frac{N_A}{n_i}\right)\bigg|_{y=0}\right]$$

Where, χ_{si} is electron affinity of Silicon, E_g is the energy band gap of Silicon, n_i is intrinsic carrier concentration and V_t is the thermal voltage [85, 86]. E_g is at 300k is

$$E_g = \left[1.16 - \left(\frac{7.02 \times 10^{-4}T^2}{1108 + T}\right)\right]$$

$$n_i = 3.1 \times 10^{16}T^{\frac{3}{2}}\exp\left(\frac{-E_g}{2KT}\right)$$

$$V_t = \frac{KT}{q}$$

Electric Flux at the center is given by

$$\frac{\partial \phi(r,y)}{\delta r}\bigg|_{r=0} = 0 \tag{3.8}$$

Therefore potential at any point y between source and drain is given by

$$\phi(0,y) = \phi_c(y) \tag{3.9}$$

The expression for the constants $C_0(y), C_1(y)$ and $C_2(y)$ can be obtained from the boundary conditions (3.3) - (3.9). Equation (3.2) at the center is given by

$$\phi(r,y)|_{r=0} = C_0(y) + C_1(y)0 + C_2(y)0$$
$$\phi(r,y)|_{r=0} = \phi(0,y) = C_0(y) \tag{3.10}$$

By comparing equation (3.9) and (3.10)

$$C_0(y) = \phi_c(y)$$

So equation (3.2) becomes

$$\phi(r,y) = \phi_c(y) + C_1(y)r + C_2(y)r^2 \tag{3.11}$$

Now differentiate equation (3.11) w.r.t r is given by

$$\frac{\partial \phi(r,y)}{\partial r} = 0 + C_1(y) + C_2(y)2r \tag{3.12}$$

$$\frac{\partial \phi(r,y)}{\partial r}\bigg|_{r=0} = C_1(y) \tag{3.13}$$

By comparing equation (3.8) and (3.13)

$$C_1(y) = 0 \tag{3.14}$$

Putting the above value of $C_1(y)$ in equation (3.2)

$$\phi(r,y) = C_0(y) + C_2(y)r^2 \tag{3.15}$$

Now again differentiate equation (3.15) w.r.t r is

$$\frac{\partial \phi(r,y)}{\partial r} = C_0(y) + C_2(y)2r \tag{3.16}$$

$$\frac{\partial \phi(r,y)}{\partial r}\bigg|_{r=\frac{t_{si}}{2}} = C_0(y) + C_2(y)2r \tag{3.17}$$

By comparing equation (3.6) and (3.17)

$$C_2(y) = \left(V_{GS} - V_{fb} - C_0(y)\right)\left(t_{Si}^2\left(1 + \frac{2\varepsilon_{Si}t_{ox}}{\varepsilon_{ox}t_{si}}\right)\right)^{-1} \tag{3.18}$$

Now potential at the center can be calculated by putting r = 0 in equation (3.1)

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}(\phi(r,y))\right)\bigg|_{r=0} + \frac{\partial^2 \phi(r,y)}{\partial y^2}\bigg|_{r=0} = \frac{qN_A}{\varepsilon_{Si}} \tag{3.19}$$

So solving equation (3.19) and above equation, we can find the center potential as given by

$$\phi_c(y) = P\exp\left(\sqrt{\frac{4}{\eta^2}}\right) + Q\exp\left(-\sqrt{\frac{4}{\eta^2}}\right) + \left(V_{GS} - V_{fb} - \frac{\eta qN_A}{4\varepsilon_{Si}}\right) \tag{3.20}$$

Where,

$$\eta = t_{si}^2 \left(1 + \frac{2\,\varepsilon_{si}\,t_{ox}}{\varepsilon_{ox}\,t_{si}} \right)$$

$$P = \left[\frac{\left(V_{bi} - \left(V_{GS} - V_{fb} - \frac{\eta q N_A}{4\varepsilon_{si}} \right) \right) \left(1 - \exp\left(-\sqrt{\frac{4}{\eta}}y \right) \right) + V_{DS}}{\exp\left(\sqrt{\frac{4}{\eta}}L \right) - \exp\left(-\sqrt{\frac{4}{\eta}}L \right)} \right]$$

$$Q = \left[\frac{\left(V_{bi} - \left(V_{GS} - V_{fb} - \frac{\eta q N_A}{4\varepsilon_{si}} \right) \right) \left(1 - \exp\left(\sqrt{\frac{4}{\eta}}y \right) \right) + V_{DS}}{\exp\left(\sqrt{\frac{4}{\eta}}L \right) - \exp\left(-\sqrt{\frac{4}{\eta}}L \right)} \right]$$

The potential distribution is visualized as a contour map or a three-dimensional plot, representing the varying potential values across different locations within the device. It provides insights into the electric field strength, voltage gradients, and potential barriers or wells that affect the behavior of charges and current flow.The potential distribution is shown in Figure 3.3
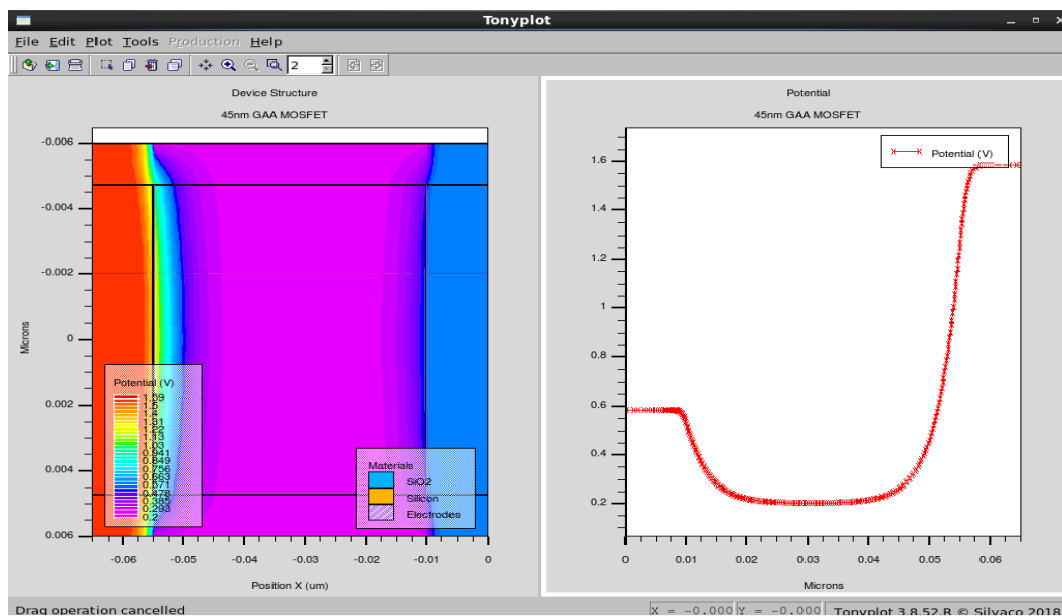

Figure 3.3: Potential distribution graph

3.2.2   Donor Concentration

Doped semiconductors are semiconductors containing impurities that are introduced into the crystal structure of the semiconductor by global atoms. Due to lack of control during semiconductor development, these impurities can either be accidental or they can be inserted to produce free charge carriers in the semiconductor. The creation of free charge carriers, insufficient amounts of impurities, allows the impurities to provide electrons to the conduction band, so in that situation, they are termed as donors, or to provide holes to the valence band, in which case they are termed as acceptors (since they efficiently acquire an electron from the filled valence band). Free carriers will thus be produced by a semiconductor doped with ionized impurities (i.e the impurity atoms have either added or adopted an electron). Shallow impurities - usually around thermal energy or less - are impurities that require less energy to ionize. Deep impurities require energy ionization greater than thermal energy so that only a portion of the semiconductor impurities lead to free carriers.

It is quite unlikely that deep impurities away from either band edge are five times the ionized thermal energy. Ionization of energies greater than thermal energy is required for deep impurities, such that a small portion of the impurities in the semiconductor contribute to the free carriers. In the simulation, the uniform donor (N_D) doping profile plot between source and drain of fixed charges 1×10^{20} cm^{-3} is used to prevent abrupt junction in Figure 3.4. The work-function $\phi_m = 3.4$ eV of the metal gate work is considered.
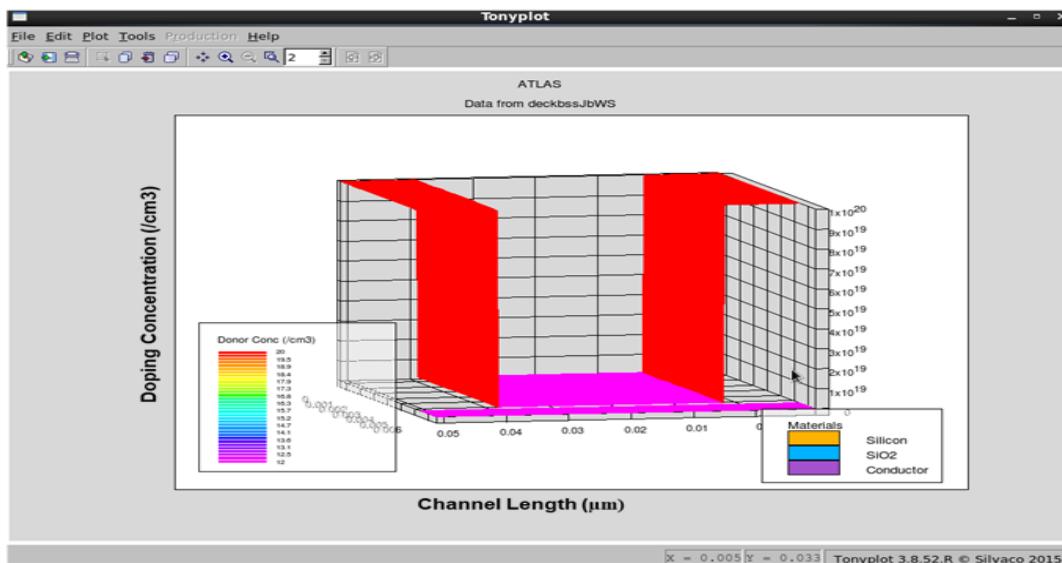

Figure 3.4: Donor concentration plot

3.2.3 Electric Field

Electric field, an electric characteristic correlated with each space point when some form of charge exists. The magnitude and direction of the electric field are denoted by symbol E, called the strength of the electric field [87]. Electronic devices subjected to ionizing radiation show deterioration because of their electrical properties, which can impair the functionality of the device [88]. It is of great importance to establish techniques for testing and improving equipment to understand the physical phenomena accountable for radiation exposure that may be unique to a specific technology. The goal of this work is to verify the impact of thermal annealing processes and electrical fields applied in total ionizing dose experiments during the irradiation of Metal Oxide Semiconductor Field Effect Transistors(MOSFET) by evaluating the changes in electrical parameters of these devices. The electric field graph is shown in Figure 3.5.
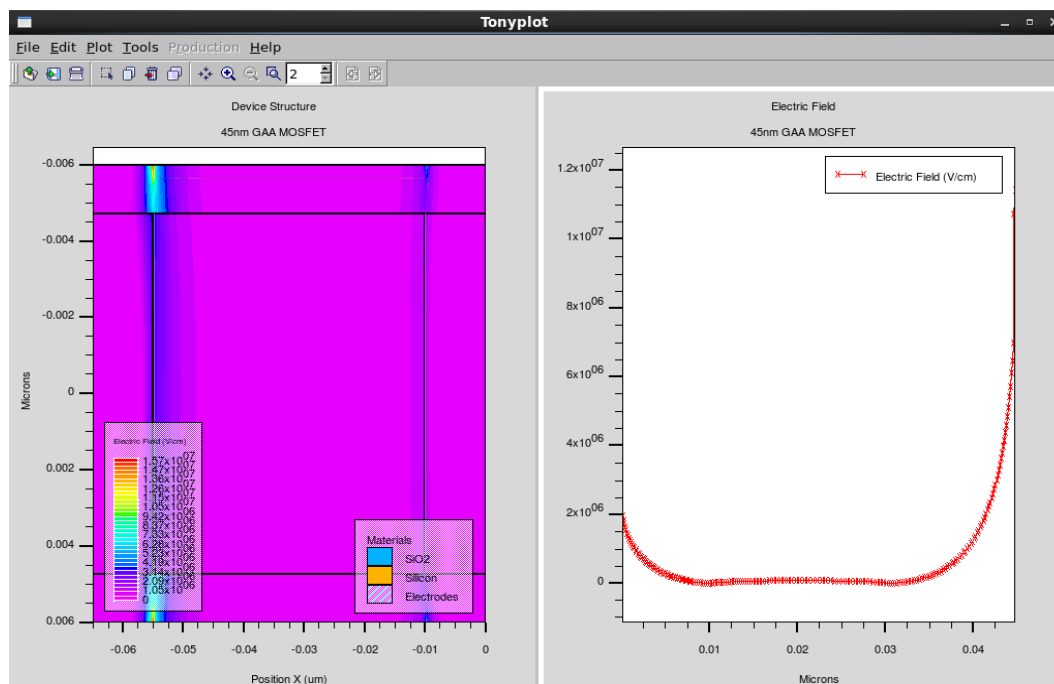
Figure 3.5: Electric field plot

3.2.4 Electron Current Density

It is a physical quantity that describes the flow of electrons in a given material or system. It is defined as the amount of electric charge per unit time per unit area carried by the electrons in a material. Furthermore, in terms of the external field and Fermi capacity, current density has an oscillatory behavior [89]. The charge density mainly comes from intentional dopants at room temperature and due to which either electron (from donors) or holes (from acceptors) will generate. Electrons and holes are thermally produced in

pairs at higher temperatures. This increases electrical conductivity greatly since both forms of carrier hold current. The current electron density is shown in Figure 3.6.

Figure 3.6: Electron current density plot

3.2.5   Energy Band Diagram

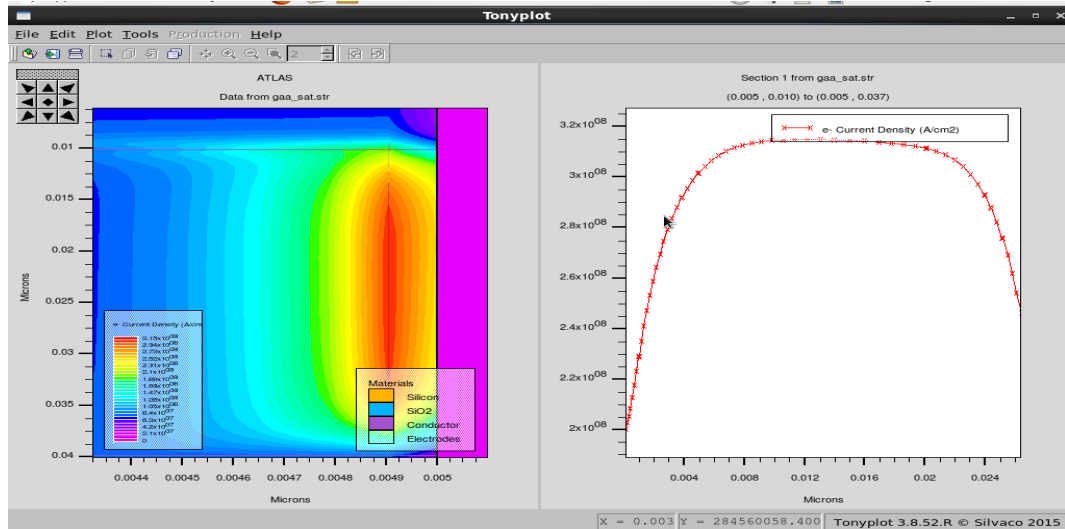The free metal electron model gives us a clear insight into the electrical conductivity and electrodynamics of the metal. But with other issues, such as the relationship of conduction electrons in the metal to the valence electrons of free particles and several transport properties, the model does not support it. Each solid includes electrons. How electrons react to an applied electric field is an important question for electrical conductivity. The electrons are grouped in crystals in energy bands divided by energy regions for which there are no wavelike electron orbits. These prohibited regions are known as energy gaps or band gaps (E_G), where the variations between a metal, a semiconductor and an insulator are schematically summarized. If the permitted energy bands are all either occupied or vacant, the crystal acts as an insulator, and then no electrons will move in an electric field. If one or more bands are partially filled, the crystal conducts like a metal. When one or two bands are partially occupied or marginally clear, the crystal is a semiconductor or semimetal.

The foundations of electronic devices are semiconductor materials. Semiconductors are made of various kinds of transistors, diodes and solar cells. Silicon is the most common semiconductor material [90]. Atoms in a silicon crystal have four valence electrons to associate with four neighbors closest to them. Only certain distinct energy levels may occupy the electrons of a separated atom. If two atoms travel closer to each

other in a semiconductor then the split energy levels fit all the electrons in the structure.

The bending of the energy bands, required for aligning the Fermi, E_F, gate and semiconductor levels, is preferably calculated at zero applied bias by the difference in the work functions of the metal and the semiconductor. Band bending means a change in electric potential in the presence of an electric field. Charges trapped by oxide and interface may also lead to a large amount of band bending [91]. With the applied bias, band bending changes and when the flat band voltage is applied to compensate for the disparity in work functions, the bands become flat. Inside the semiconductor, the Fermi level stays unchanged, independent of biasing constraints as well as due to the very high resistance of the dielectric layer, there is no net current flow perpendicular to the interface of the device [92]. Owing to the abundance of free carriers, very little band bending occurs in the metal. The energy band diagram is shown in Figure 3.7

Figure 3.7: Energy Band diagram

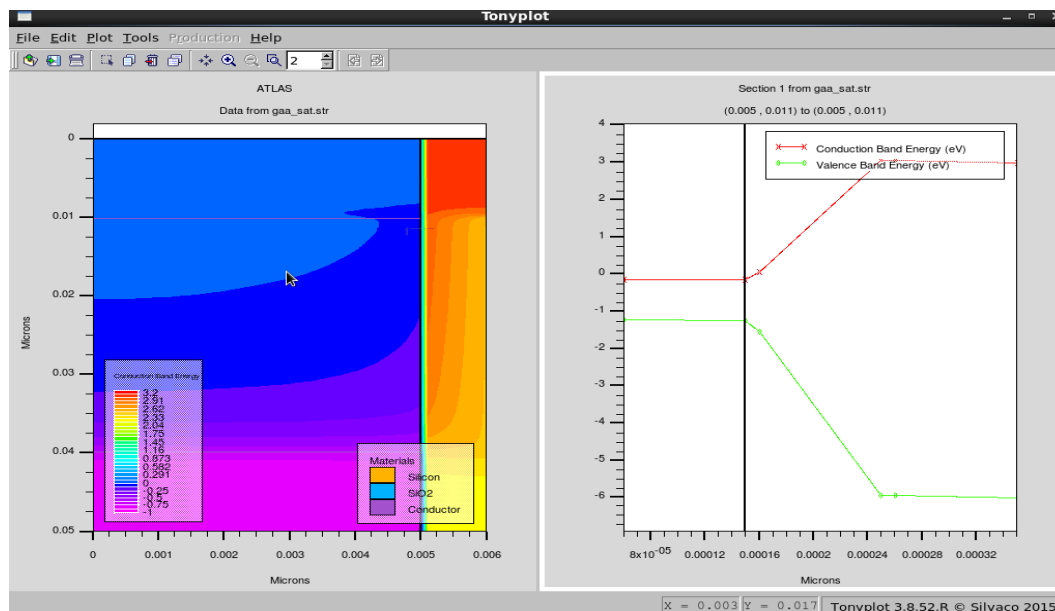## 3.3   CONCLUSION

The overview of SILVACO TCAD tools-ATHENA & ATLAS used for the design, virtual fabrication and modeling of a silicon MOSFET is given in this chapter. Here, the mathematical expression of surface potential is also derived. After simulating the device, various parameters such as electron current density, conduction band, valence band profiles and donor concentration are obtained.

CHAPTER 4

ELECTRICAL CHARACTERISTICS OF GATE ALL AROUND MOSFET

4.1 INTRODUCTION

A tremendous boost was provided to various studies on Silicon On Insulator (SOI) due to its acceptance for the fabrication of electronics appliances [93]. Initially, SOI architectures suggested by researchers were invasive and inefficient, but then achievements in the semiconductor industry have given this technique, the recognition and reward deserved by it [94]. The sizes of standard transistors need to be reduced to the sub-nanometre region to obtain low price, high operating speed and better results [95]. Downscaling of the conventional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) device resulted in an imminent power crisis, particularly static power consumption. Because of device downscaling, the drain and source regions become so adjacent to each other due to which MOSFET degrade the gate control over channel and short channel effects arise [96].

Therefore new technologies are explored to handle heat dissipation, leakage current and cost-related problems. Among various proposed SOI devices, Multi-Gate Field-Effect Transistor certainly comes out to solve the above issues [97]. To improve the energy-efficiency of electronic circuits, small sub-threshold swing switches are the best option to replace the existing MOSFETs [98]. However, Gate All Around MOSFET is one of the innovative devices that further allow scaling without affecting the efficiency of the device [25]. Gate All Around (GAA) MOSFET has great electrostatic channel control, better scaling alternative and optimal sub-threshold swing as compared to other devices. The structure of source/drain regions of GAA MOSFETs is different due to

cross-sectional dimensions and shapes. Therefore numerous establishments created their GAA MOSFET with their procedures [99]. It is therefore very essential to discover guidelines for cross-sectional shape design and sizes that are appropriate for cylindrical GAA MOSFET. In this chapter, the virtual fabrication of 45nm cylinder-shaped GAA MOSFET has been performed and then the device is simulated using ATLAS device simulator to extract its electrical characteristics of the device.

4.2 GAA STRUCTURE AND DEVICE PARAMETERS

The structure of a Gate-All-Around (GAA) MOSFET is characterized by having the gate electrode completely surrounding the channel region. The GAA MOSFET is typically built on a semiconductor substrate, such as a silicon wafer. The substrate provides mechanical support and serves as a foundation for the fabrication of the various layers and components of the MOSFET. Figure 4.1 depicts the simulated Cylindrical Gate All Around (CGAA) MOSFET structure in the ATLAS simulator.The device is designed and simulated using the ATLAS SILVACO tool. The radial guidelines are supposed to be along the radius and lateral direction along the z-axis of the cylinder [100, 101].
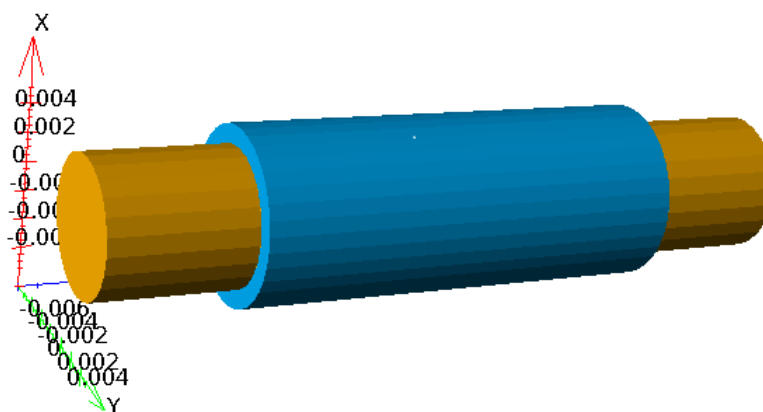
Figure 4.1: Schematic structure of the Cylindrical Gate All Around (CGAA) MOSFET

The Length of the Gate (L_g) is 45nm and a radius of 5nm. The gate oxide thickness (t_{ox}) is 1nm. The specifications are taken according to the ITRS standards [102]. The source/drain (S/D) extension doping profile is taken as gaussian with a peak concentration of 1.0×10^{20} cm^{-3}. The details of the physical parameters of the device used in the structure are shown in Table 4.1.

Table 4.1: Device dimensions for channel length of 45nm

Parameter	Value
Gate Length L_g	$45nm$
Radius $t_{Si/2}$	$5nm$
Oxide Thickness t_{ox}	$1nm$
Channel Doping	1.0×10^{18} cm^{-3}
Source Doping N_D	1.0×10^{20} cm^{-3}
Drain Doping N_D	1.0×10^{20} cm^{-3}

Various parameters i.e Threshold voltage (V_{th}), ON current (I_{on}), OFF current (I_{off}), ON/OFF current (I_{on}/I_{off}) ratio, DIBL (Drain Induced Barrier Lowering) and Sub-threshold swing (SS) of 45nm GAA MOSFET have been extracted. The cut plane view of GAA MOSFET is shown in Figure 4.2
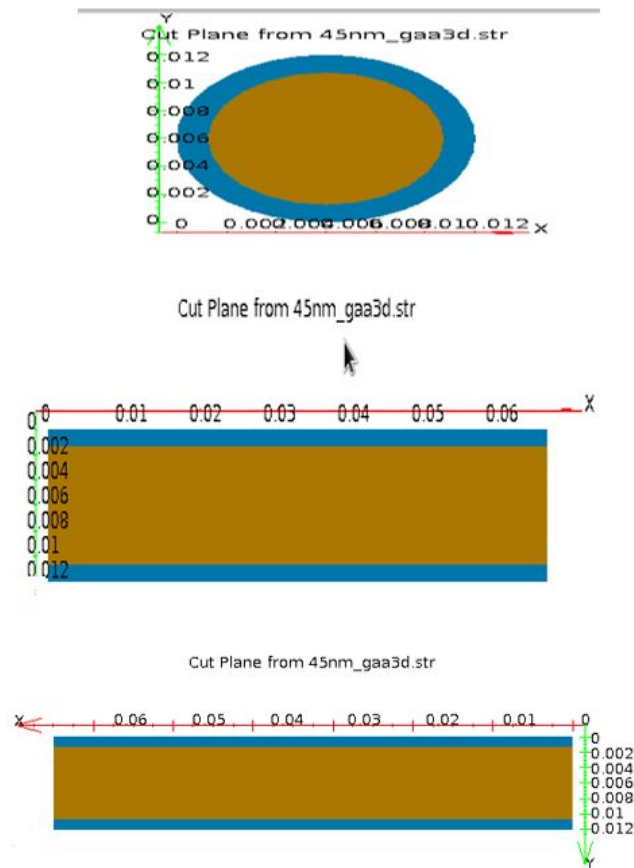
Figure 4.2: Cut plane view of the simulated device

4.3   RESULTS AND DISCUSSION

To investigate the electrical characteristics of the device and validate the proposed analytical model, the device was simulated in 3-D. [103]

4.3.1   Transfer Characteristics

Figure 4.3 depicts the transfer characteristics of 45nm GAA MOSFET in the linear scale. Transfer characteristics relate drain current response to the input voltage at the gate terminal [77]. These characteristics are obtained at fixed drain voltages of 0.1V and 1V. Gate voltage varies from 0 to 1V for fixed drain voltage V_d. A graph is plotted between drain current along with the y-axis and gate voltage along the x-axis at small drain-source voltage $V_{DS} = 0.1V$. Similarly, Saturation region curve is also plotted at drain-source voltage $V_{DS} = 1V$.
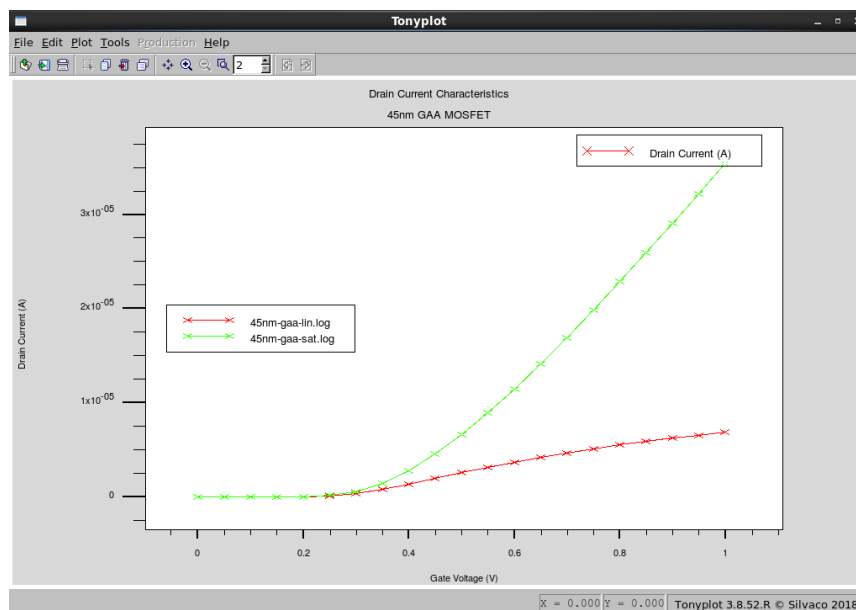
Figure 4.3: Drain current characteristics in linear mode

A drain current versus gate voltage plot in logarithmic scale is often used to illustrate the behavior of a transistor, typically a MOSFET, over a wide range of gate voltages. The logarithmic scale allows for a better representation of the wide dynamic range of drain current values typically observed in the plot. Figure 4.4 shows the transfer characteristics where drain current is plotted along the y-axis in the logarithm scale.

Figure 4.4: Drain current characteristics in logarithmic mode

Various device parameters like ON current, Threshold voltage, OFF current, Sub-threshold swing and DIBL, etc. are extracted in the ATLAS device simulator.The values of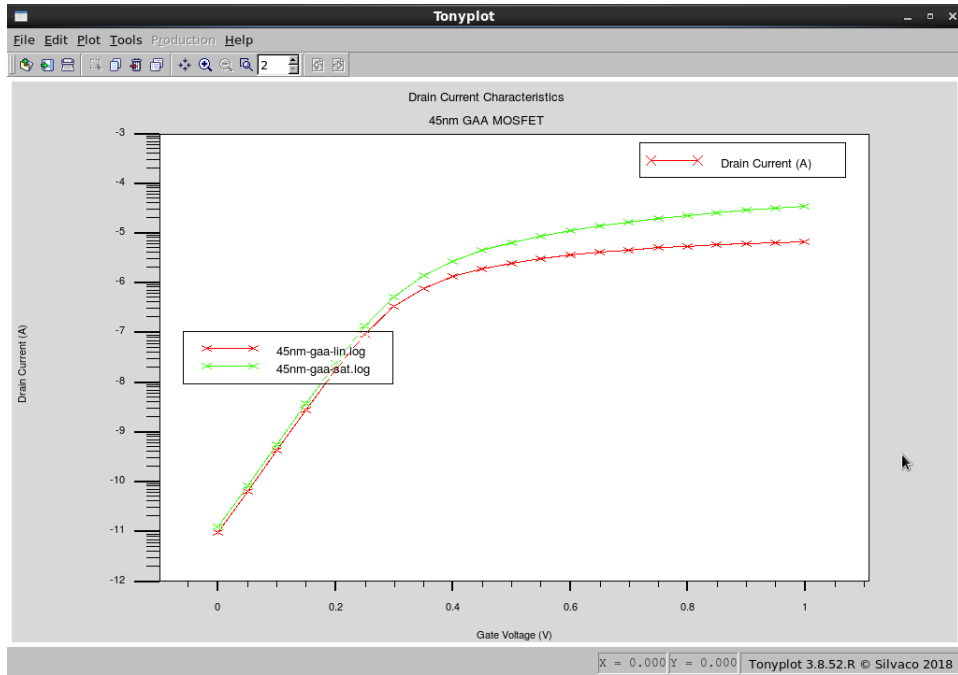 driving current, I_{on} and leakage current, I_{off} are estimated for different values of gate voltage. Driving current, I_{on} has been obtained at drain voltage $V_D = 1V$ and leakage current, I_{off} has been obtained at drain voltage $V_D = 0.1V$.

4.3.2 Trans-conductance

Trans-conductance (gm) is a significant parameter to estimate the performance of MOSFET. It is characterized as the ratio of drain current change to gate voltage change over an arbitrary small interval on drain current versus gate voltage curve [104]. Figure 4.5 shows the trans-conductance versus gate voltage plot. In the plot, the transconductance (gm) is typically represented on the vertical axis, while the gate voltage (V_G) is shown on the horizontal axis. It is often used to analyze and optimize circuit designs, determine the operating region of the device, and assess its linearity and sensitivity to input voltage changes.
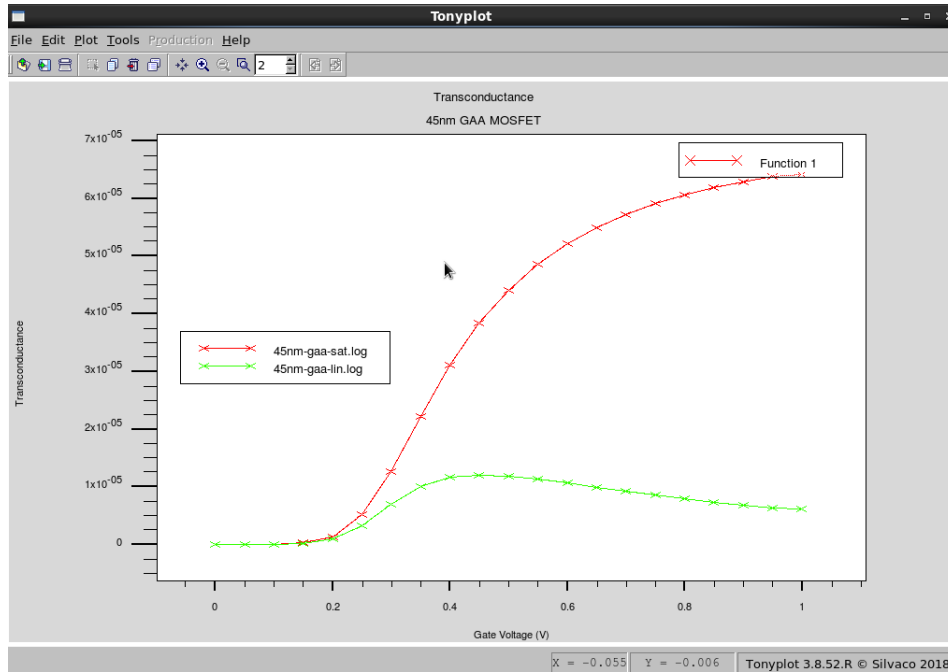
Figure 4.5: Trans-conductance versus gate voltage plot

Table 4.2 displays the various extracted parameter values. ON/OFF current ratio (I_{on}/I_{off}) is determined by extracting minimum and maximum current from drain current versus gate voltage plot. Considering the small-scale geometry device, the calculated value of I_{on}/I_{off} equals $2.8e+06$ is tremendous. Similarly, the Subthreshold Slope (SS) and DIBL have been extracted and calculated values are 60.47 mV/dec and 16.8 mV/V respectively.

Table 4.2: Extracted value of 45nm GAA MOSFET

Parameter	Values
V_{tsat}	0.24 V
I_{on}	$4.38e-05$ A
I_{off}	$2.03e-10$ A
I_{on}/I_{off}	$2.80e+06$
V_{tlin}	0.25 V
SS	60.47 mV/dec
DIBL	16.8 mV/V

4.3.3   Comparison of Simulated Results with the Literature

A Gate All Around MOSFET has been simulated in an ATLAS simulator and its results are compared with the existing work done in literature. Various parameters have been extracted i.e. Drain current (I_{on}), Sub-threshold current (I_{off}), DIBL, Sub-threshold Slope (SS), I_{on}/I_{off} ratio after the simulation of the device in ATLAS. The simulated sub-threshold characteristics are compared with et al M. Karbalaei [105] as shown in Figure 4.6 .
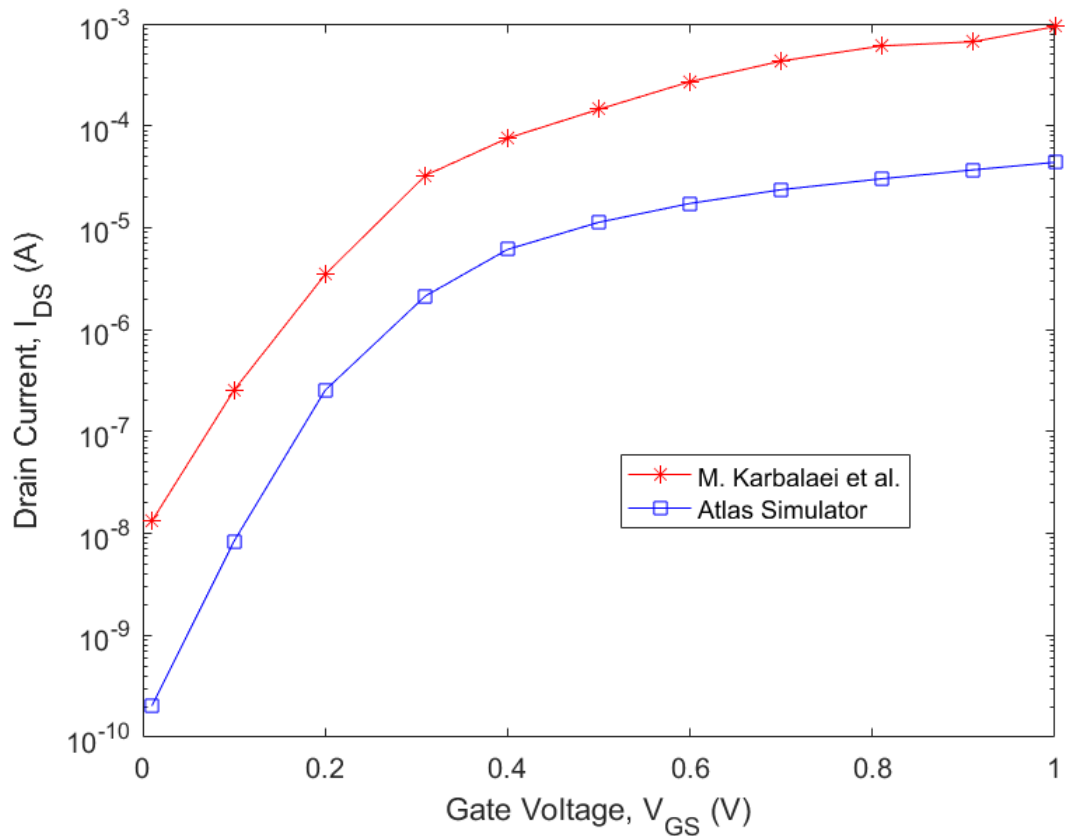
Figure 4.6: Sub-threshold current characteristics and its calibration with literature

It is shown that the proposed device has better sub-threshold characteristics as compared to its counterpart [106]. It has been noted that the OFF current of the reference device is 1.32e-08 A and the simulated device is 2.03e-10 A, which is better than the reference device as shown in Figure 4.6 also. The drain current transfer characteristics of GAA MOSFET have been shown in Figure 4.7(a) at $V_{DS} = 1$ V. The Gate work-function (ϕ_f) is taken at 4.45 eV. It has been noted that the ON current of the reference device is 9.40e-04 A and the simulated device is 4.38e-05 A, which is comparable with the reference device as shown in Figure 4.7(b).
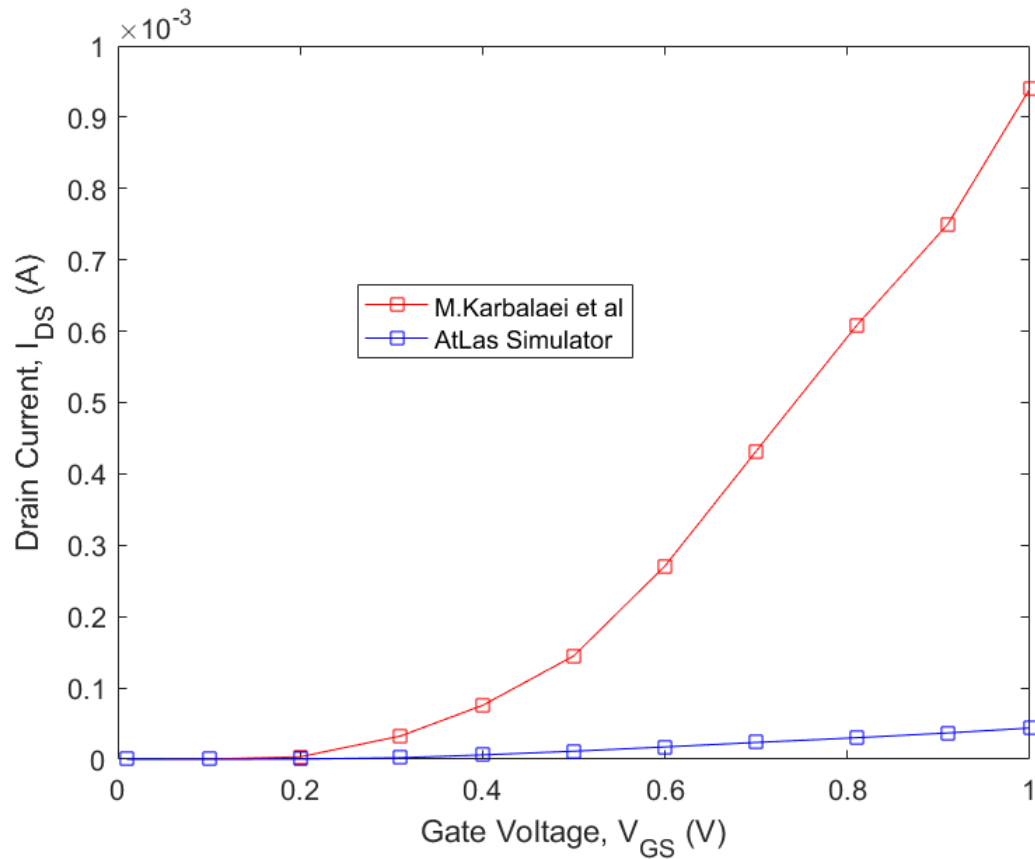
(a) Drain current characteristics
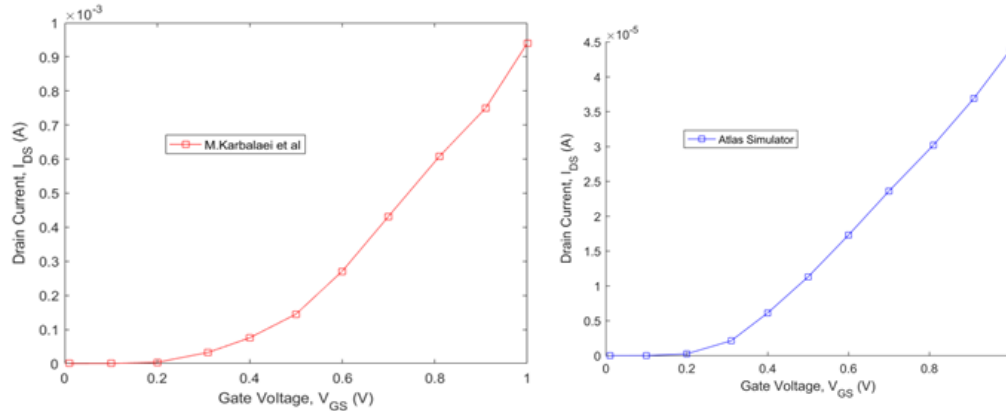
(b) Drain current characteristics and its calibration with Literature

Figure 4.7: Drain current characteristics comparison

After the calculation of I_{on} and I_{off} current, the I_{on}/I_{off} ratio has been calculated and compared with the reference device. It has been noted that the simulated device is showing better results as compared to the reference device in the terms of I_{on}/I_{off} ratio as shown in Figure 4.8.
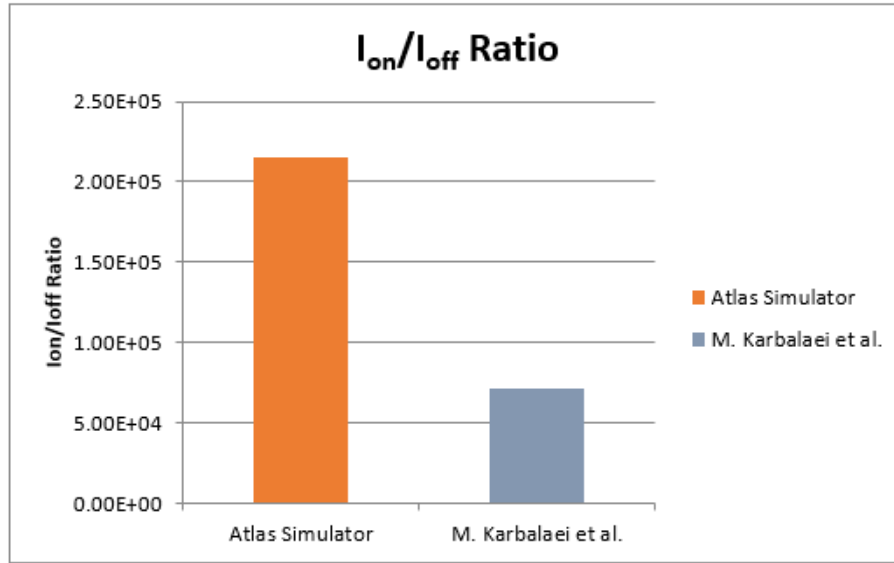
Figure 4.8: I_{on}/I_{off} ratio characteristics and its calibration with literature

4.3.4 Comparison of Simulated Results with the Analytical Results

The oxide capacitance can be calculated from the derived formula given in equation (4.1)

$$C_{ox} = \frac{\varepsilon_{ox}}{R \ln\left[1 + \frac{t_{ox}}{R}\right]} \tag{4.1}$$

Where ε_{ox} = 4.97 $\times$ 8.85e-14 F/cm, t_{ox} = 1 nm, R = 5 nm. After calculating the values of oxide capacitance, drain saturation voltage can be calculated from the derived formula given in equation (4.2)

$$V_{Dsat} = \frac{V_{GS} - V_{th}}{1 + \frac{(V_{GS} - V_{th})}{L * E_{eff}}} \tag{4.2}$$

In the saturation region, an expression for the drain current is given as

$$I_{dsat} = 2\pi R V_{sat}\, Q_{insat} \tag{4.3}$$

where Id_{sat} is the saturation drain current and *Qinsat* inversion charge at $V_{DS} = V_{Dsat}$ and given as

$$Q_{insat} = C_{ox}\left(V_{GS} - V_{th} - V_{Dsat}\right) \tag{4.4}$$

Using Eq. (4.4) in Eq. (4.3) drain current at saturation region become

$$I_{dsat} = 2\pi RC_{ox}V_{sat}(V_{GS} - V_{th} - V_{Dsat}) \tag{4.5}$$

By substituting the values of calculated $V_{Dsat}, V_{sat} = 10^7 cm/s, C_{ox}$ (calculated in equation (4.2)), $R = 5nm, V_{GS} = 1$ V, $V_{th} = 0.16$ V, the drain current is calculated as 1.3e-05 A which is comparable to the simulated value. The comparison graph of simulated and analytical values is shown in Figure 4.9.
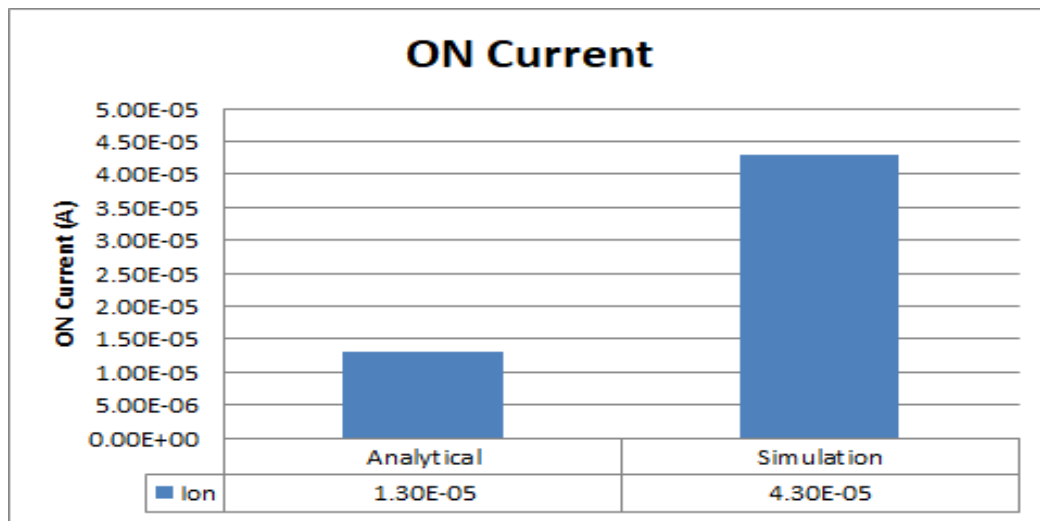

Figure 4.9: Comparison curves of I_{on} current

The Trans-conductance is analytically calculated and compared with the simulation results as shown in Figure 4.10.
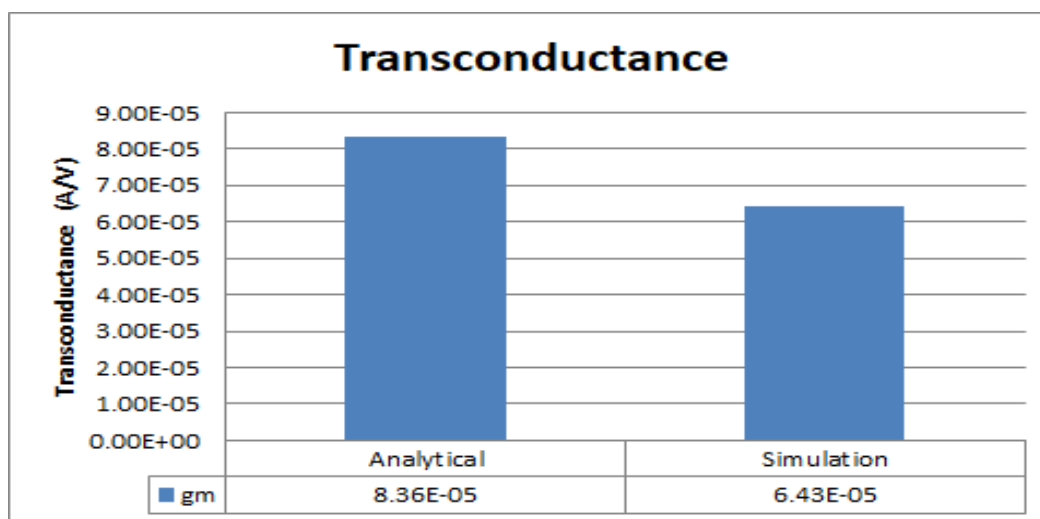
Figure 4.10: Trans-conductance comparison with analytical & extracted value

4.4   GATE ALL AROUND STRUCTURE WITH VARIATION IN CHANNEL LENGTH

The schematic structure of the 30nm cylindrical GAA (CGAA) MOSFET after the simulation is shown in Figure 4.11. This structure is designed using the ATLAS
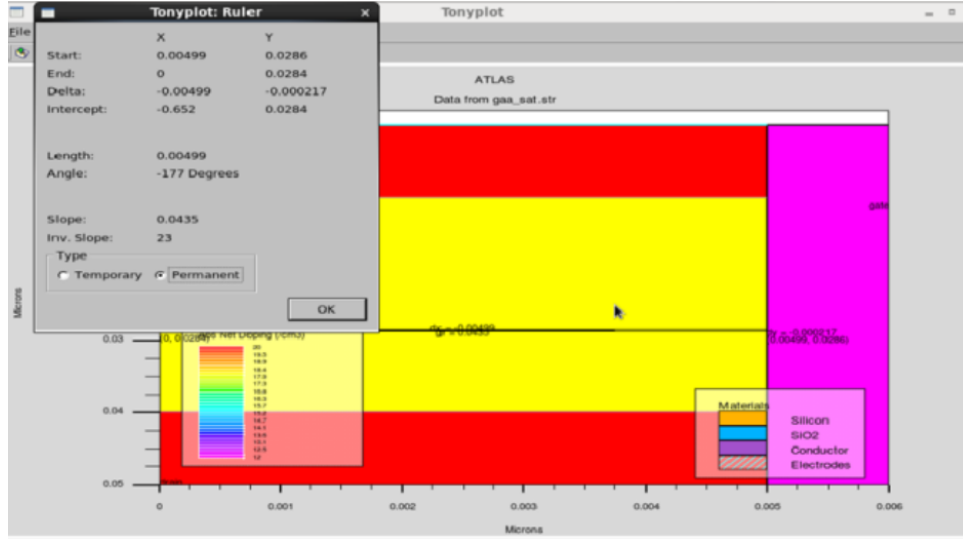
Figure 4.11: GAA structure with channel length=30nm

SILVACO tool. The radial parameters are assumed to be along the radius and lateral direction along the z-axis of the cylinder. Figure 4.11 illustrates the cross-sectional view of GAA structure for silicon thickness of radius 5nm and gate oxide thickness of 1nm has been taken in the simulation. The physical parameters of the device used in the structure are shown in Table 4.3.

Table 4.3: Device dimensions for channel length of 30nm

Parameter	Value
Gate Length L_g	30 nm
Radius $t_{si/2}$	5 nm
Oxide Thickness t_{ox}	1 nm
Channel Doping	1.0×10^{18} cm^{-3}
Source Doping N_D	1.0×10^{20} cm^{-3}
Drain Doping N_D	1.0×10^{20} cm^{-3}

The Gate length (L_g) is 30 nm with a work function of 4.45 eV, the diameter is 10 nm and gate oxide equals 1 nm. The source/drain (S/D) extension doping profile is taken as gaussian with a peak concentration of 1.0×10^{20} cm^{-3}.

4.4.1 Transfer Characteristics

Figure 4.12 shows the transfer characteristics of 30nm GAA MOSFET. The simulation is done with two different drain voltages.
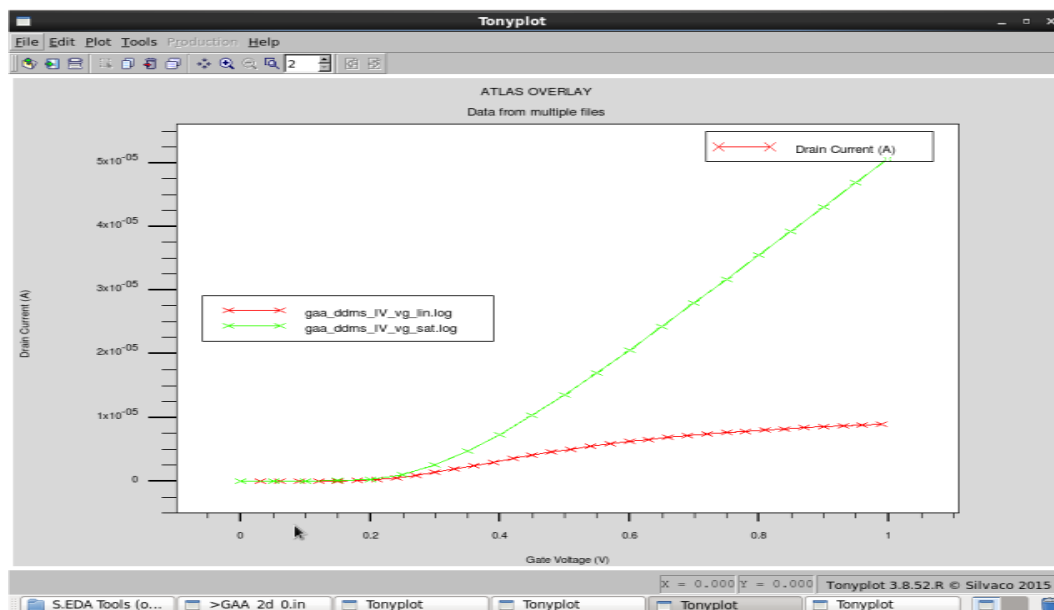
Figure 4.12: Drain current (I_D) versus gate voltage (V_{GS}) plot for V_{DS} =1 V and 0.1 V

Based on a constant current method, which is universally customized for drain current calculation, the threshold voltage (V_{th}) of the device is extracted [107]. The value of constant current is considered 1×10^{-7} A/m during the simulation [108, 109].

The drain current versus drain voltage characteristics, commonly referred to as the output characteristics or the I_D vs V_{DS} curve, of a MOSFET illustrate the relationship between the drain current (I_D) and the drain voltage (V_{DS}) for a given set of operating conditions. The transition characteristics of the GAA MOSFET for different gate voltages are shown in Figure 4.13. This plot provides insights into the behavior of the MOSFET and its different operating regions. In the triode/linear region, the MOSFET operates as a voltage-controlled resistor, and the drain current (I_D) is directly proportional to the drain-source voltage (V_{DS}). The drain current increases linearly with increasing V_{DS} until the MOSFET enters saturation [110, 111]. In the saturation region, the MOSFET operates as a voltage-controlled current source, and the drain current remains relatively constant despite further increases in V_{DS}.
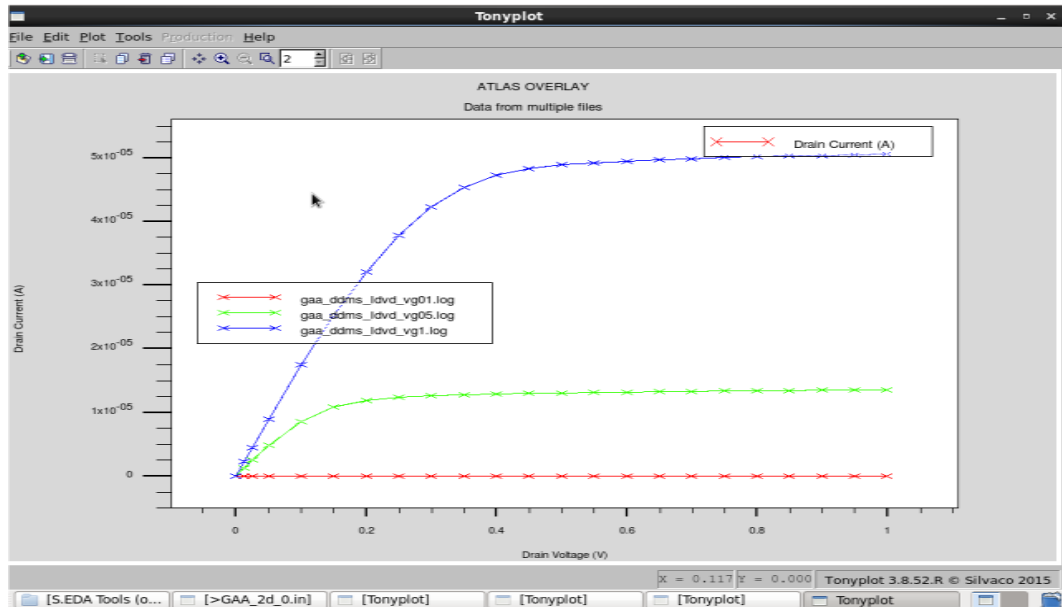
Figure 4.13: I_D vs V_{DS} characteristics

When the drain voltage is varied from 0.1 to 1 V, DIBL is calculated as the difference in threshold voltage.Driving current, I_{on} and sub-threshold current, I_{off} is estimated for different gate voltages. Figure 4.14 shows the driving current, I_{on} obtained at V_G=1.0 V, and I_{off} obtained at V_G= 0.1 V.
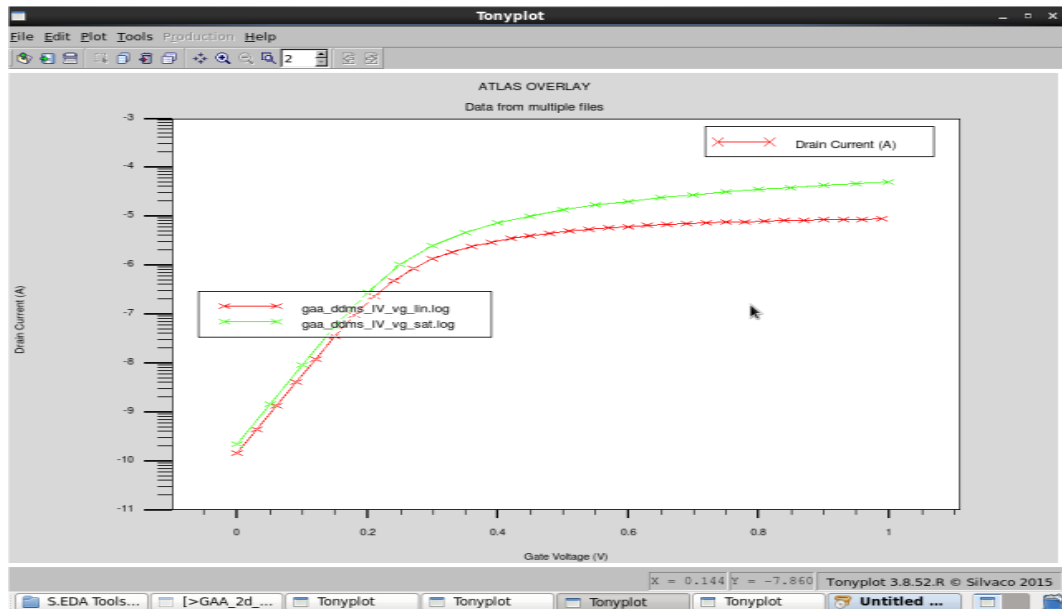
Figure 4.14: I_{on} & I_{off} current for different gate voltage V_{GS}

The simulated results are presented for different gate-source voltage (V_{GS}) in Table 4.4

Table 4.4: Parameter values after simulation

Parameter	Value
V_{th}	0.17 V
SS	61.5 mV/dec
DIBL	18.2 mV/V
I_{on}	7.74e-5 A
I_{off}	1.74e-10 A

4.5 COMPARISON OF 45nm AND 30nm CHANNEL LENGTH DEVICES

After the design and simulation of devices, the performance parameters are being compared with different channel lengths. From Figure 4.15, it has been observed that the threshold voltage at different drain voltages is less in 30 nm device as compared to 45nm device.
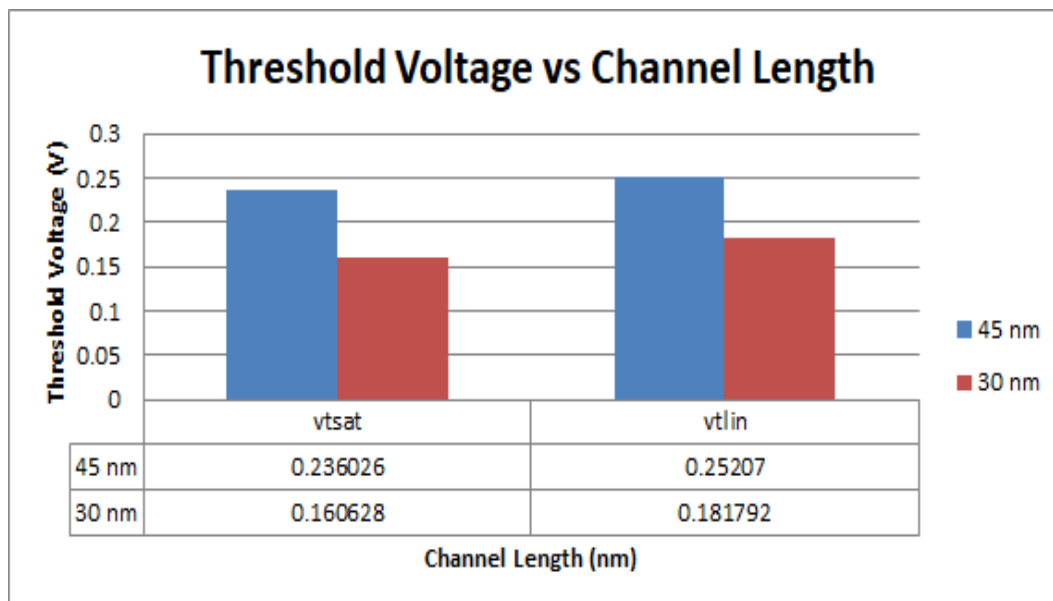
Figure 4.15: Threshold voltage comparison graph

It has been observed that the ON current is more in 30 nm device as compared to 45nm device as shown in Figure 4.16.
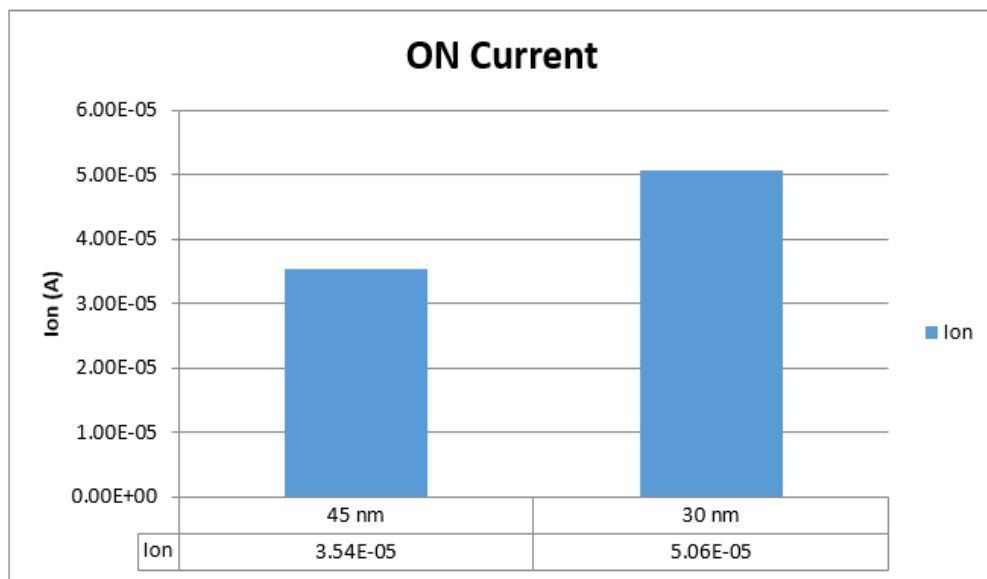
Figure 4.16: ON current comparison graph

The OFF current is also more in 30nm device equals to 2.20 e-11 A as shown in Figure 4.17.
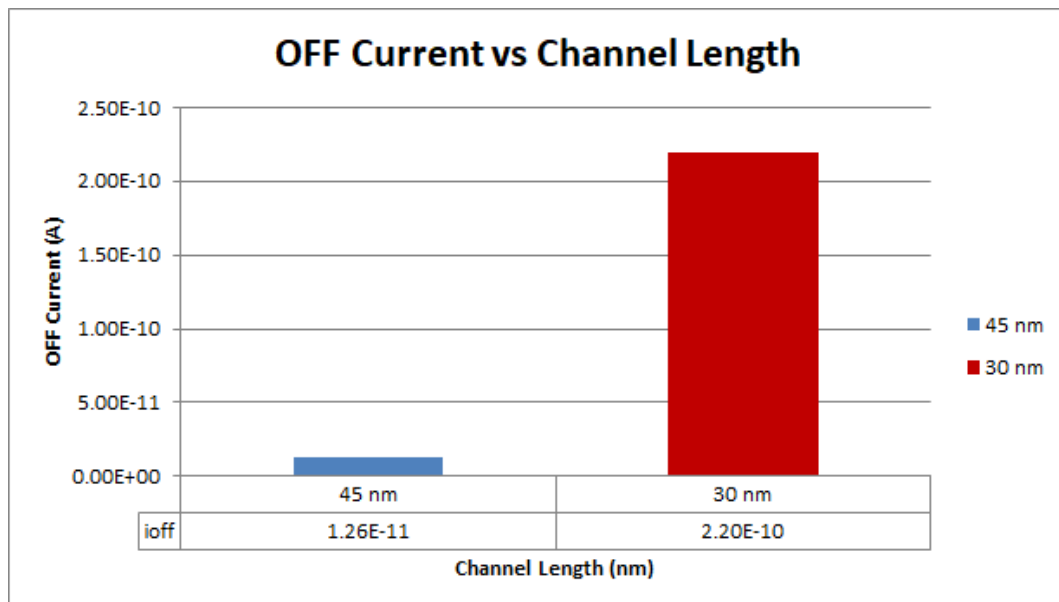
Figure 4.17: OFF current comparison graph

After the simulation of both devices and the calculation of ON current and OFF state leakage current, 45nm device has a better ON/OFF current ratio as shown in Figure 4.18

ON/OFF Current Ratio vs Channel Length

Channel Length (nm)	45 nm	30 nm
Ion/Ioff	2.80E+06	2.30E+05
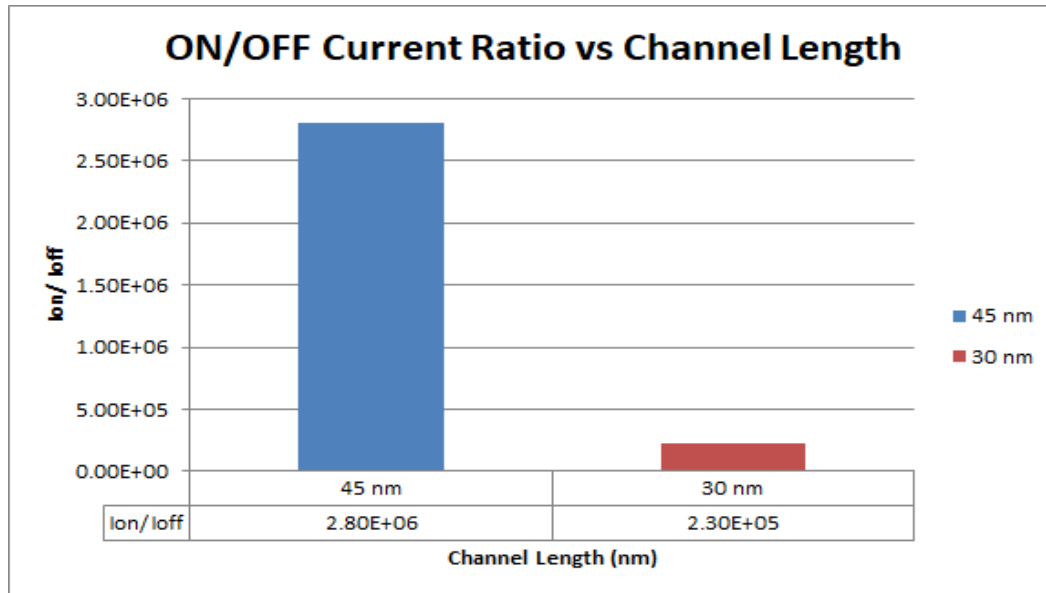
Figure 4.18: ON/OFF current ratio comparison graph

GAA is the probable option for MOS technology that can reduce the sub-threshold swing (SS) boundary and enhance the device efficiency [112, 113]. From Figure 4.19, 45nm device has less sub-threshold slope as compared to 30nm device.

Subthreshold Slope vs Channel Length

Channel Length (nm)	45 nm	30 nm
SS	60.2	61.4
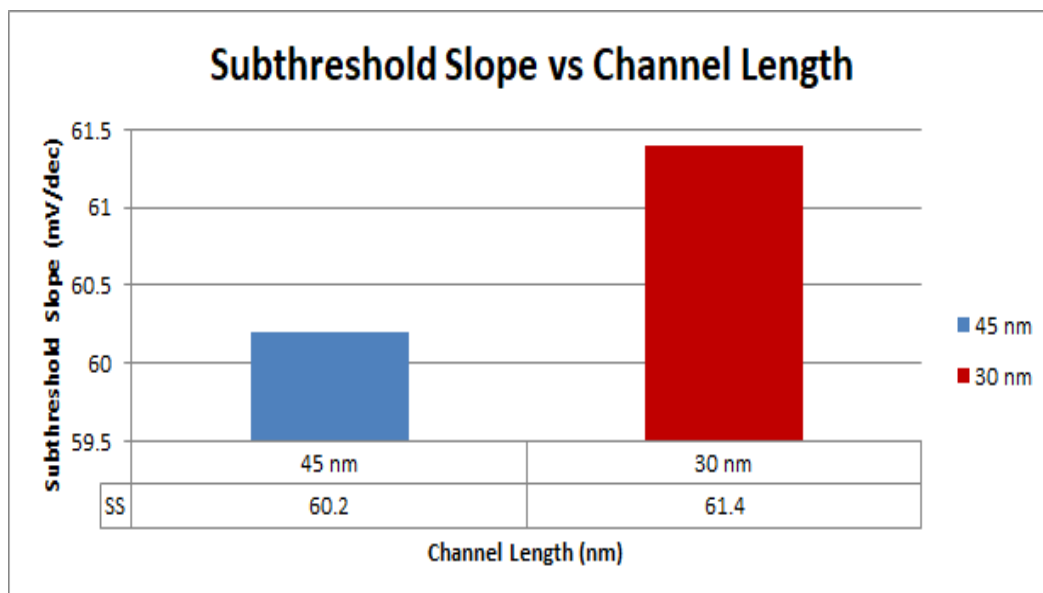
Figure 4.19: Subthreshold Slope comparison graph

It has been observed that 45nm device has better DIBL value as compared to 30nm device as shown in Figure 4.20
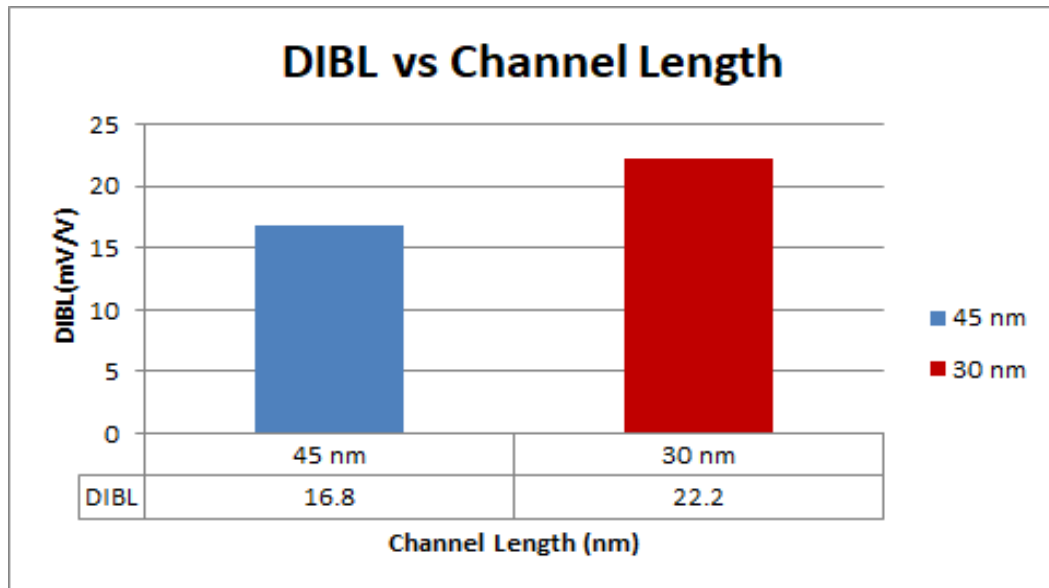
Figure 4.20: DIBL comparison graph

To explore their electrical response, three-dimensional (3-D) simulations of Gate All Around transistors with 30 nm channel length and 10 nm silicon film thickness are performed. The GAA devices have been found to show excellent control over impact ionization and bipolar amplification. As a result of cylindrical gate confinement, it also provides better electrostatic control over the channel. This design minimizes leakage current and improves control over the channel potential, resulting in better device performance. It is a promising transistor structure for future generations of integrated circuits, offering improved performance, better control, and scalability, making them an attractive option for advanced semiconductor technology nodes. However, Gate All Around MOSFET has low device driving capabilities. By optimizing the bandgap energy of the semiconductor, the driving capability of the device can be enhanced [114, 115].

4.6 CONCLUSION

In this chapter, the drain characteristics of 45nm and 30nm Cylindrical Gate All Around (CGAA) are explored and the performance evaluation is carried out with an extensive device simulator. Various electrical characteristics have been extracted i.e. Drain current (I_{on}), Sub-threshold current (I_{off}), DIBL, Sub-threshold slope, I_{on}/I_{off} ratio

after the simulation of the device in ATLAS. Also, the output (I_D–V_{DS}) and transfer (I_D–V_{GS}) characteristics of GAA FET have been plotted. As a result, it has been observed that with the increase of drain to source voltage and gate to source voltage, drain current increases. The simulated value of various parameters is compared with the literature review as well as analytical values. The drain current is significantly improved when the device approaches the nanowire.

CHAPTER 5

IMPACT ANALYSIS OF VARIOUS DESIGN PARAMETERS

5.1   IMPACT OF WORK FUNCTION

The continuous downscaling of the MOS devices has always sustained a requirement for the intense scaling in package density and performance resulting in efficient chip functionality for faster switching devices. However, due to the extreme vicinity between source and drain, the scaling of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) can decrease the gate control over the channel [116]. Cylindrical Gate All Around (GAA) MOSFET is a major invention and most promising candidate to replace conventional MOSFET, fit into the next generation. As the threshold voltage degrades, the Gate All Around MOSFET suffers from undesirable short channel effects. A Metal Gate Technology can be prevailing over this limitation by providing the desirable Gate work function [117]. This can also be done by regulating the threshold voltage by channel doping concentration but it decreases the device performance due to the dopant fluctuations, carrier mobility degradation, and large sub-threshold slope [118].

As the channel doping is increased, it increases the band to band tunneling effect between the substrate and the drain and hence the performance of Gate All Around MOSFET degrades [119]. It draws attention towards Gate work function as an alternative solution. To minimize the leakage current, the Metal Gate is used for submicron technology [120]. Metal Gate electrode desires to regulate threshold voltage to a preferred value to decrease short channel effects [121]. Here, the effect of Gate electrode work function on several electrical characteristics like MOS Threshold Voltage (V_t), ON current (I_{on}), Sub-threshold leakage current (I_{off}), ON/OFF current

ratio (I_{on}/I_{off}) and Drain Induced Barrier Lowering (DIBL) are extracted using ATLAS device simulator.

This chapter includes the impact of the work-function on 45nm Gate All Around MOSFET and estimation of various parameters that have been performed after the device is simulated at different work-functions. In this research work, the Gate work function (ϕ_m) is methodically evaluated and analyzed on different performance indicators such as threshold voltage (V_t), ON current (I_{on}), Subthreshold leakage current (I_{off}), ON/OFF current ratio (I_{on}/I_{off}), Subthreshold Slope and DIBL of Cylindrical All Around (CGAA) MOSFET. The Short channel effects generated due to the shortening of channel length can wisely be controlled and enhanced by appropriate modification of the work-function of the gate electrode [122]. All the device parameters are investigated using ATLAS device simulator. ATLAS is a 2D and 3D device simulator that accomplishes silicon and various other material-based devices for DC, AC and transient analysis [123]. ATLAS allows characterization and enhancement of the device for an extensive range of technologies.

5.1.1 Impact of Work-function on Threshold Voltage

Since the Metal gate work function can be accustomed to fulfill a given threshold voltage requirement, therefore the choice of the metal gate material will depend upon the metal which offers the suitable work function for the preferred threshold voltage [124].The threshold voltage can be written as

$$V_t = \phi_{ms} + 2\phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \qquad (5.1)$$

Where Q_{SS} signifies the charges in Gate Dielectric, C_{ox} is the Gate Oxide Capacitance, ϕ_{ms} is the work function difference between the semiconductor and gate electrode, ϕ_f is the difference between the fermi level, E_F and the intrinsic fermi level, E_{Fi} of the semi-conductor [125, 126].

In this simulation work, the Gate work function is varied from 4.4 eV to 4.6 eV to analyze the effect on threshold voltage of the device. It has been analysed that by increasing the gate work function of the Gate All Around MOSFET, the corresponding threshold voltage also increases to the chosen value as shown in Figure 5.1. The results as shown in this figure have been attained for a device having $L_g = 45nm, R = 5nm, t_{ox} = 1nm$.
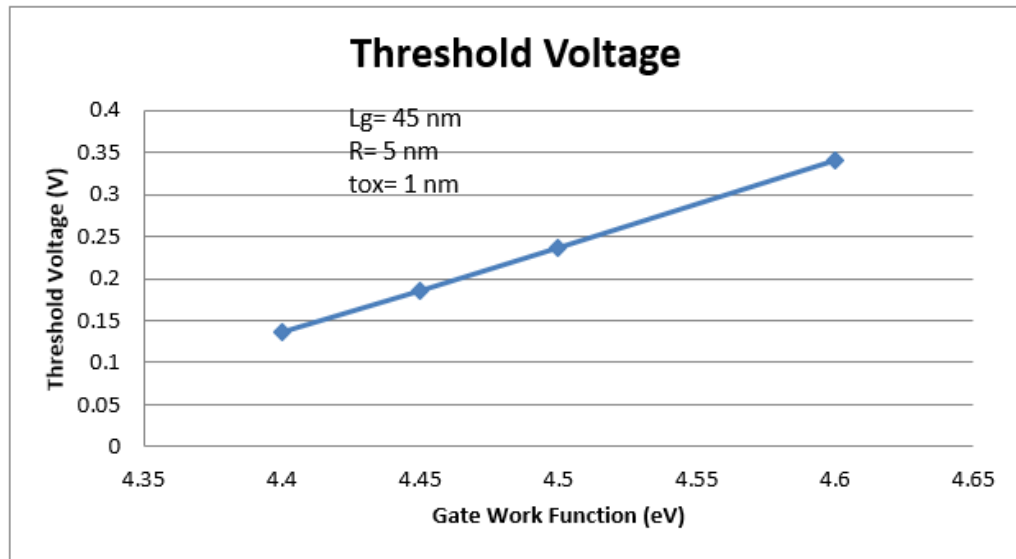
Figure 5.1: Threshold voltage deviation at various Gate work functions

Figure 5.2 shows the variation of threshold voltage at different work-functions. The simulation results show that the threshold voltage rises with the rise in the work-function of the Gate electrode. The work-function varies from 4.4 eV to 4.6 eV.

Work Function (eV)	vtsat	vtlin
$\phi = 4.4$	0.136026	0.15207
$\phi = 4.45$	0.186026	0.20207
$\phi = 4.5$	0.236026	0.25207
$\phi = 4.6$	0.339816	0.35207
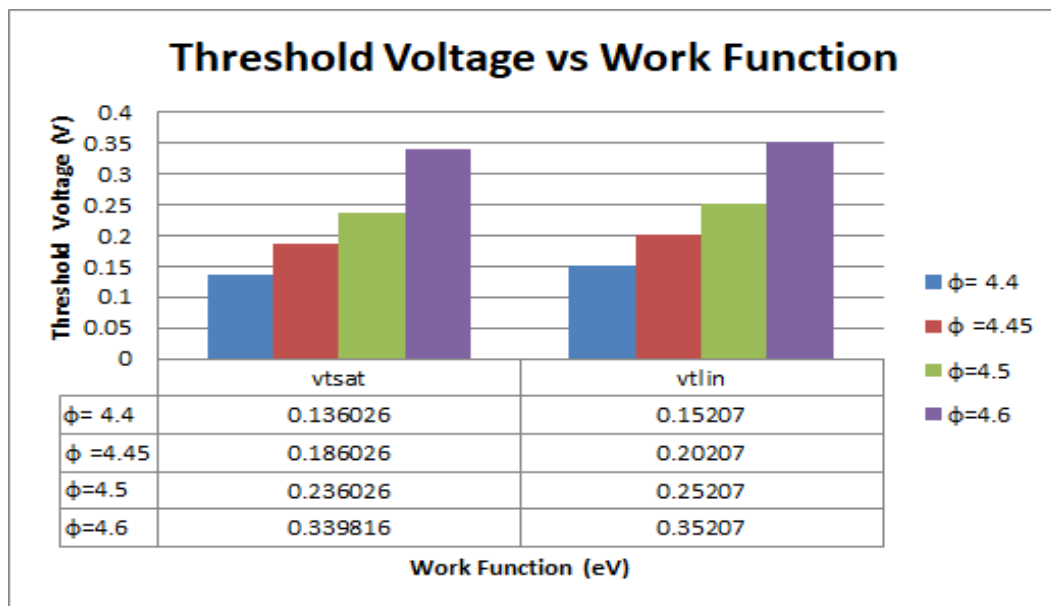
Figure 5.2: Threshold voltage comparison at various Gate work functions

5.1.2 Impact of Work-function on Drain Current and Sub-threshold Current

Figure 5.3 shows the ON Current behavior of the device as a function of the Gate work function. As the threshold voltage and the Metal Gate work function of the Cylindrical Gate All Around MOSFET increases, the ON current of the device decreases.
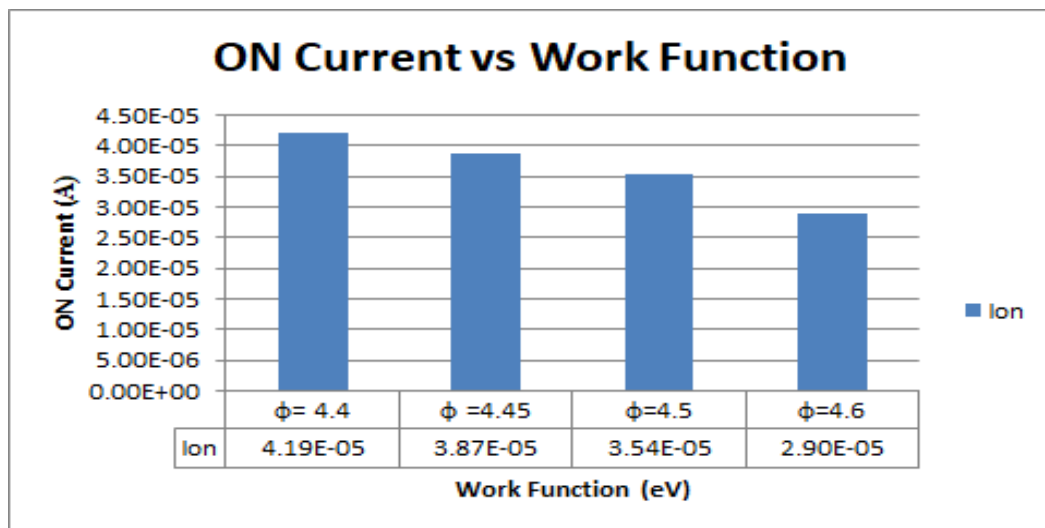
Figure 5.3: ON current behavior at various Gate work functions

The transfer characteristics of a MOSFET, also known as the output characteristics or I_{DS}-V_{GS} curve, illustrate the relationship between the drain current (I_{DS}) and the gate-source voltage (V_{GS}) for a given drain-source voltage (V_{DS}). Figure 5.4 shows transfer characteristics (I_{DS}-V_{GS} characteristics) in linear mode for different values of Gate work function. The work function is ranging from 4.4 eV to 4.6 eV.
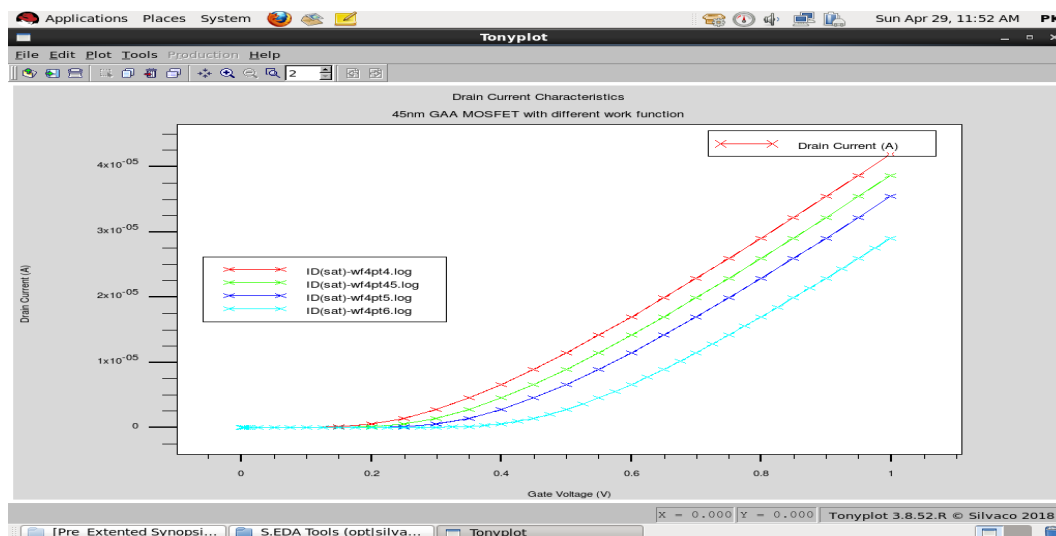
Figure 5.4: Drain characteristics in linear mode

Figure 5.5 shows the plot between drain current versus the gate voltage (I_{DS}–V_{GS}) in the logarithmic mode of the Gate All Around MOSFET for various values of work function. The plot shows as the metal gate work function increases, the sub-threshold behavior of the device improves. The improvement in the efficiency of the device is due to the increase in work function, the corresponding threshold voltage increases which lead to a decrease in sub-threshold current.
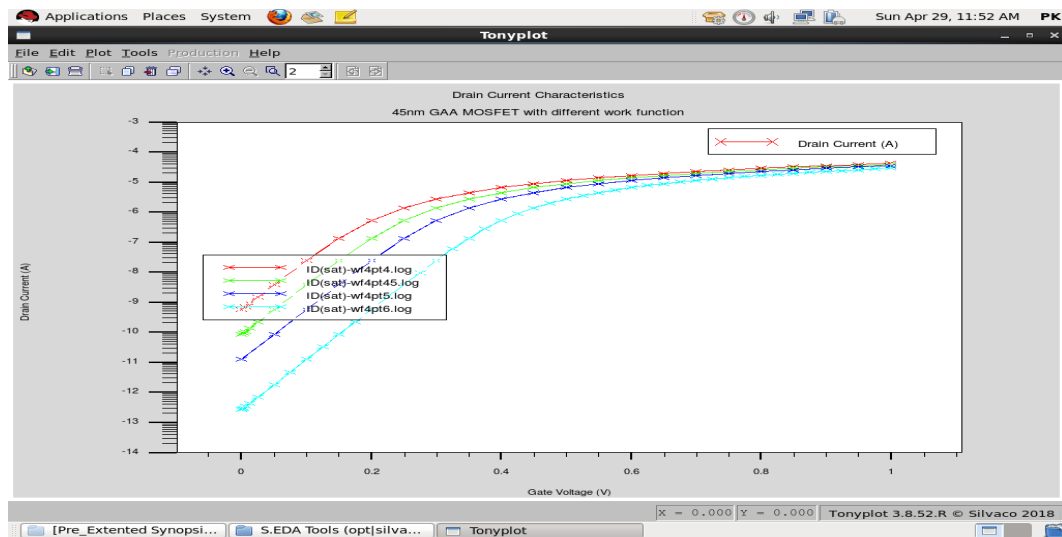
Figure 5.5: Drain characteristics in logarithmic mode

The trans-conductance versus gate voltage plot, also known as the trans-conductance characteristics, illustrates the relationship between the trans-conductance (gm) and the gate-source voltage (V_{GS}) of a MOSFET. Figure 5.6 shows the plot between trans-conductance versus the gate voltage for various values of work function.
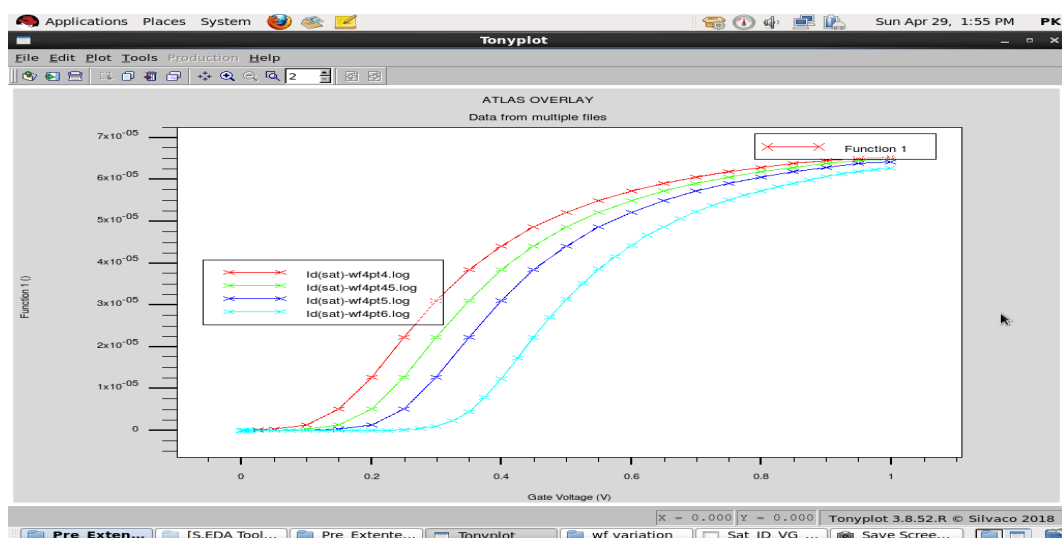
Figure 5.6: Trans-conductance at various work functions

In a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), the OFF-state current refers to the leakage current that flows between the drain and source terminals when the transistor is in the off or non-conducting state. In the off state, the gate-source voltage (V_{GS}) is typically below the threshold voltage (Vth), and the transistor is designed to be non-conductive [127]. The OFF current of the device as a function of the Gate work function has been illustrated in Figure 5.7. It is clearly shown that OFF current of the device also decreases as there is an increase in the metal gate work function of the Gate All Around MOSFET structure.

OFF Current vs Work Function

	ϕ= 4.4	ϕ =4.45	ϕ=4.5	ϕ=4.6
Ioff	5.75E-10	8.55E-11	1.26E-11	2.74E-13
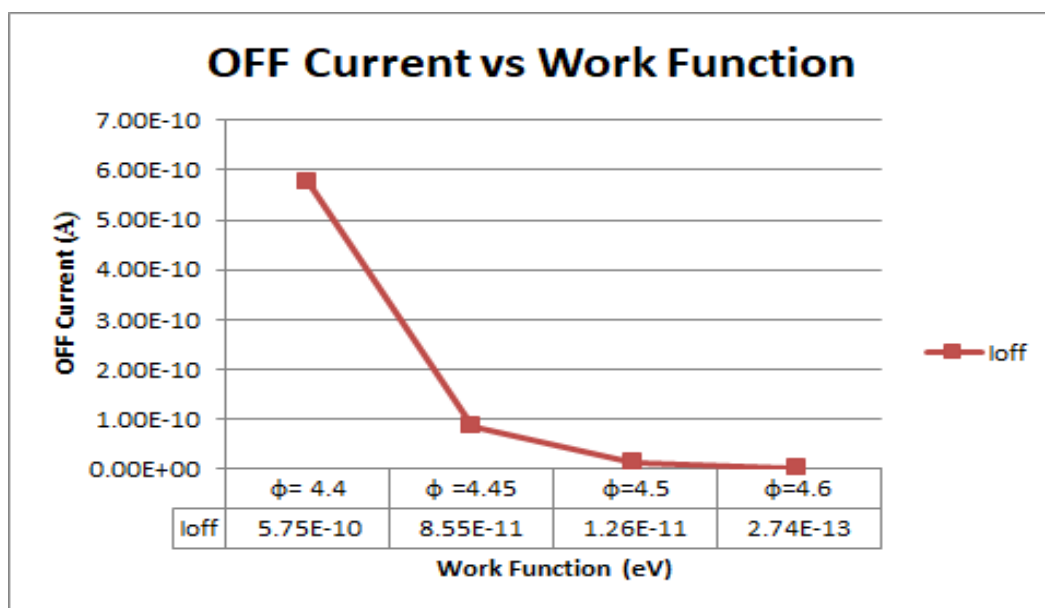
Work Function (eV)

Figure 5.7: OFF current behaviour at various Gate work functions

5.1.3   Impact of Work-function on ON/OFF Current Ratio

The I_{on}/I_{off} current ratio of the device as a function of the Gate work function has been clarified in Figure 5.8. It is clearly shown in the plot that the device I_{on}/I_{off} current ratio extracted from the device simulator has been considerably enhanced with the rise in the Gate work function of the Cylindrical Gate All Around MOSFET.. Even though the on current sacrifice up to some extent as the gate work function increases, but improvement in the I_{on}/I_{off} current ratio is a strong sign of progress in device performance which is required in fast switching operations.

ON/OFF Current Ratio vs Work function

	φ= 4.4	φ =4.45	φ=4.5	φ=4.6
Ion/Ioff	7.29E+04	4.52E+05	2.80E+06	1.06E+08
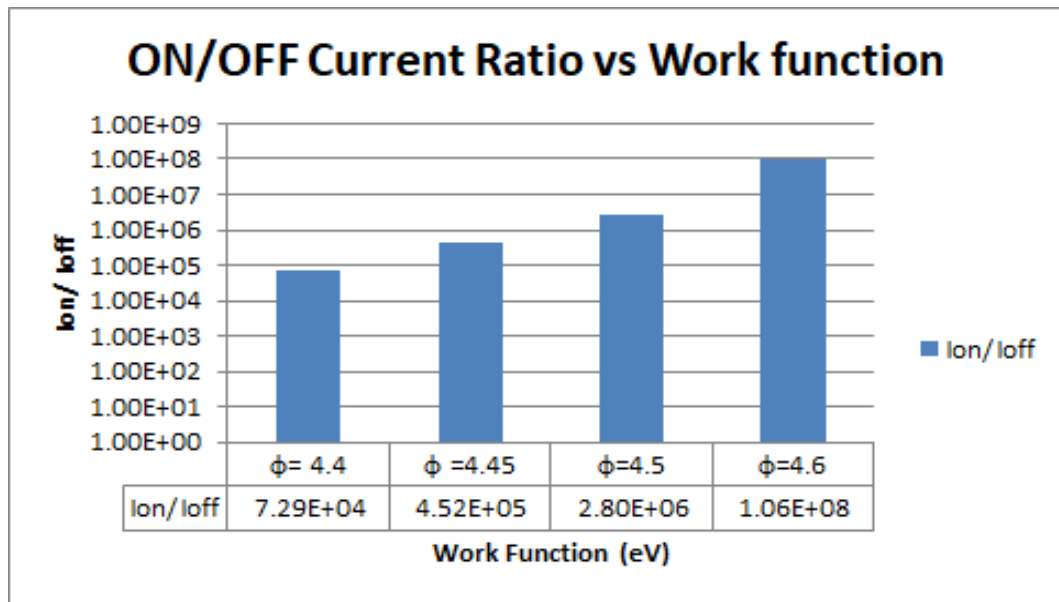
Work Function (eV)

Figure 5.8: ON/OFF current ratio at various Work-functions

5.1.4 Impact of Work-function on DIBL

The Drain Induced Barrier Lowering (DIBL) effect is defined as the lateral shift of the transfer curves in the sub-threshold regime when the drain voltage varies from 0.05 V to 1 V [128]. It is one of the serious short channel effect parameters in submicron devices, as it evaluates the overall electrostatic gate control on a channel [129]. The DIBL behavior as a function of the gate work function has been shown in Figure 5.9.

DIBL vs Work function

	φ= 4.4	φ =4.45	φ=4.5	φ=4.6
DIBL	16.9	16.8	14.2	12.8
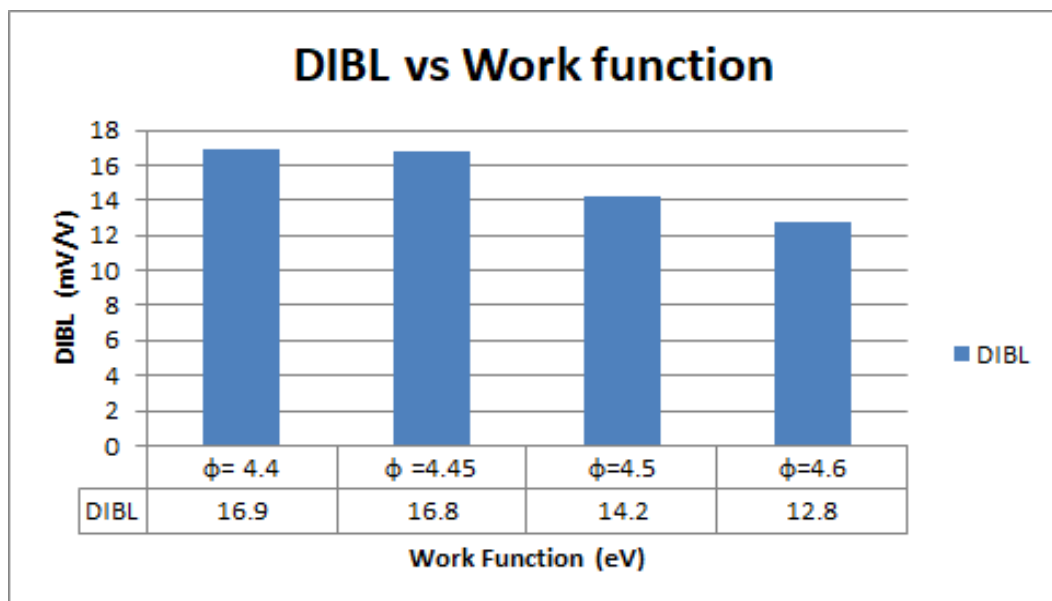
Work Function (eV)

Figure 5.9: DIBL deviation at various Gate work functions

The effect of DIBL in nano-scale devices is to decrease threshold voltage by applying drain voltage to change the source to drain potential to enable the conduction of the channel even for the smaller gate voltage [130, 131]. It is depicted from Figure 5.9 that DIBL decreases as the gate work function increases.It is due to the increase in threshold voltage with the gate work function as a result, the DIBL effect is reduced.

5.1.5 Impact of Work-function on Subthreshold Slope

Figure 5.10 shows the plot between the Sub-threshold Slope and gate work function. It is depicted from the graph that the Sub-threshold Slope of the Gate All Around MOSFET structure improves as the work function of the gate electrode increases. It is because of the enhanced threshold voltage with the rise in gate work function.
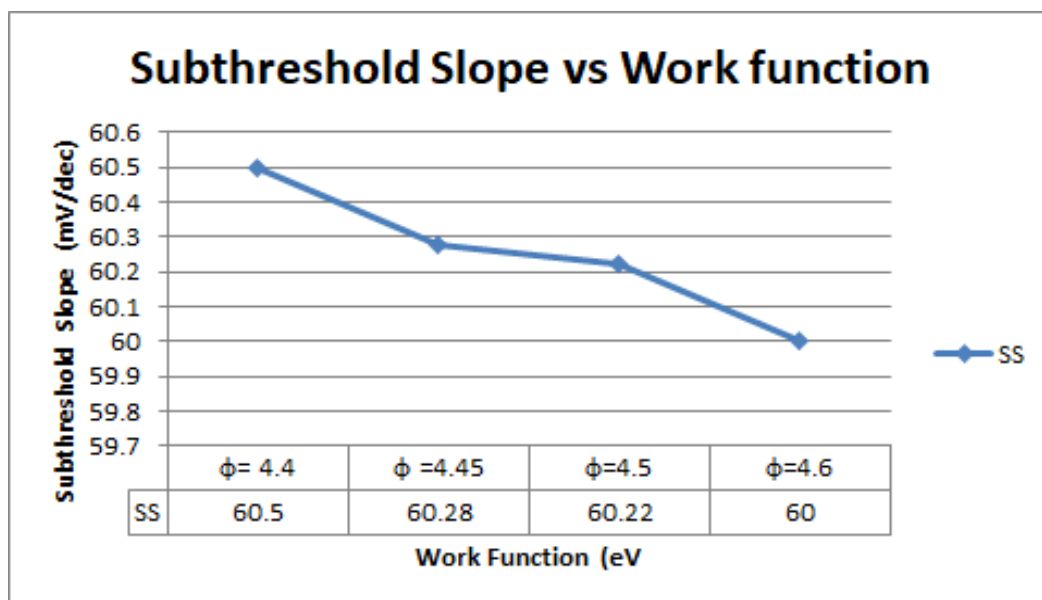
Figure 5.10: Variation of Subthreshold Slope with work-function

It has been analysed that the device has a higher driving current and leakage current for work function 4.4 eV as matched to work function 4.5 eV and 4.6 eV. But the ratio of I_{ON}/I_{OFF} current increases by increasing the work function ranging from 4.4 eV to 4.6 eV. It is also observed Tthat the Cylindrical Gate All Around MOSFET having work function 4.6 eV has a greater threshold voltage and lower DIBL effect. Hence, the leakage current has been reduced with the variation in work function.

The parameter extraction results after the simulation is elaborated in Table 5.1.

Table 5.1: Work-function variation simulated results

ϕ_m (eV)	I_{on} (A)	I_{off} (A)	(I_{on}/I_{off})	V_{th} (V)	DIBL (mV/V)
4.4	1.33e-3	1.83e-8	7.29e4	0.13	16.8
4.45	1.23e-3	2.72e-9	4.52e5	0.18	15.9
4.5	1.13e-3	4.01e-10	2.82e6	0.23	14.7
4.6	9.24e-4	8.72e-12	1.06e8	0.33	12.8

5.2 IMPACT OF SILICON FILM THICKNESS

Scaling the base component measure directly affects Short Channel Effects (SCE), for example, the effect of charge sharing close to source/deplete transporter expansion, Drain Induced Barrier Lowering, and Punch Through Effect. For Silicon On Insulator (SOI) advances, scaling additionally requires a diminishment of both the silicon film and buried oxide thickness with a specific end goal to decrease the Short Channel effects (SCE). [132]. This will impact the threshold voltage, which as indicated by the traditional hypothesis is relied upon to be brought down for reduced gate lengths and film thickness. The developing interest in economical gadgets with complex functionalities and truculent scaling in package density and execution dependably move toward becoming necessities [133]. In turn, the ceaseless growth in the framework necessities requests a more elevated amount of integration and execution which have been comprehended by persistent downscaling of MOS devices. However, MOS transistor scaling has resulted in unacceptable leakage currents beyond the sub-threshold region.

In the past couple of years, analysts show solid consideration and enthusiasm towards surrounded nanowire MOSFET rather than planner structure MOS. Cylindrical Gate All Around (GAA) MOSFET is a remarkable innovation and most encouraging contender to replace the traditional MOSFETs. The scaling of silicon film thickness is needed to improve the undesired short channel effects and to reduce the floating body effect [96]. This can, however, make the feature of the transistor different from adequate thin-film devices.

It has been remarked that scaling down the silicon film thickness has a strong influence on the threshold voltage and sub-threshold leakage due to the effect of edge-based transistors [134]. The effect of silicon film thickness on various electrical characteristics like MOS Threshold voltage (V_t), ON current (I_{ON}), Sub-threshold leakage current (I_{OFF}), ON/OFF current ratio (I_{on}/I_{off}) and DIBL are explored. The characteristics of the Gate All Around MOSFET have been explored in terms of the requirement of various performance device metrics on silicon film thickness (t_{si}). Here, the effect of silicon film thickness on numerous performance metrics like threshold voltage (V_t), ON current (I_{on}), Subthreshold leakage current (I_{off}), ON/OFF current ratio (I_{on}/I_{off}) and DIBL of cylindrical GAA are comprehensively evaluated and analysed. It has been observed that Gate All Around MOSFET offers high drive current (I_{on}), low off state current (I_{off}), superior ON/OFF current ratio (I_{on}/I_{off}) and hence enhanced gain. Thus, for ultra-low power applications surrounding nanowire is contemplated as a superior aspect.

In advanced MOSFET technologies, the silicon film thickness is typically in the range of a few nanometers. As technology nodes have been scaled down over the years, the silicon film thickness has also decreased to maintain proper control over the channel and improve device performance. Figure 5.11 shows the device structure for silicon film thickness t_{si}=10nm. The channel region of the MOSFET consists of a thin layer of silicon with a thickness of 10nm.

Figure 5.11: Device Structure for $t_{si} = 10nm$

Figure 5.12 shows the device structure for silicon film thickness t_{si}=5nm. The channel region of the MOSFET consists of a thin layer of silicon with a thickness of 5nm.

Figure 5.12: Device Structure for $t_{si} = 5nm$

Figure 5.13 shows the device structure for silicon film thickness t_{si}=4nm. The channel region of the MOSFET consists of a thin layer of silicon with a thickness of 4nm.
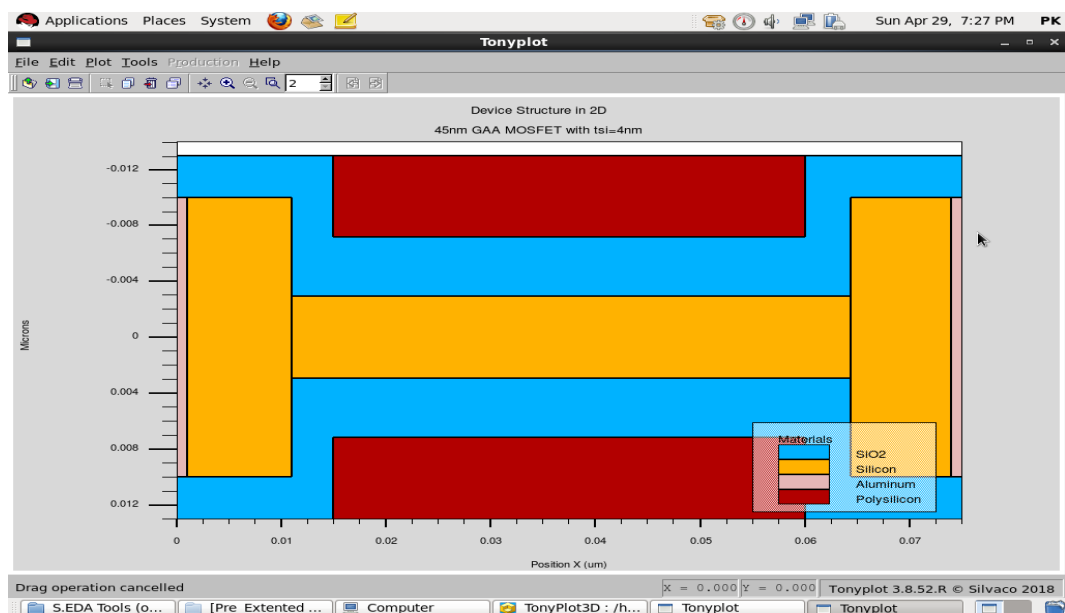
Figure 5.13: Device Structure for $t_{si} = 4nm$

Figure 5.14 shows the device structure for silicon film thickness t_{si}=2.5nm. The channel region of the MOSFET consists of a thin layer of silicon with a thickness of 2.5nm.
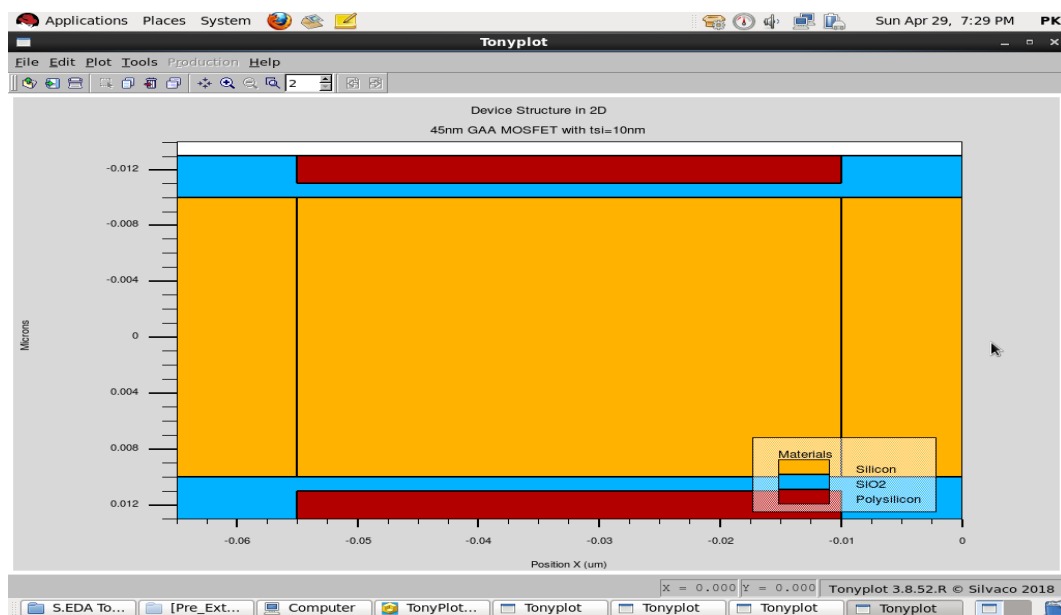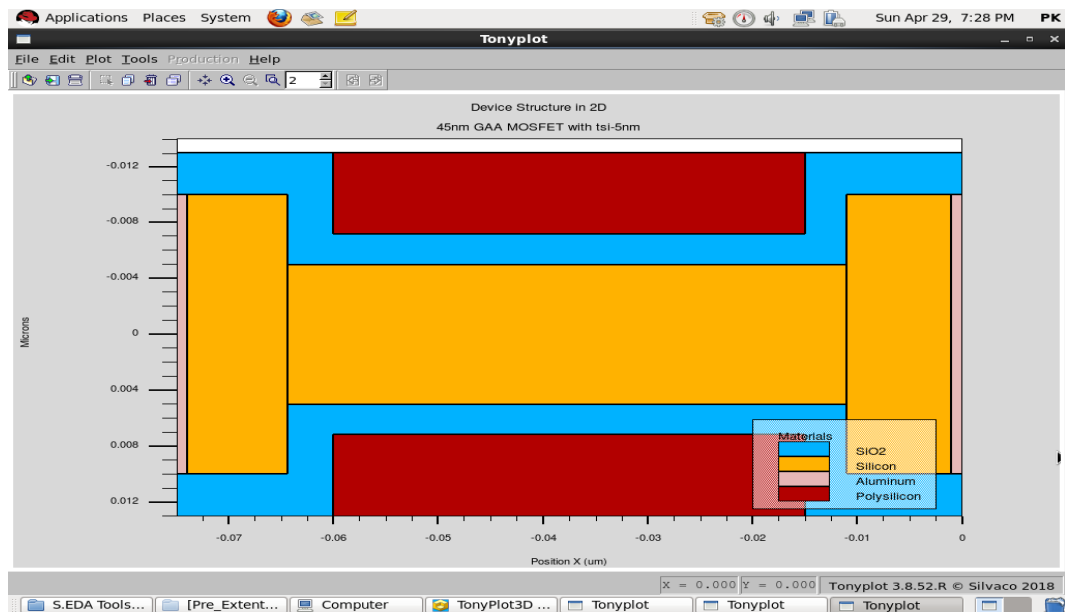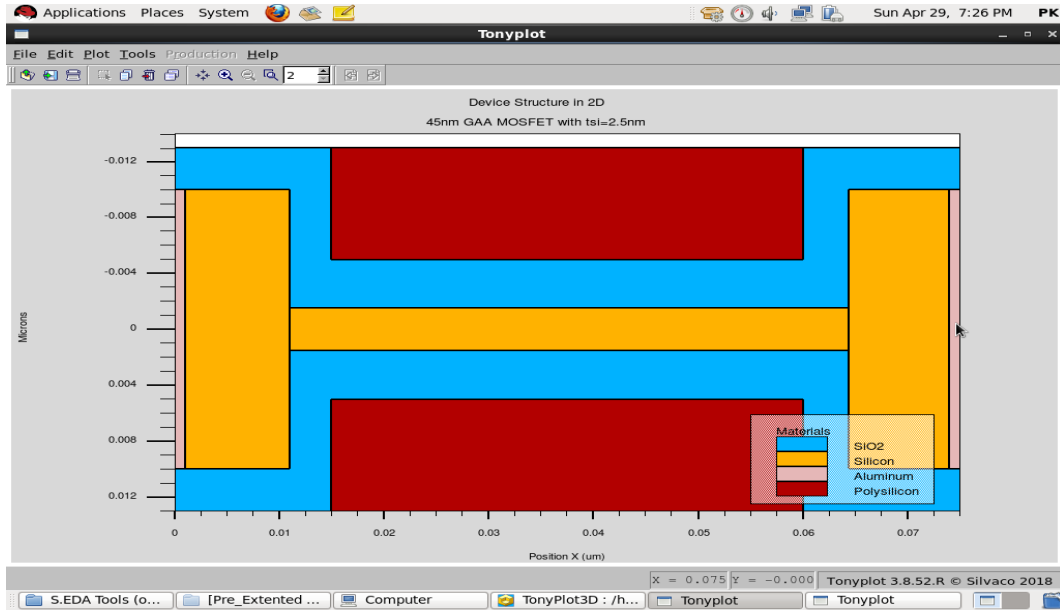

Figure 5.14: Device Structure for $t_{si} = 2.5nm$

5.2.1 Impact of Silicon Film Thickness on Threshold Voltage

The threshold voltage (V_t) variation as a function of film thickness varies from 2.5 nm to 10 nm is examined in the present simulation study. For CGAA MOSFET threshold voltage can be stated as

$$V_{th} = V_{fb} + \phi_{smin-th} + \frac{\lambda q N_a}{4\varepsilon_{si}} \left(1 - \frac{t^2_{si}}{\lambda} \right) \tag{5.2}$$

Where V_{fb} is flat band voltage, $\phi_{smin\text{-}th}$ is the value of the surface potential at which the volumetric inversion electron charge density in the Si device is equal to the substrate doping.

$$\lambda = t^2_{si} \left(1 + \frac{2\,\varepsilon_{si}\,t_{ox}}{\varepsilon_{ox}\,t_{si}} \right) \tag{5.3}$$

ε_{ox} and ε_{si} are the permittivity of SiO_2 and Si respectively. As the silicon film thickness decreases, the MOSFET channel becomes more susceptible to short-channel effects. Short-channel effects, such as drain-induced barrier lowering (DIBL) and channel length modulation, can cause a reduction in the threshold voltage. Figure 5.15 shows the threshold voltage variation as a function of silicon film thickness.
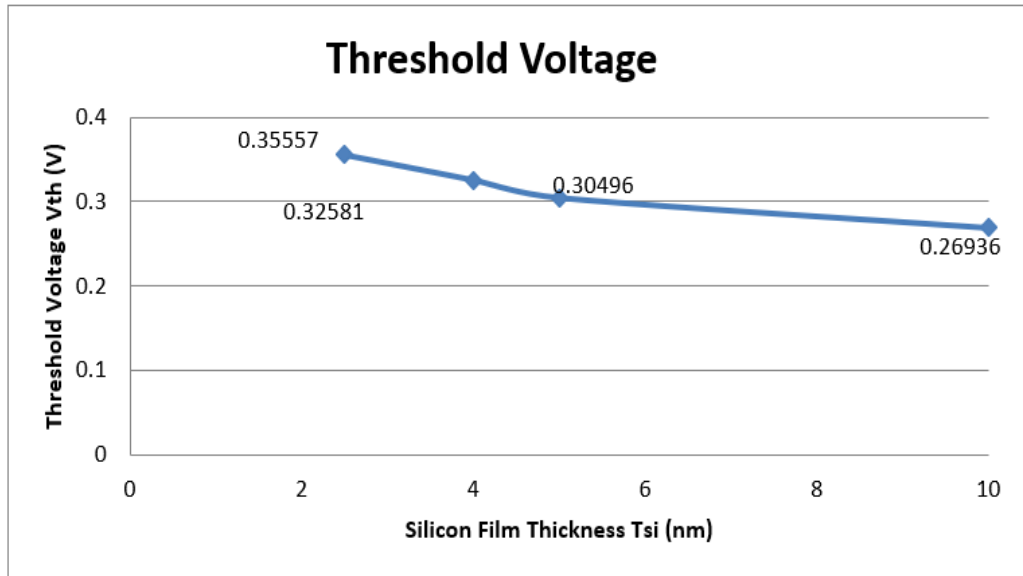
Figure 5.15: Threshold voltage at various Silicon film thickness

It has been analysed that by decreasing the silicon film thickness of Cylindrical Gate All Around MOSFET, the corresponding threshold voltage increases as shown in Figure 5.16. The device exhibiting the results in this figure has specifications $L_g =$
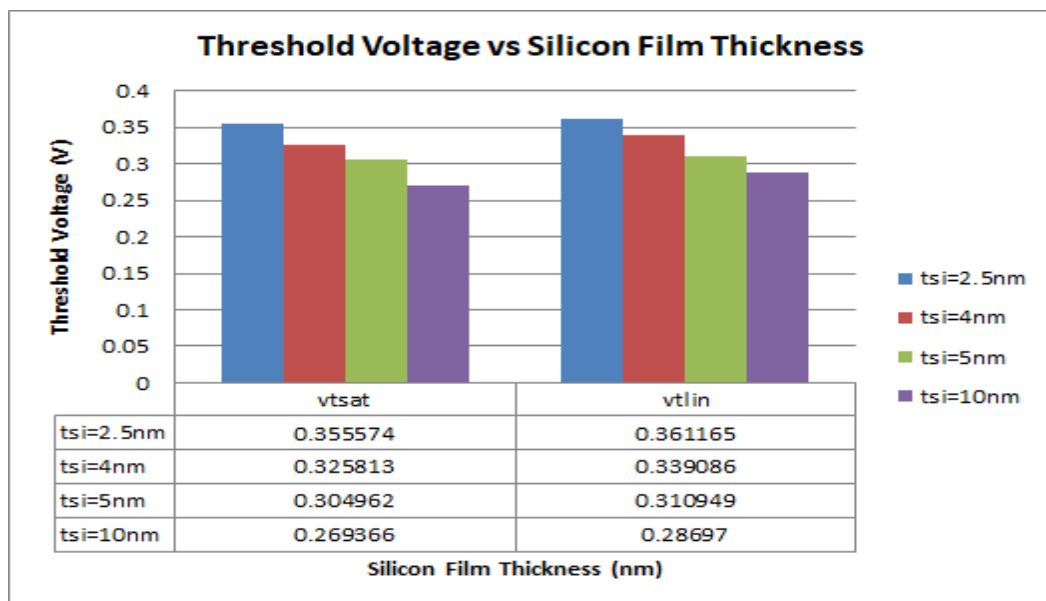
Figure 5.16: Threshold voltage comparison at various Silicon film thickness

$45nm, R = t_{si/2} = 5nm, t_{ox} = 1nm$. This increase in threshold voltage as the decrease in film thickness is because of the rise of the minimum energy for holes within the valence band. It is well-identified that the inversion carrier concentration required to achieve threshold voltage is increased as the silicon film thickness is decreased.

5.2.2 Impact of Silicon film thickness on drain Current and sub-threshold current

The ON current behavior of the device as a function of silicon film thickness has been illustrated in Figure 5.17. It has been observed that the ON current of the device is deteriorates as threshold voltage increases with a decrease in film thickness.
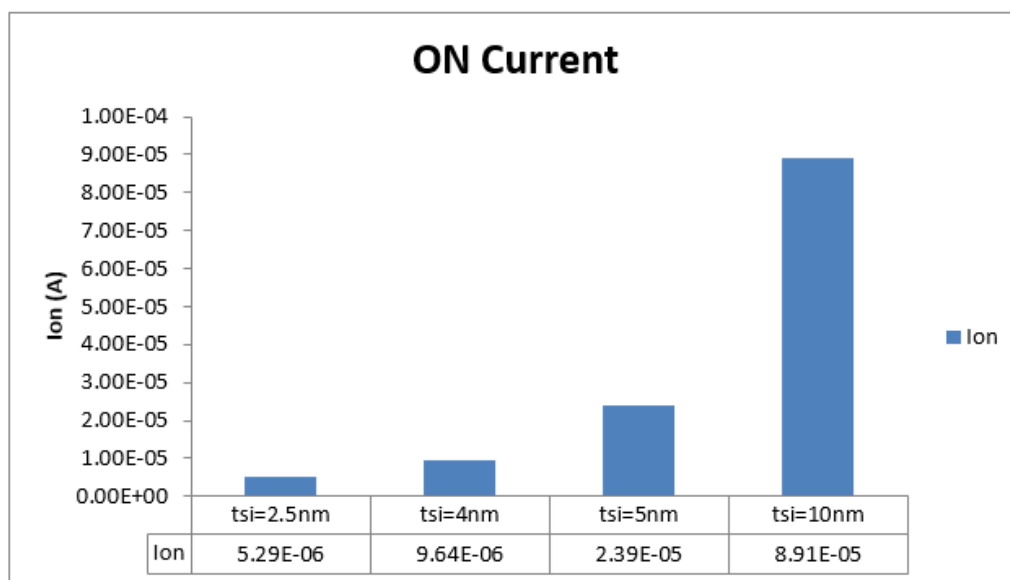
Figure 5.17: ON current at various Silicon film thickness

The transfer characteristics, also known as the output characteristics or I_D-V_{GS} curve, provide a graphical representation of this relationship. Figure 5.18 shows the I_D-V_{GS} transfer characteristics for different silicon film thickness at V_{DS}=0.05 V.
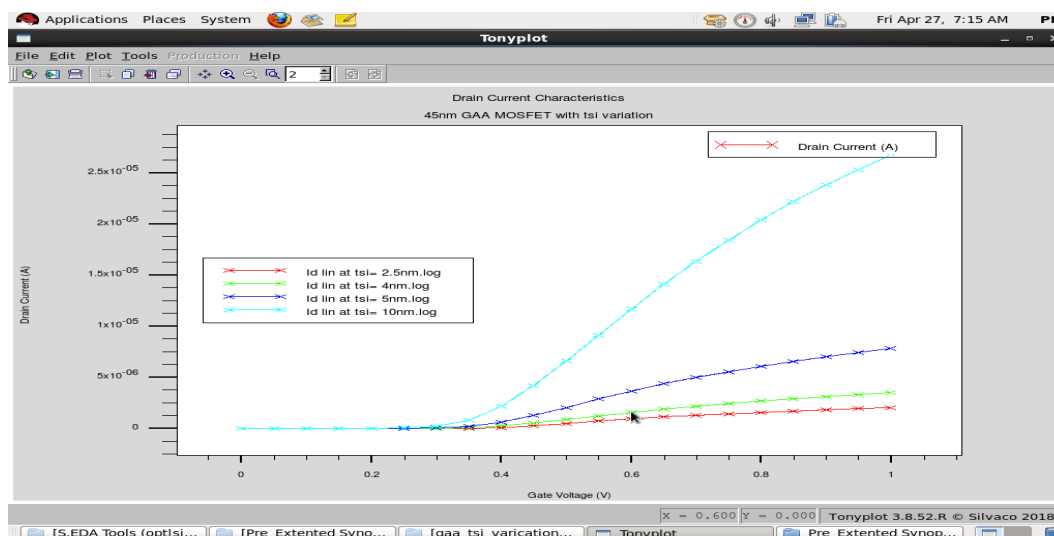
Figure 5.18: Drain current characteristics at different t_{si}

In the logarithmic mode of operation, the transfer characteristics of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) are plotted using a logarithmic scale for both the drain current (I_D) and the gate-source voltage (V_{GS}). This plot is commonly referred to as the I_D-V_{GS} characteristics in logarithmic scale or the transfer characteristics in the log-scale. Figure 5.19 shows the I_D-V_{GS} transfer characteristics in logarithmic mode at $V_{DS} = 0.05$ V.
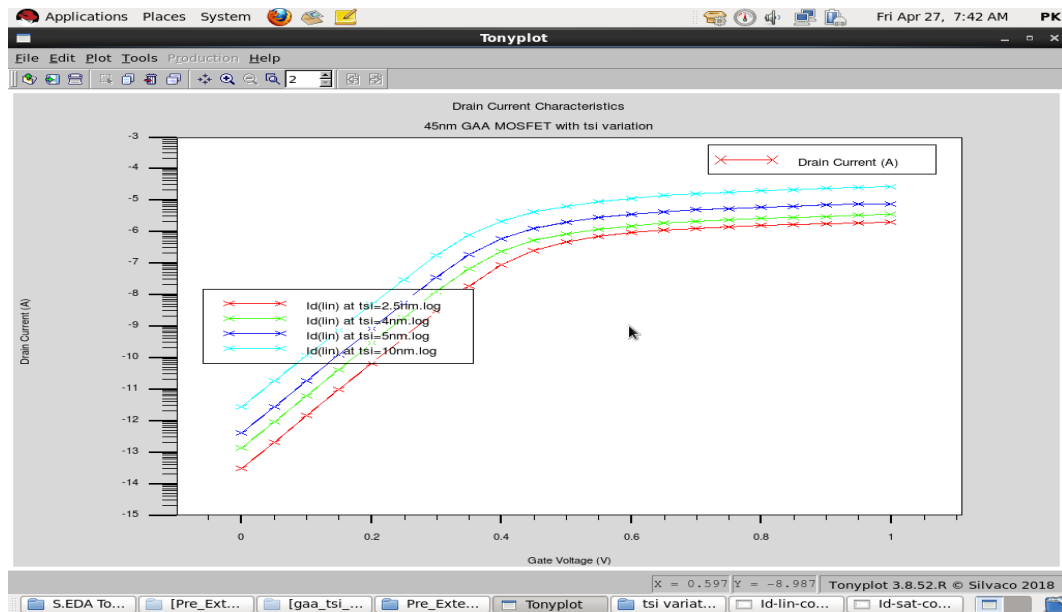
Figure 5.19: OFF current characteristics at different t_{si}

Figure 5.20 shows the I_D-V_{GS} transfer characteristics in linear mode at V_{DS}= 1 V.
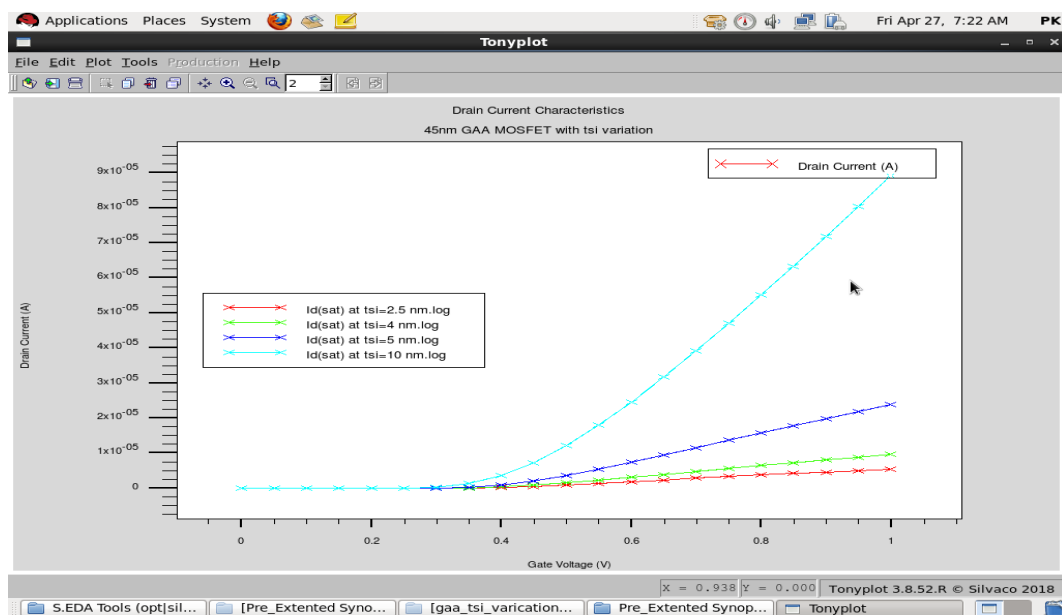
Figure 5.20: Drain current characteristics at different silicon thicknesses

Figure 5.21 shows the I_D-V_{GS} transfer characteristics in Logarithmic mode at $V_{DS}=$ 1V.
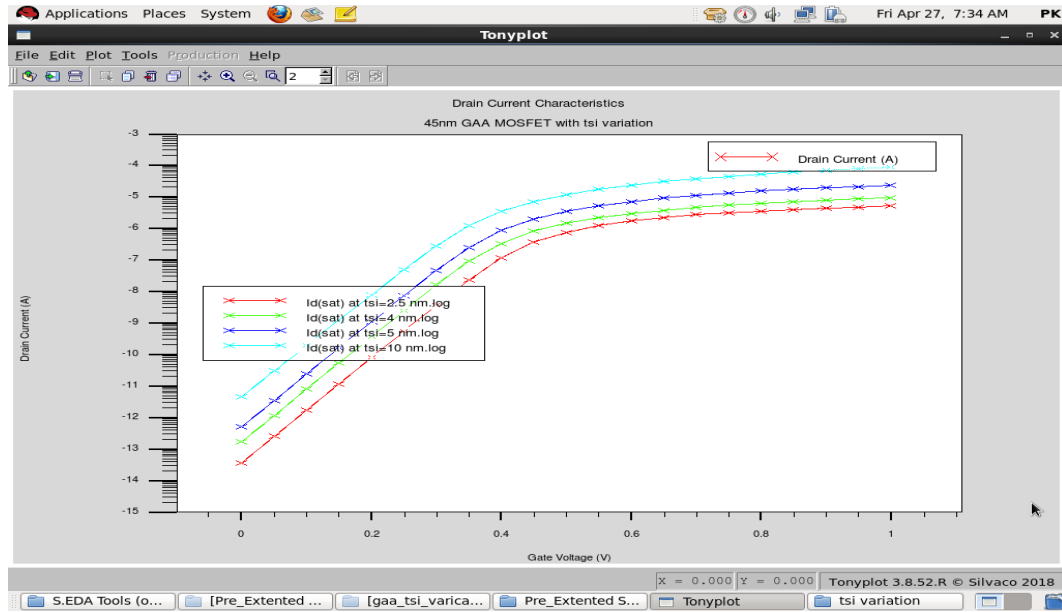
Figure 5.21: Drain current characteristics (in log mode) at different Silicon film thicknesses

The OFF current behavior of the device as a function of film thickness has been illustrated in Figure 5.22. It is clear that the OFF current of the device also decreases as
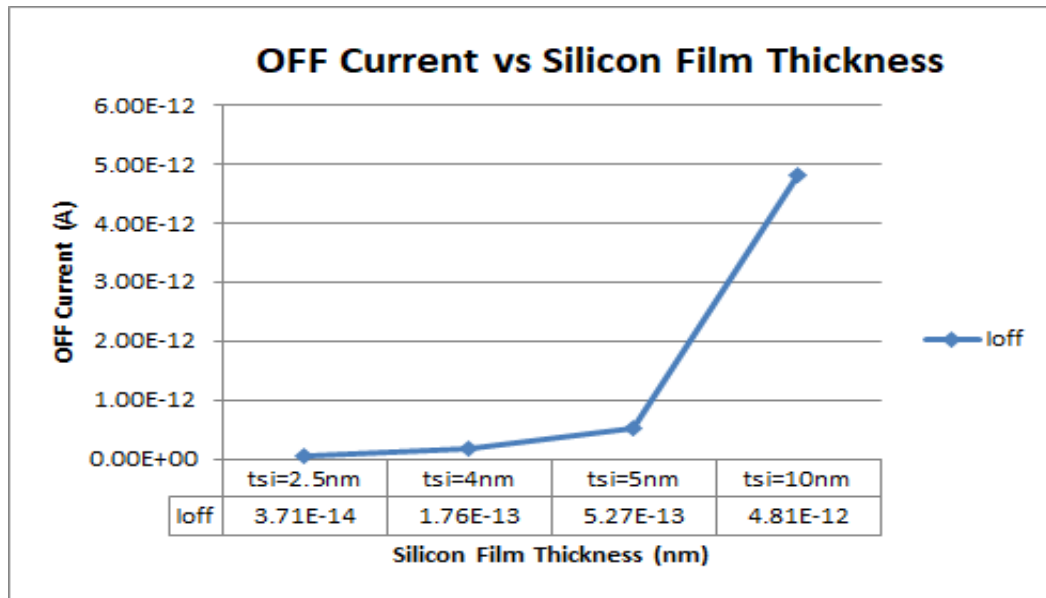
Figure 5.22: OFF current behaviour at various Silicon film thickness

a decrease in film thickness of the Gate All Around MOSFET.

5.2.3   Impact of Silicon Film Thickness on ON/OFF ratio

The I_{on}/I_{off} current ratio behavior of the device as a function of silicon film thickness has been illustrated in Figure 5.23. It is clearly shown in the plot that the device I_{on}/I_{off}
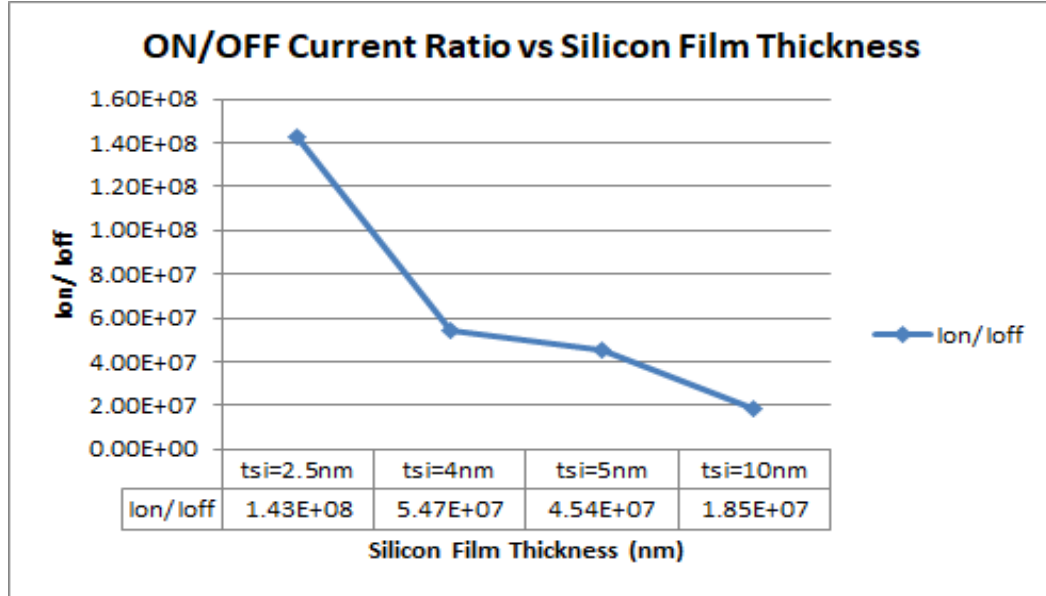
Figure 5.23: ON/OFF current ratio at different t_{si}

current ratio extracted from the device simulator has been considerably enhanced with the decrease in silicon film thickness of the Gate All Around MOSFET structure. Even though the on current sacrifices up to some extent as the silicon film thickness decreases, but progress in the I_{on}/I_{off} current ratio is a rich sign of enhancement in device performance which is required in fast switching operations.

5.2.4   Impact of Silicon film thickness on DIBL

The DIBL behavior as a function of silicon film thickness has been illustrated in Figure 5.24. It is depicted from the plot that DIBL reduces as the silicon film thickness is reduced. It is because of the increase in threshold voltage with the decrease in silicon film thickness, DIBL effect is decreased for a given drain voltage. The drain-induced barrier lowering (DIBL) effect is defined as the lateral shift of the transfer curves in the sub-threshold regime when the drain voltage varies from 0.05 V to 1 V.
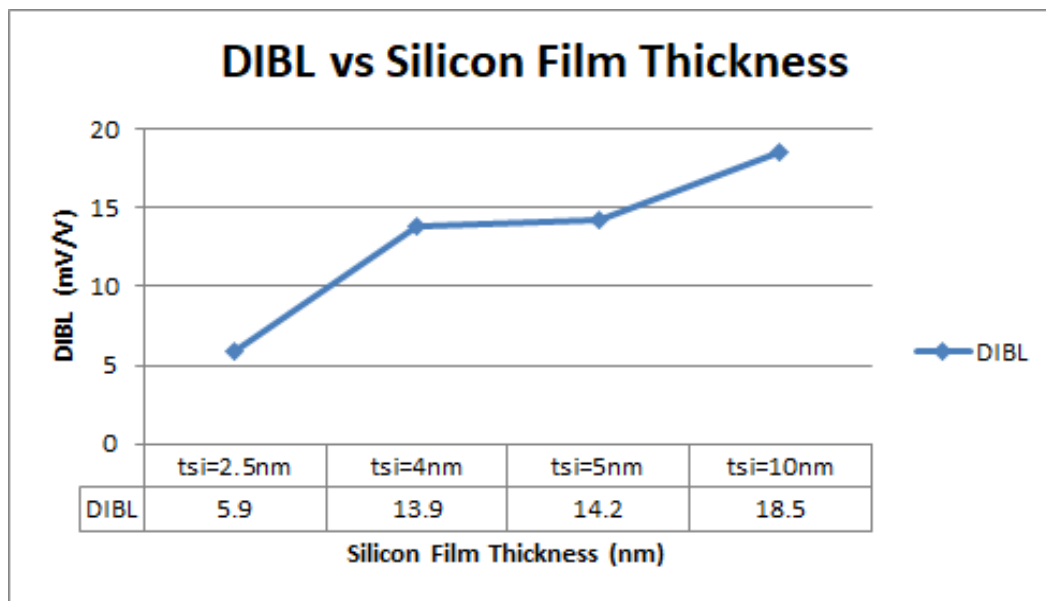
Figure 5.24: DIBL variation at various Silicon film thickness

5.2.5   Impact of Silicon film thickness on Subthreshold Slope

Figure 5.25 shows the plot between the sub-threshold slope and silicon film thickness. It is depicted from the graph that the sub-threshold slope of the Gate All Around MOSFET structure improves as the silicon film thickness is decreased. It is because of the increased threshold voltage and decreased silicon film thickness.
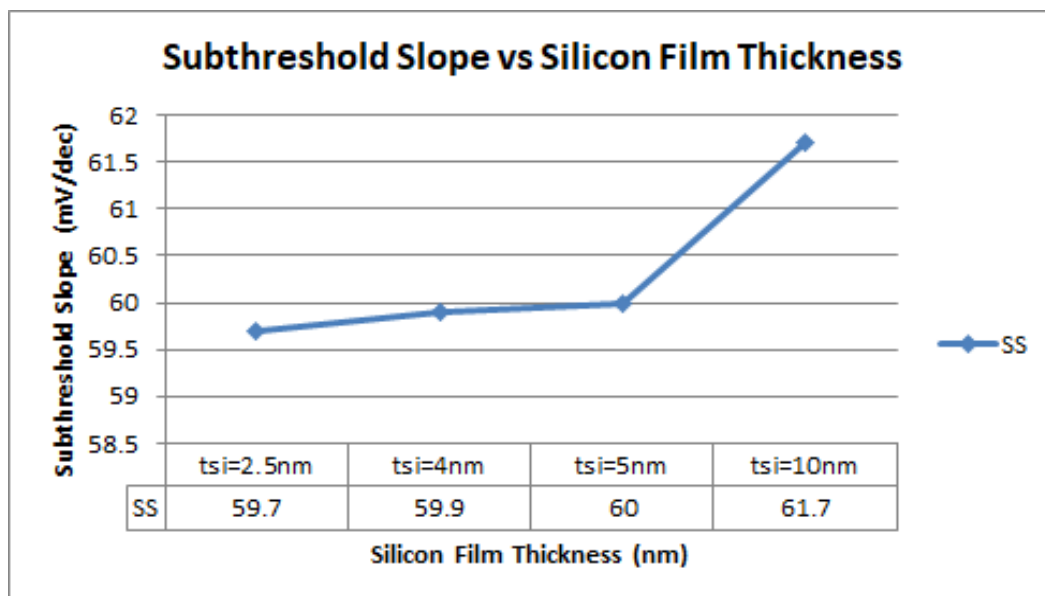
Figure 5.25: Comparison curves of Subthreshold Slope at various Silicon film thicknesses

Table 5.2 contains the extracted parameter values after simulation.

Table 5.2: Silicon film thickness simulation results

t_{si} (nm)	I_{on} (A)	I_{off} (A)	(I_{on}/I_{off})	V_{th} (V)	DIBL (mV/V)
2.5	5.29e-6	3.71e-14	1.42e8	0.36	5.8
4.0	9.64e-6	1.76e-13	5.46e7	0.33	13.9
5.0	2.39e-5	5.26e-13	4.54e7	0.31	14.2
10.0	8.91e-5	4.81e-12	1.85e7	0.27	18.5

It has been analysed that the device has a higher driving current and leakage current for silicon film thickness is equal to 10nm as compared to film thickness 5nm, 4nm & 2.5nm . But the ratio of I_{on}/I_{off} current increases by decreasing the silicon film thickness ranging from 10nm to 2.5nm. It is also observed cylindrical GAA MOSFET having a film thickness of 2.5nm has a higher threshold voltage and lower DIBL effect. So in this way, we can advance the device performance by reducing the leakage current with the variation of film thickness in the sub-threshold regime.

5.3   CONCLUSION

In this chapter, the influence of Gate electrode work function engineering to adjust the threshold voltage in the Gate All Around MOSFET is presented. Since metal gates can resist high dielectric Gate dielectric materials, which is very important for incessant shrinkage of the device structure, therefore its use for Gate All Around MOSFET has been proposed. During the simulation, it is observed that threshold voltage can be changed to a desired value by varying the metal gate work function of the Gate All Around MOSFET can manufacture devices that may have to lessen short channel effects and hence higher device performance. By properly adjusting the Metal gate work function the short channel effects can be fairly managed and enhanced. Also, an improvement in DIBL, SS, OFF state current and ON/OFF current ratio has been observed as the Metal Gate work function increases however the ON current has

to sacrifice some extend. Further, the effect of silicon film thickness tsi on device performance has been observed. It has been observed that threshold voltage rises with an increase in silicon film thickness and therefore an improvement has been observed in the Sub-threshold current. Also as the silicon film thickness reduces, an improvement in DIBL, SS, ON/OFF current ratio has been observed. Since the simulated device has better SS, therefore the device can be used for low power high-frequency circuit applications.

CHAPTER 6

DUAL MATERIAL GATE ALL AROUND MOSFET

The performance improvement in traditional bulk Si MOSFETs with deca-nanometer technology nodes seems to be severely restricted by increased short-channel effects (SCEs). ITRS claims that integrating new technology is essential for deep sub-micron CMOS devices. Using gate-material engineering, non-conventional MOSFET device structure improves carrier transport efficiency, increases transconductance, and suppresses SCEs by altering the electric field pattern and surface potential along the channel [135]. By solving the Poisson equation, a 2D analytical model for the Dual Material Surrounding Gate MOSFET has been proposed and simulated using the ATLAS TCAD device simulator. The SCEs for device architectures with the same dimensions in DMSG and SMSG have been compared.

Since the device parameters like ON/OFF current ratio, Threshold voltage, OFF state leakage current and Sub-threshold Swing (SS) are very much dependent on device geometry like channel thickness, channel length and gate work function. In this chapter, an analysis of the performance dependency of Dual material on device geometry variation has been introduced.

Dual material Gate All Around MOSFET uses two materials having different work-functions for gate electrode [136]. The work function of gate material near to source is taken higher than the work function of gate material near the drain end. These type of architectures prevents any changes in the drain bias. It additionally shifts the electrostatic potential profile to a step-like profile along the length of the channel. Due to the abrupt increase of electric field and velocity of charge carriers close to the gate materials interface, thereby the driving capabilities of the device can be enhanced [137].

Under the gate terminal, a peak electric field is acquired, thus reducing the electric field at the drain end and increasing the electrostatic gate control over the channel. Hence, the gate transport efficiency can be increased in this manner [138, 139].

6.1 DEVICE STRUCTURE

The structure of the dual material Cylindrical Gate All Around MOSFET (CGAA) MOSFET structure after the simulation is shown in Figure 6.1. This structure is
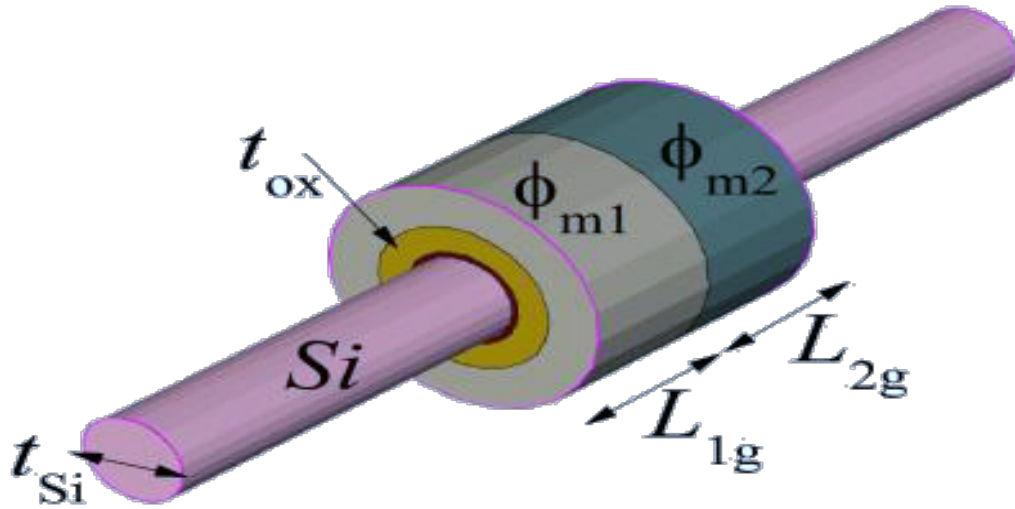
Figure 6.1: Schematic diagram of 45nm dual material Gate All Around MOSFET

virtually fabricated and simulated using the ATLAS SILVACO tool. The radial directions are supposed to be along the radius and the lateral direction is along the *z*-axis of the cylinder. The metal gate work functions $\phi_{m1} = 4.4\text{eV}$ and $\phi_{m2} = 4.6\text{eV}$ for Dual material are considered.

6.2 DRAIN CURRENT CHARACTERISTICS

6.2.1 Transfer Characteristics

The transfer characteristics of a dual material gate all around MOSFET (DMGAA-MOSFET) exhibit unique characteristics compared to traditional MOSFETs [140]. Figure 6.2 shows the transfer characteristics of 45nm dual-material GAA MOSFET in linear mode. These characteristics are obtained at fixed drain voltages of 0.1V and 1V. At each drain voltage V_D, the gate voltage V_{GS} is varied from 0 to 1V. The drain current is plotted along with the y-axis and gate voltage along the x-axis.
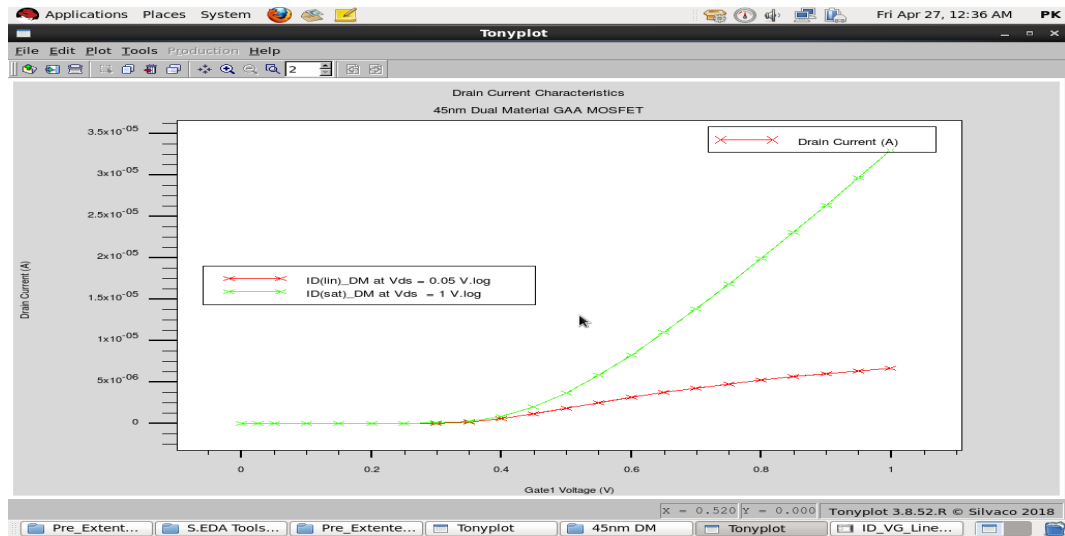
Figure 6.2: Drain current characteristics in Linear mode

The logarithmic scale is used to better visualize the wide range of drain currents that a MOSFET can exhibit. In the linear mode, the drain current can span several orders of magnitude, and using a logarithmic scale helps in compressing this wide range into a more manageable plot. Figure 6.3 shows the transfer characteristics where drain current is plotted along the y-axis in logarithm scale.
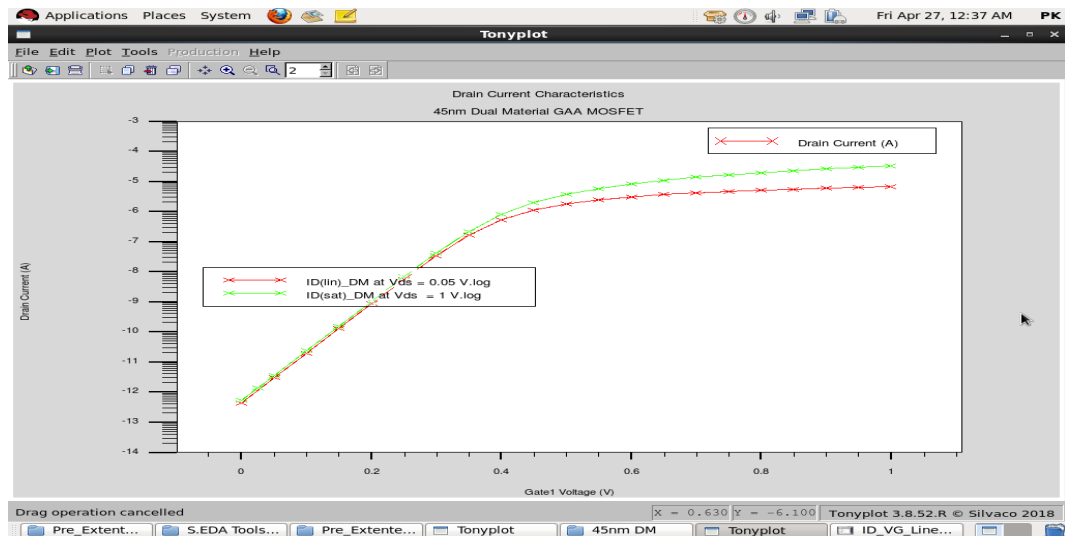
Figure 6.3: Drain current characteristics in Logarithmic mode

6.2.2   Trans-conductance

Trans-conductance (gm) is a parameter used to measure the performance of MOSFET. It is defined as the ratio of the variation in drain current to the change in gate voltage over an arbitrary slight interval on drain current versus gate voltage curve.

Figure 6.4 shows the trans-conductance versus gate voltage curve.
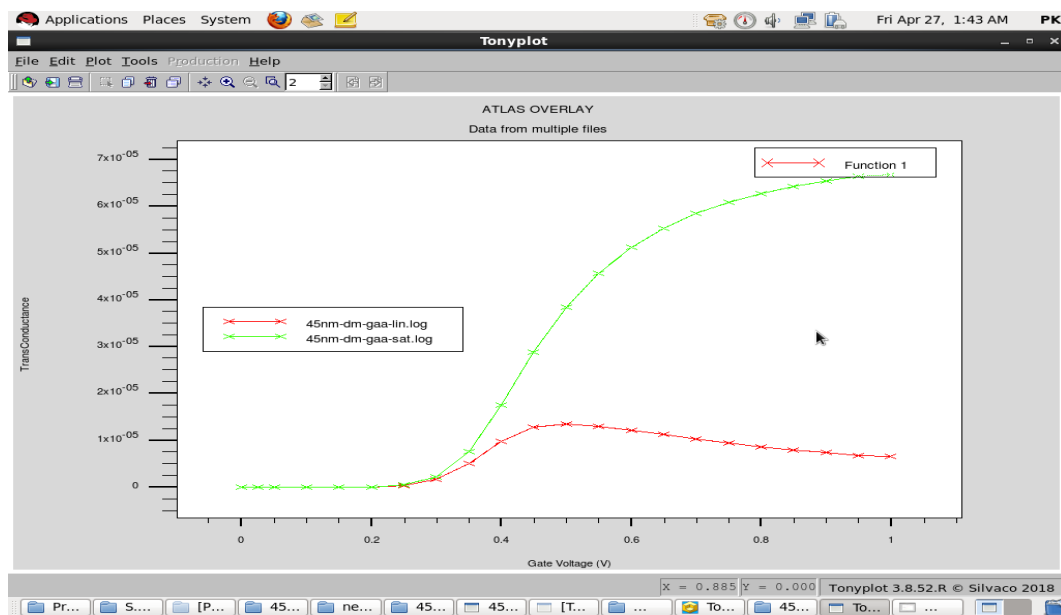
Figure 6.4: Trans-conductance versus gate voltage plot

6.3 COMPARISON OF SINGLE GATE AND MULTI GATE DEVICES

Figure 6.5 shows the comparison plot of drain current versus gate voltage of dual material and single material Gate All Around MOSFET.
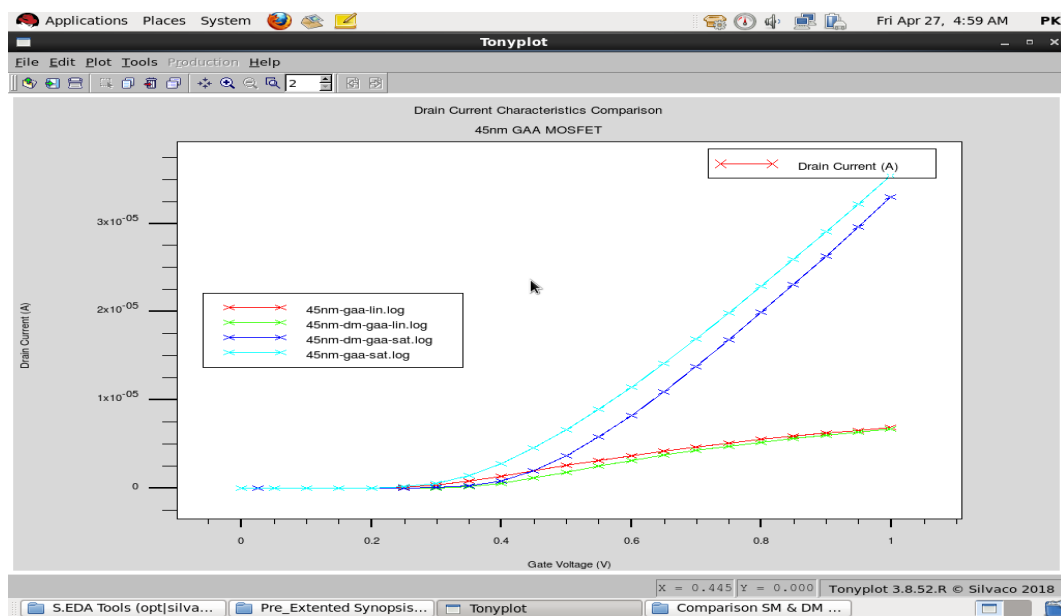
Figure 6.5: Drain current comparison of single and dual material GAA MOSFET in linear mode

The simulations are done for V_{DS}=0.1V and V_{DS}=1V. The gate voltage V_{GS} varied from 0V to 1V. Figure 6.6 shows the transfer characteristics of single and dual materials gate with drain current in logarithmic mode. The improvement in OFF current is noticeable in the Dual material Gate All Around MOSFET.
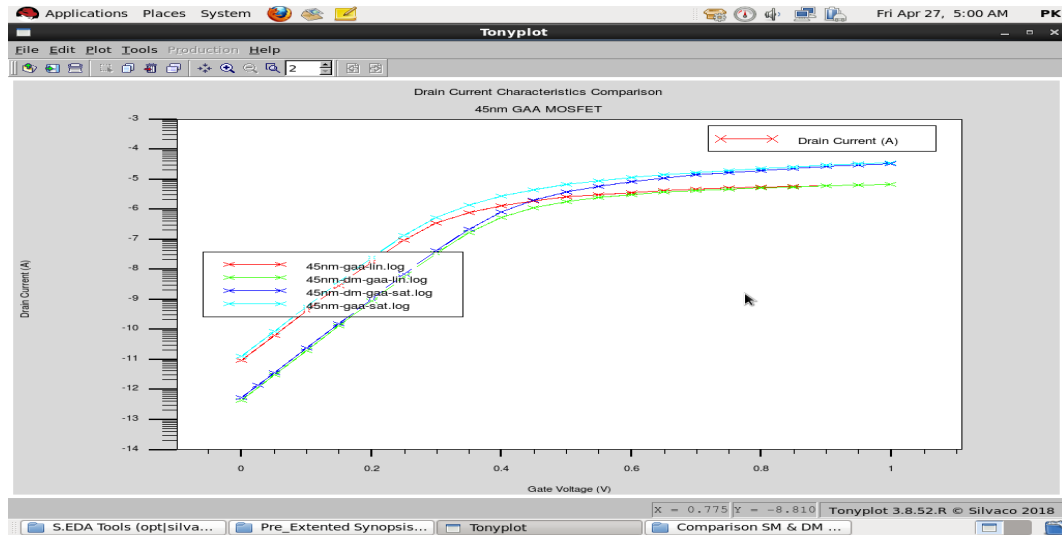
Figure 6.6: Drain current comparison of single and Dual material GAA MOSFET in Logarithmic mode

Figure 6.7 depicts the ON current characteristics in Dual material gate design as compared to the single material gate. The effect of step potential profile due to the introduction of Dual material gate design in device leads to enhanced ON current.
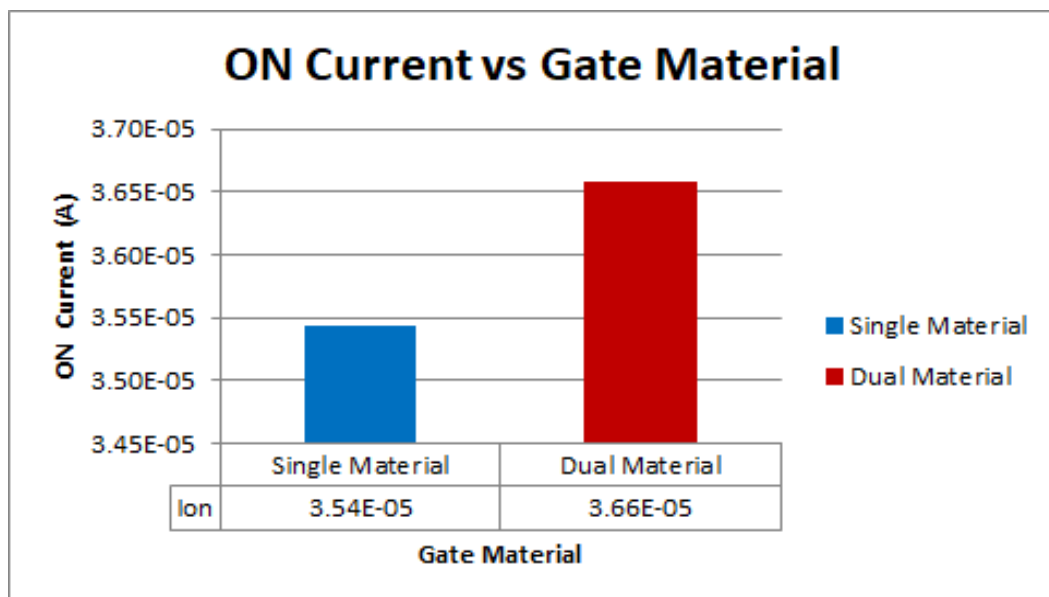
Figure 6.7: Drain current comparison of Single and Dual material GAA MOSFET

Figure 6.8 shows leakage current is significantly improved in OFF current in Dual material as compared to the Single material gate because no leakage path is available apart from gate.
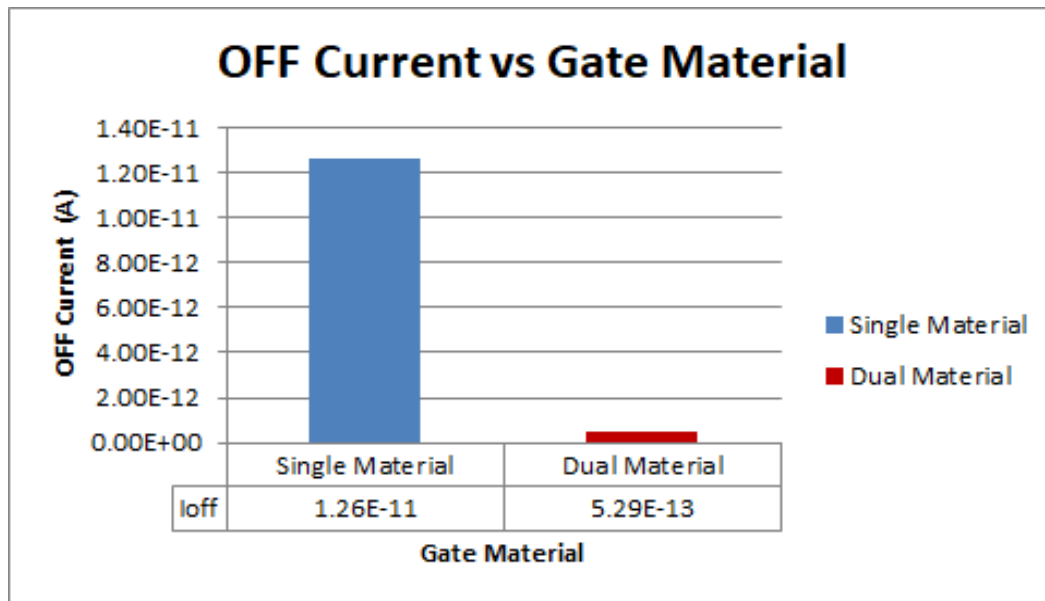
Figure 6.8: Leakage current comparison of Single and Dual material GAA MOSFET

Figure 6.9 shows that the ON/OFF current ratio also improves significantly in dual material as compared to the single material gate which is a required parameter for fast switching appliances.
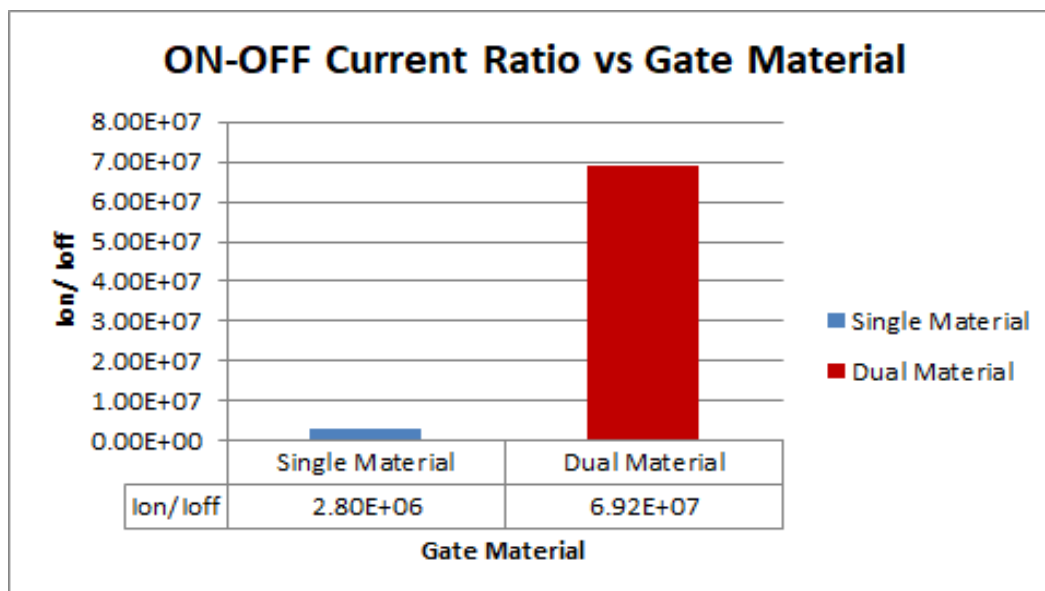
Figure 6.9: ON/OFF current ratio comparison of Single and Dual material GAA MOSFET

Figure 6.10 depicts the sub-threshold slope of the dual material gate which almost the same as a single material gate and offers a sub-threshold swing in limits which helps to improve device scaling performance.
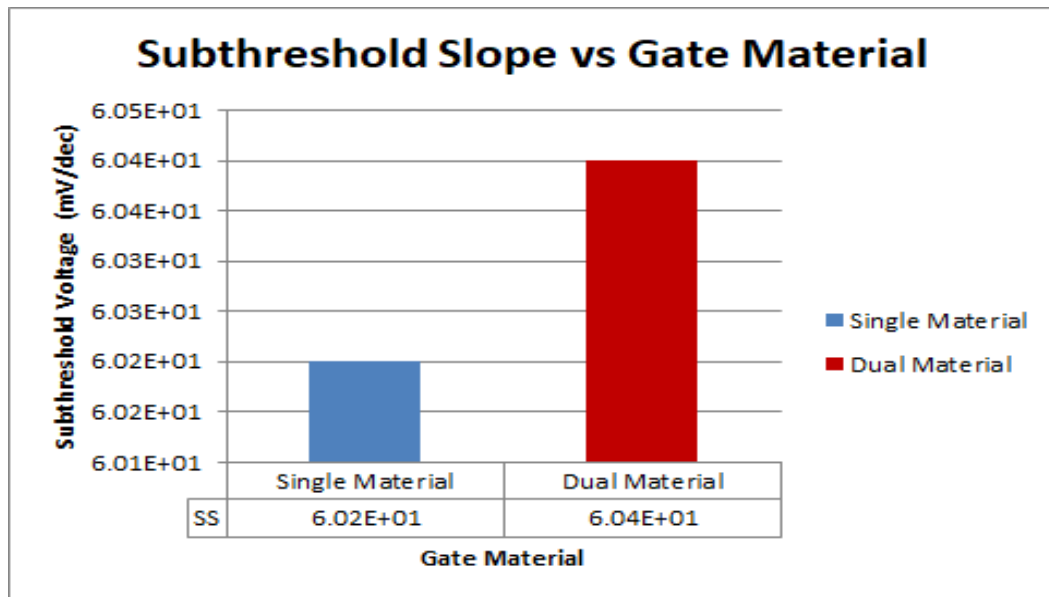
Figure 6.10: Subthreshold Swing comparison of Single and Dual material GAA MOSFET

Figure 6.11 indicates that the greater work function improves the threshold voltage in dual material compared to the single material gate which is required to minimize OFF state current and enhance the sub-threshold characteristics of the device.
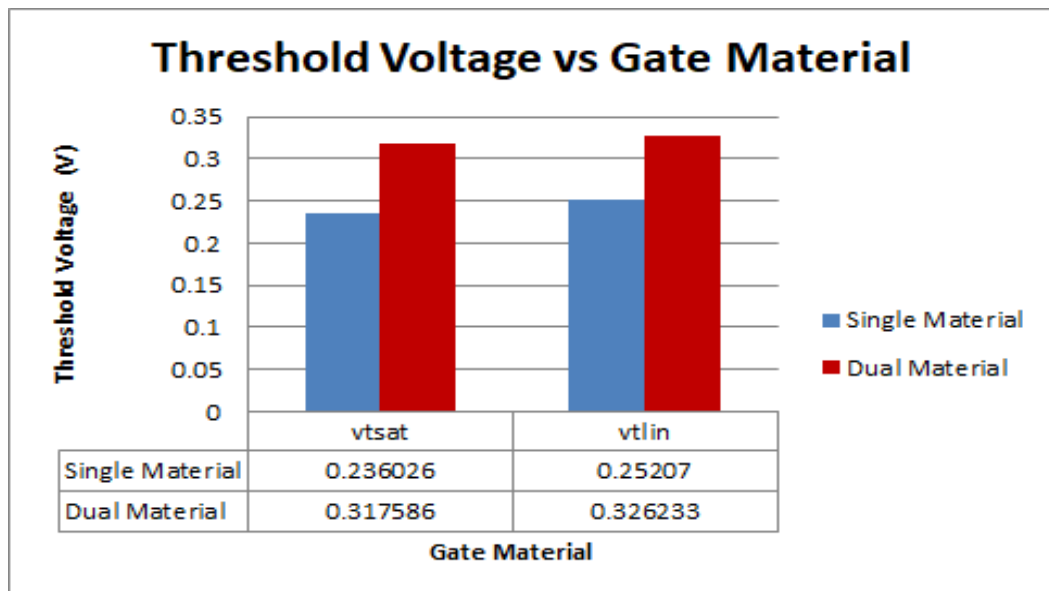
Figure 6.11: Threshold voltage comparison of Single and Dual material GAA MOSFET

The Dual-material device outperforms over single material owing to the greater control of gate over a channel, enhanced screening of the threshold voltage defining

region from the change of the drain bias induced by the step pattern in the potential profile. Beyond the saturation voltage metal gate near the drain end absorb any extra variations from potential at the drain, hence reducing the DIBL.

The Dual-material GAA has lesser DIBL as compared to Single material GAA as shown in Figure 6.12.
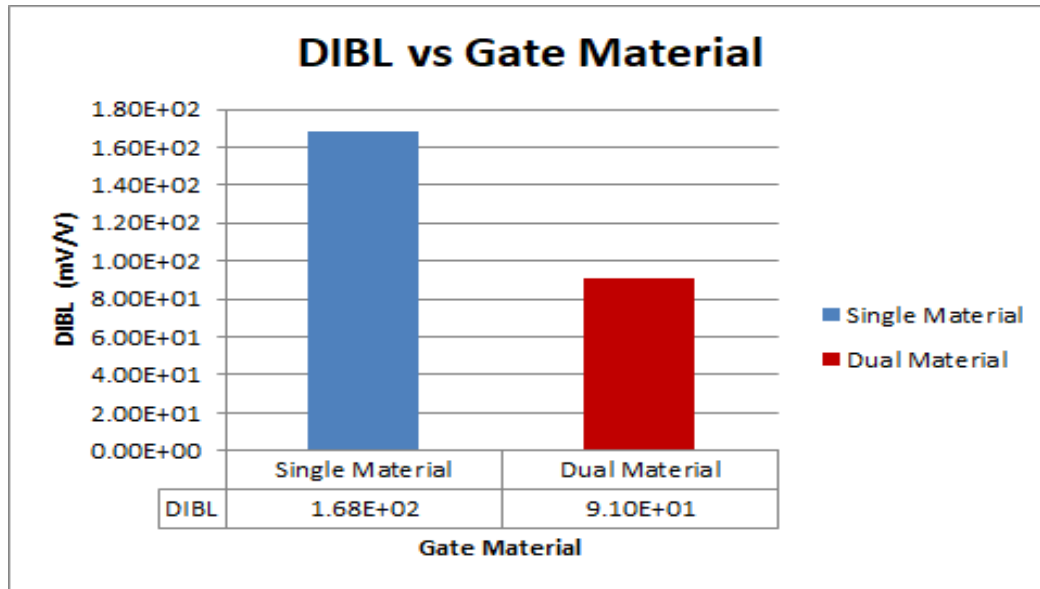
Figure 6.12: DIBL comparison of Single and Dual material GAA MOSFET

6.4   CONCLUSION

In this chapter, the potential analysis has been performed for Dual material Gate All Around MOSFET. Then the dual material Gate All Around MOSFET is compared with single material Gate All Around MOSFET based on various parameters i.e drain current, sub-threshold current, ON/OFF current ratio and DIBL. It has been observed that Dual material GAA is a improved device with OFF current of 5.29e-13 A and ON/OFF ratio of 6.29e7 suitable for low power applications.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSIONS

The primary objective of this research work is to perform the mathematical modeling and optimization of Gate All Around MOSFET. The design, simulation and improvement of the device depends upon the input parameters defined during the simulation. After the input parameter definition and simulation using Technology computer-aided design (TCAD) tool, the estimation and improvement of the output device and process parameters are performed. This research is intended to discover the difficulties faced due to device dimension scaling and find out the different techniques to reduce the short channel effects. The major contributions of this research are as follows:

- The performance of the single gate, double gate and FinFETs are deteriorating day by day due to scaling which results in to increase in short channel effects. In this research work, a device called GAA (Gate All Around MOSFET) is designed, virtually fabricated and simulated using an ATLAS device simulator to reduce short channel effects.

- The main purpose of this research is to replace the existing devices with GAA due to their excellent performance. Then, in order to enhance sub-threshold leakage current, DIBL, Sub-threshold Slope, and ON/OFF current ratio, the parameters Gate oxide thickness, Silicon film thickness, and Work-function are adjusted.

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- The analytical modeling of the device is carried out and then the device is simulated using a device simulator having similar parameters defined during the analytical modeling. After that, the simulated results are compared with the analytical results. The simulated values of I_{on} current, I_{off} current and I_{on}/I_{off} current ratio are also compared with the existing literature. The potential distribution is also estimated analytically in this thesis and the various parameters such as electron current density, conduction band, valence band profiles and donor concentration are obtained.

- In this thesis, the drain characteristics of 45nm and 30nm Cylindrical Gate All Around (CGAA) are explored and the performance evaluations are carried out with an extensive device simulator. Various electrical characteristics have been extracted i.e. Drain current (I_{on}), Sub-threshold current (I_{off}), DIBL, Sub-threshold slope, I_{on}/I_{off} ratio after the simulation of the device in ATLAS. Also, the output (I_D–V_{DS}) and transfer (I_D–V_{GS}) characteristics of GAA MOSFET have been plotted. As a result, it has been observed that with the increase of drain to source voltage and gate to source voltage, the drain current increases. The simulated value of various parameters is compared with the literature review as well as analytical values. The drain current is significantly improved when the device approaches the nanowire.

- The potential analysis has been performed for Dual material Gate All Around MOSFET. Then Dual material Gate All Around MOSFET is compared with single material Gate All Around MOSFET based on various parameters i.e Drain current, Sub-threshold current, ON/OFF current ratio and DIBL. It has been observed that dual material GAA is a better device for low power applications.

- The influence of Gate work function engineering to adjust the threshold voltage in the Gate All Around MOSFET is presented. Since metal gates can resist high dielectric gate materials, which is very important for incessant shrinkage of the device structure, therefore its use for Gate All Around MOSFET has been proposed. During the simulation, it has been observed that threshold voltage can be adjusted to the desired value by varying the metal gate work function of the gate electrode. The short short channel effects has been reduced by effectively adjusting the metal gate work function. Also, an improvement in DIBL, Sub-threshold slope, OFF state current and ON/OFF current ratio has been observed by increasing the metal gate work function in order to sacrifice the ON current.

- Also as the silicon film thickness reduces, an improvement in DIBL, Sub-threshold slope, ON/OFF current ratio has been observed. Since the simulated device has better Sub-threshold slope, therefore the device can be used for low power high-frequency circuit applications.

7.2 FUTURE SCOPE

The current study presented in this dissertation has demonstrated the potential to minimize short-channel effects. Also, the efficiency of the device can be enhanced by selecting suitable device dimensions with appropriate materials. Single material and dual material GAA devices have been designed and simulated so that the device can be used for low-power applications. The research can be further extended in the below directions:

- Quantum mechanical effects play an essential role in exploring the transport issues as the device dimensions shrink to the sub-nanometer regime. It is important to correlate a self consistently quantum transport equation with Poisson's equation to obtain these effects accurately.

- To study and explore NEGF (Non Equilibrium Green's Function) formalism for transport issues in the nanometer regime.

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LIST OF PUBLICATIONS

Sr. No.	Title of Paper	Journal	No.	Volume & Issue	Year	Pages
1.	Performance Investigation of dual-halo dual-dielectric Triple material Surrounding Gate MOSFET with high-k dielectrics for low power applications	Journal of Semi-conductor Technology and Science	2233-4866	Vol. 20, No.3	2020	297-304
2.	Effect of variation of gate work-Function on electrical characteristics of lightly doped PMOSFET	International Journal of Future Generation Communication and Networking	2207-9645	Vol. 12, No.4,	2019	17-26
3.	Investigate sub-threshold performance measures of cylindrical Gate All Around MOSFET at sub-nanometer regime	Journal on Embedded systems, i-manager Publications	2320-2335	Vol. 6, No.1,	2017	1-5
4.	Investigation and dependency analysis of silicon film thickness on performance of Surrounding Gate MOSFET at sub-threshold regime	Journal of VLSI Design Tools & Technology	2321-6492	Vol. 8, No. 2,	2018	49-54
5.	Design, Analysis and simulation of 30nm Cylindrical Gate All Around MOSFET	International Journal of Advanced Research in Computer and Communication Engineering	2278-1021	Vol. 5, No. 10,	2016	358-360

6.	Study the effect of various parameters on threshold voltage of 180nm NMOS using SILVACO TCAD TOOL	National Conference, RSTTMI,YMCAUST, Faridabad			2016	
7.	Low Power High Speed One Bit Hybrid Full Adder	International Conference, SDREM, YMCAUST, Faridabad			2016	

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