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Total Pages : 3

009604

May 2023

B.Tech. (EIC) VI SEMESTER

VLSI Design (EIEL-611)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) Why resistance is not used as load element for NMOS logic inverter? (1.5)

(b) What is the threshold voltage of the MOSFET? (1.5)

(c) How a depletion mode MOSFET is different from enhancement mode MOSFET? (1.5)

(d) How MOSFET can work as a switch? (1.5)

(e) What is latch up issues in CMOS circuits? (1.5)

(f) Why non-ideal effects are observed mainly in short channel devices? (1.5)

(g) What do you mean by noise margins? (1.5)

(h) What is the requirement of circuit layout in VLSI designing? (1.5)

(i) Why do we use "standard unit of capacitance" in VLSI circuits? (1.5)

(j) What is CMOS Pseudo MOS logic? (1.5)

PART–B

2. (a) What do you mean by VLSI? Explain VLSI Design flow using suitable diagram. (7.5)

   (b) What is MOSFET? Explain the operation of basic MOS transistor in all the region of operations. (7.5)

3. (a) Describe the p-well process for fabrication of the "CMOS INVERTER" with the sketches of all the steps. (7.5)

   (b) Draw and explain the VTC characteristics of NMOS inverter. What is BiCMOS inverter? How BiCMOS inverter is different from CMOS inverter? (7.5)

4. (a) Draw the schematic and stick diagram for $Z=A\overline{B}+C\overline{D}$ using CMOS combinational logic designs. (7.5)

   (b) Explain the different types power dissipation occurring in CMOS circuits in detail. (7.5)

5. (a) What is dynamic logic circuits? Why these circuits are used? What is the major issues which can occurs in these dynamic logic circuits? How these issues can be overcome using Domino logic circuits? (7.5)

   (b) What is scaling of the MOSFET circuits? Explain different kinds of scaling for these MOSFET based circuits and also discuss the advantages and limitations of scaling. (7.5)

6. (a) Discuss the design of CMOS parity generator. (7.5)

   (b) Explain in detail the different second order effects occurring in MOSFET using clear diagram. (7.5)

7. Explain

   (a) Concept of sheet capacitance in VLSI circuits. (5)

   (b) Lambda based design rules for layout preparation. (5)

   (c) Design half adder using transmission gates. (5)
