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Total Pages : 3

017302

January 2023

B.Tech. EEIoT - III SEMESTER

Digital Electronics (EEN-301)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Assume relevant data, if required.*

PART–A

1. (a) Implement Ex-or gate using NOR gate. (1.5)

(b) Convert the following :

$(10.2B)_{16} = (\ )_8$ (1.5)

(c) How decoder is different from Demultiplexer? (1.5)

(d) Implement an AND gate using mux. (1.5)

(e) What is the difference between Toggling and Race around condition. (1.5)

(f) Convert the JK flip flop to SR flip flop. (1.5)

(g) Draw the circuit of tristate logic. (1.5)

(h) Explain the switching mode operation of PN junction. (1.5)

(i) Draw sample and Hold circuit. (1.5)

(j) List the specifications of a digital to analog converter. (1.5)

PART–B

2. (a) Minimize the following using Quine Mcluskey method : $f(A,B,C,D) = \Sigma m(0,1,2,3,5,7,8,10,12,13,15)$ (10)

(b) The seven bit hamming code received is 001 0001. Assume that even parity has been used, check is it correct or not. If not find the correct code. (5)

3. (a) Design a Gray to BCD code converter using **one 1:16 Demultiplexer** and NAND gates. (5)

(b) Design a nine's complement circuit using one 4-bit Adder and Logic gates. (10)

4. (a) Design a MOD-8 synchronous UP counter using JK flip-flop. (12)

(b) Explain the working of Master-slave J-K flip flop. (3)

5. (a) Explain the functionality of TTL NAND Gate using circuit diagram. (5)

(b) What are the features and limitations of Emitter coupled logic? (5)

(c) Interface CMOS with TTL. (5)

6. (a) A 12 bit DAC has full scale analog voltage of 5 V. Determine step size, percentage resolution and analog output voltage to input of 1101 0000 0001. (5)

(b) Explain the working of parallel-comparator A/D converters. (10)

7. (a) Design the circuit for Half-Adder using ROM. (5)

(b) Describe the difference between PAL and PLA. (10)