Roll No.

Total Pages : 3

311104

January 2023

BCA 1st SEMESTER Logical Organization of Computer-I (BCA-17-104)

Time : 3 Hours]

[Max. Marks: 75

Instructions :

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- 1. It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.
- 2. Answer any four questions from Part-B in detail.
- 3. Different sub-parts of a question are to be attempted adjacent to each other.
- 4. Use of Scientific calculator is not allowed.

PART-A

(a)	Define the following terms: Bit, Nibble, Byte.	(1.5)
(b)	Explain De Morgan's Law.	(1.5)
(c)	Find the Binary equivalent of (22A.3) ₁₆ .	(1-5)
(d)	Perform 47-36 using 2's complement method.	(1.5)
(e)	Encode the decimal number 37 to gray code.	(1.5)
(f)	Difference between Minterm and Maxterm.	(1.5)
(g)	Explain XOR Gate.	(1.5)
(h)	Why we add Don't care conditions in our Boolean	
	Expression?	(1.5)

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(i)	Design parallel binary adder.	(1.5)

(j) What is AND-OR-INVERT Gate? (1.5)

PART-B

 (a) Explain Floating point representation of number. Represent (625.125)₁₀ using single-precision floating point representation. (10)

(b) Write note on BCD codes. (5)

3. (a) Simplify and Minimize using K-map the following Function (7)

 $F(A, B, C, D) = \Sigma m(0, 2, 5, 7, 8, 10, 13, 15).$

(b) Find out the values of X, Y & Z in following : (8)

 $(523.225)_{10} = (X)_2 = (Y)_8 = (Z)_{16}.$

- 4. Design a circuit with the help of K-map which convert 4bit binary number into Excess-3 code and also write the expression for each binary bit. (15)
- 5. (a) Simplify the following expression using Boolean Algebra : (5)
 - (i) XY + XYZ + X(Y + XY).
 - (ii) C(B + C)(A + B + C).
 - (iii) (AB'(C + BD) + A'B')C.
 - (b) Explain Decoder and also design the circuit for 3 to 8 Decoder. (10)

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- (a) Design and explain the parallel Binary Adder/Subtractor circuit. (10)
 - (b) Difference between Decoder and Encoder. (5)
- 7. (a) What is Multiplexer? Design the circuit for 4*1 Multiplexer. (8)
 - (b) Design a 1-bit magnitude comparator with three outputs: A > B, A < B and A = B. (7)

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