ETS

Roll No. ..... Total Pages : 3

009604

August/September 2022
B.Tech. (EIC) VI SEMESTER
VLSI Design (EIEL-611)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART-A

1. (a) Define threshold voltage in MOSFET. (1.5)

(b) Why MOSFET is symmetrical device? (1.5)

(c) Define Noise margin for symmetrical CMOS inverter. (1.5)

(d) What is stick diagram? (1.5)

(e) What are micron rules? (1.5)

(f) What are advantages of pseudo NMOS logic? (1.5)

(g) What is pass transistor logic? (1.5)

(h) What is the need of scaling? (1.5)

(i) What is dynamic MOS logic? (1.5)

(j) What are the advantages of BiCMOS? (1.5)

PART-B

2. (a) Derive Ids *versus* Vds Relationship for NMOS transistor and explain the operation in linear region and saturation region. (10)

(b) What is substrate bias effect in MOSFET? Explain. (5)

3. (a) Explain the dynamic operation of Symmetrical CMOS inverter and find the relationship for propagation delay. (8)

(b) What is latch problem in CMOS? What are the methods to avoid this? (7)

4. (a) What is the role of design rules in VLSI design. Discuss lambda based design rules for NMOS design. (8)

(b) Explain the CMOS domino logic and its advantages. (7)

5. (a) Explain the switching power consumption in CMOS inverter and on which factor it depends. (8)

(b) Design XOR and XNOR gate with transmission gate approach. (7)

6. (a) Design a Two input NAND gate and two input NOR gate with standard CMOS. (8)

(b) Explain the pseudo. NMOS inverter and explain the VTC. (7)

7. Write notes on :

(a) Scaling in MOS devices. (7.5)

(b) Design issues in VLSI. (7.5)