80742

B.Tech. 4th Semester
DIGITAL ELECTRONICS (EC-232-C)

Time : 3 Hours]   [Max. Marks : 75

Instructions :

(i) It is compulsory to answer the questions of Part-1. Limit your answers within 20-40 word in this part.

(ii) Answer any four questions from Part-2 in detail.

(iii) Different parts of the same question are to be attempted adjacent to each other.

(iv) Assume suitable standard data wherever required, if not given.

PART–1

1. (a) Subtract the binary number 00110111 from 10110001
(1.5)

(b) Perform the operation (23-46) using 2's complement method. (1.5)

(c) What is the difference between a latch and a flip flop? (1.5)

(d) Differentiate between PLA and PAL. (1.5)

(e) Why do we use ASCII code? (1.5)

(f) Compare SRAM and DRAM. (1.5)

(g) Differentiate between edge triggering and level triggering. (1.5)

(h) What is the difference between a combinational and a sequential circuit ? (1.5)

(i) Explain why a synchronous counter is faster than the ripple counter? (1.5)

(j) What are error detecting codes? (1.5)

PART–2

2. (a) Simplify the logic function using Quine-McCluskey method (8)

$F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$.

(b) Design and implement a Mod-6 synchronous counter using D-Flip Flop. (7)

3. (a) Simplify the logic expression using K-map (7)

$F(A,B,C,D,E) = \Sigma m(0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27, 29, 31)$.

(b) Design and implement a 2-bit comparator using suitable logic gates. (5)

(c) Find the maximum frequency of a clock pulse at which the 4-bit ripple counter operates reliably. Assume delay of the flip flop is 40 ns and the pulse width of strobe signal is 25 ns. (3)

4. (a) What is meant by a Universal shift register? Design a 4-bit universal shift register with the help of a function table. (6)

(b) Design a BCD to Excess-3 converter (5)

(c) Implement $(A + C)(A + \bar{D})(A + B + \bar{C})$ using NOR gates only. (4)

5. (a) Design a combinational circuit for a common cathode display BCD to 7 segment code converter. (8)

(b) With a neat circuit diagram explain the operation of a Dual slope A/D converter. (7)

6. (a) Explain full adder and design a full adder circuit using 3 to 8 decoder and two OR gates. (5)

(b) What is race around condition? With the help of truth table, explain the working of J-K Master-slave flip flop. (5)

(c) Simplify the expression: (5)

(i) $A = XY + \overline{XZ} + X\overline{Y}Z(XY + Z)$

(ii) $Y = (A + B)(\overline{A} + C)(B + C)$.

7. (a) Implement following Boolean function using 8 : 1 multiplexer. (5)

$F(A, B, C, D) = \Sigma m(2, 3, 5, 7, 8, 9, 12, 13, 14, 15)$.

(b) Write short notes on : (5 × 2)

(i) PLA and PAL.

(ii) TTL circuit with totem pole output.

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