YMCAUST -May 2019

B.Tech, V|SEMESTER

MOSICs & Technology (ECE-308), Scheme 2010

Time: 3 Hours **Max. Marks:60**

Instructions:
1. *It is compulsory to answer all the questions (2 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART -A

Q1 (a) Draw equivalent circuit for MOSFET. (2)

(b) Explain what is the need of oxidation in MOS devices? (2)

(c) What are the various causes of power dissipation in CMOS circuit. (2)

(d) Implement F= A . (B + C) using CMOS design style. (2)

(e) Define constant voltage scaling of MOS device. (2)

(f) Explain MOS transistor transconductance. (2)

(g) Differentiate between CMOS and BiCMOS inverters. (2)

(h) Explain annealing. What are the requirements of annealing process? (2)

(i) Explain the working of MOS in saturation region of operation with neat sketch. (2)

(j) Using CMOS combinational logic design draw circuit for Xorgate? (2)

Q2 (a) Discuss the n-well process of fabricating the CMOS transistor with suitable sketches. (5)

(b) What is NMOS inverter? Explain the different form of pull up. Determine the pull up to pull down ratio for an NMOS inverter driven by another NMOS inverter. (5)

Q3 (a) What are the various causes of power dissipation in CMOS circuit?Explain how thresholdvoltage of MOS transistor affects drain current with the help of necessaryequations. (5)

(b) Derive the expression for threshold voltage of MOS transistor and explain the significance of different parameters present in the equation. (5)

Q4 (a) Design left/right shift serial/parallel register using CMOS logic. (5)

(b) What is photolithography? What are the various steps for carrying out photolithography process? (5)

Q5 (a) Explain the following terms briefly: (5)

(i) Punch through

(ii) Impact Ionization

(b) Explain with an example, why NAND gates are preferred over NOR gates for Implementing combinational logic function in CMOS.Implement F= A.(D+E) + BC using CMOS design style. (5)

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Q6 (a) What is ion implantation? What are its advantages over diffusion process? Also explain why annealing is necessary after implantation? (5)

(b) Consider an n channel MOSFET with following characteristics: t ox =10nm, μ n =520cm 2 /V-s, (W/L)=8,VTn =+0.70V,V gsn =2V V dsn =2V. Find the drain source current. (5)

Q7 Write short noes on: (10)

(i) Advantages of CMOS over nMOS

(ii) DC characteristic of CMOS inverter

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