Roll No. .....

Total Pages : 4

307401

May, 2019

B.Tech. IV SEMESTER

Digital Electronics (ELPC-401)

Time : 3 Hours

Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART–A

1. (a) What is the function of clock in sequential circuits? (1.5)

(b) What is race around condition? (1.5)

(c) Differentiate between ripple and synchronous counter. (1.5)

(d) Which logic family has highest speed of operation? (1.5)

(e) What is the significance of ASCII code? (1.5)

(f) What are the various types of Read only memories? (1.5)

(g) Differentiate between edge triggering and level triggering. (1.5)

(h) What is the resolution in volts of a 10-bit D/A Converter whose full scale output is 5V ? (1.5)

(i) Perform (20-42) using 2's complement method. (1.5)

(j) What are various types of error correcting codes? (1.5)

PART–B

2. (a) Design and implement a Mod-5 up/down counter using JK-Flip Flop. (7)

(b) Simplify the logic function using Quine-McCluskey method.

$F(A, B, C, D) = \Sigma m(1, 2, 3, 8, 9)$ (5)

(c) Convert the following :

$(2A6)_{16} = (?)_{10}$

$(10011.101)_2 = (?)_{16}$

$(221)_{10} = (?)_8$. (3)

3. (a) Write short notes on PLA and PAL. (8)

(b) Simplify the logic expression using K-map $F(A, B, C, D) = \Sigma m\ (0, 1, 5, 7, 10, 14) + d(2, 4)$. (4)

(c) Implement $Y(A, B, C) = \Sigma m(0, 4, 5, 7)$ using 3 : 8 line decoder. (3)

4. (a) Discuss in detail the different types of shift registers. (5)

(b) Convert S-R to T Flip Flop. (5)

(c) Implement $(A + C)(A + D)(A + B + C)$ using NOR gates only. (5)

5. (a) Design a combinational circuit for a common anode display BCD to 7 segment code converter. (8)

(b) With a neat circuit diagram explain the operation of a Successive Approximation type A/D converter. (7)

6. (a) Explain the following terms:

(i) Fan in.

(ii) Fan out.

(iii) Propagation delay.

(iv) Tristate logic.

(v) Hold time. (5)

(b) With the help of truth table, explain the working of J-K Master-slave flip flop. (5)

(c) Simplify the following expression :

(i) $Z = A[B + C(AB + AC)]$

(ii) $Z = \overline{A}\,\overline{B}\,C + \overline{(A + B + C)} + \overline{A}\,\overline{B}\,\overline{C}\,D$. . (5)

7. (a) Explain the working of a basic TTL NAND gate with a neat diagram. Explain the following output configurations :

(i) Open collector output.

(ii) Totem pole output. (8)

(b) Implement following Boolean function using 8 : 1 multiplexer.

$F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 5, 8, 9, 15)$ (7)
