YMCAUST -MAY 2019

B.Tech, VI SEMESTER

Digital System Design(E-302), Scheme 2010

Time: 3 Hours | **Max. Marks:60**

Instructions:
1. *It is compulsory to answer all the questions (2 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART –A

Q1 (a) What is the difference between function and procedure? (2)

(b) Explain with example that how a component can be made more general using generics. (2)

(c) Explain with example assert statement. (2)

(d) What is the need of configuration? Explain with an example (2)

(e) Write VHDL code for 2-bit comparator using any modelling style. (2)

(f) Write a data flow style of VHDL code for 8-bit unsigned multiplier. (2)

(g) Explain the need of resolution function. (2)

(h) What are signal attributes? Explain with example. (2)

(i) What is sensitivity list in behavioural and data flow modelling? (2)

(j) Implement 2-bit magnitude comparator using PLA. (2)

PART –B

Q2 (a) What aredifferent abstraction levels to describe any system? Describe the role of VHDL in these different levels. How HDL is different from other programming languages. (5)

(b) What is library clause and why it is used? Write a VHDL package that provides overload function for plus operator that enables the operation A<= B+C+3, where A, B, C are bit vectors. (5)

Q3 (a) Write behavioral VHDL code that represents a modulo-12 up counter with synchronous reset. (5)

(b) Write a data flow description of a system that has three 1-bit inputs a(1),a(2) and a(3) and 1 bit output b where LSB input is a(1).Further b is 1 only when a(1),a(2),a(3)=1,3,6 and 7 otherwise b is 0. Derive a minimized Boolean function of the system and write data flow description. (5)

Q4 (a) Design a combinational circuit using a ROM. The circuit accepts a 3 bit number andgenerates an output binary number equal to the square of the input number. (5)

(b) Discuss the concept of multiple signal assignment of a same signal in dataflow. (5)

P. T. O.

Explain resolution function with respect to above statement with appropriate example.

Q5 (a) Write a VHDL program for detecting the number of '1' in an 8 bit-vector. If even output is '0' & odd output ='1'. (5)

(b) Design and write VHDL code for a universal shift register that can shift both left-to-right and right-to-left directions and it has parallel load capability. (5)

Q6 (a) Discuss inertial & transport delay with waveforms. Consider the assignments below, executed at simulation time 100 ns, form the driver for signal S: (5)

S <= 8 after 20 ns, 2 after 40 ns, 5 after 65 ns, 10 after 100 ns;

S <= reject 55 ns inertial 5 after 90 ns;

(b) Write VHDL code for finding factorial of number using while and for loop. (5)

Q7 Differentiate the following with suitable examples: (10)

(i) Next and exit statements

(ii) Different data classes

(iii) Sequential and concurrent statements

(iv) Array and record data types

(v) Simulation and synthesis

****