University Roll No:

J.C. BOSE UNIVERSITY OF SCIENCE & TECHNOLOGY, YMCA FARIDABAD

B.TECH EXAMINATION (Under CBS) (Scheme 2010)

SUBJECT: ANALOG ELECTRONICS (E-211)

Time: 3hrs **M.Marks: 60**

Note: Attempt total five questions. Part-I (Q1) is compulsory. Part-II contains six questions. Attempt any four questions from part-II.

PART-I

Q1. (a) Why inductor filter is more suitable for low value of load resistance and capacitor filter is suitable for large value of load resistance? (2)

(b) Explain why FET is termed as voltage controlled device? (2)

(c) Why the width of the base region of a transistor is kept very small compared to other regions? (2)

(d) Why the Q point should be in the middle of active region? (2)

(e) Prove that $g_{b'c} = h_{re} g_{b'e}$ (2)

(f) Define ac drain resistance and transconductance of FET. (2)

(g) A power supply X delivers 10V dc with a ripple of 0.5 volts rms while the power supply Y delivers 25V dc with a ripple of 1mV rms. Which is better power supply? (2)

(h) Define α and β, also find relation between α and β. (2)

(i) Why fixed biased circuit is not commonly used? (2)

(j) What is the effect of temperature on P-N junction diode? (2)

PART-II

Q2 (a) Draw the circuit diagram of bridge rectifier and explain its working. Also determine an expression for average current, rms current, rectification efficiency and PIV. (5)

(b) Draw the circuit diagram of full wave centre tap rectifier with shunt capacitor filter. Explain the operation with waveform and also obtain ripple factor for full wave centre tap rectifier with shunt capacitor filter. (5)

Q3 (a) Sketch the output characteristics of Common base amplifier. Clearly indicate the cut off, active and saturation regions and also explain it. (5)

(b) A common emitter amplifier uses a voltage source having internal resistance R_s=800Ω and the load resistance R_l=1000Ω. The h parameters are h_{ie} =1kΩ, h_{re} = $2x10^{-4}$, h_{fe}=50, h_{oe}=25μA/V. Calculate the current gain (Ai), input impedance (Zi), and voltage gain (Av). (5)

Q4 (a) Draw the circuit of self biased CE amplifier using diode compensation for Ico. Describe how bias compensation is achieved? (5)

(b) Design self bias circuit for CE amplifier having β =99 and S=5. The other values are V_{CE} =6V, V_{RE}=5.5V, V_{CC}=15V, R_C=2.5kΩ and V_{BE} = 0.3V (5)

Q5(a) Draw the structure of N channel FET and explain its operation. Also draw its V-I characteristics. Define pinch off voltage and mark it on the characteristics. (5)

(b) Draw hybrid Π model for common emitter amplifier. Also determine the short circuit current gain at high frequency. (5)

Q6 (a) Draw circuit diagram of a common source FET amplifier. With the help of a small signal equivalent circuit analyze the amplifier for voltage gain. (5)

(b)Write short note on IC voltage regulator. (5)

Q7. Explain the following:

(a) BJT shunt Regulator (3)

(b) FET as VVR (3)

(c) Clamper circuits (4)