Sr. No.....

Dec 2018

B.Tech. III SEMESTER

Analog Electronics (EC-211-C)

Time: 3 Hours	Max. Marks:75

Instructions:
1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART -A

Q1 (a) Differentiate between BJT and FET. (1.5)

(b) What is peak detector? How does it work? (1.5)

(c) Explain the term "thermal runaway" in transistor? (1.5)

(d) Explain the significance of ripple factor. (1.5)

(e) Why fixed bias circuits are not commonly used? (1.5)

(f) Why the Q point is established in the middle of active region? (1.5)

(g) What is Pinch off voltage for FET? Explain using characteristics curve. (1.5)

(h) Explain why JFET is termed as voltage controlled device? (1.5)

(i) Enlist the distinguished features of regulated power supply? (1.5)

(j) What is the meaning of unipolar device and bipolar device? (1.5)

PART -B

Q2 (a) Deduce collector current, draw and explain input and output characteristics in Common emitter configuration of transistor. (7.5)

(b) Enumerate the various requirements for biasing a circuit. Analyze the voltage divider biasing circuit. (7.5)

Q3 (a) What is Full wave rectifier? Construct a full wave bridge rectifier using diode and calculate peak inverse voltage, dc output current, rms current and ripple factor. (7.5)

(b) Discuss the importance of filter circuits for a rectifier. Explain the working of half wave rectifier with shunt capacitor filter. (4)

(c) Determine the value of emitter current and collector current of a transistor having $\alpha_{dc}=0.98$ and collector to base leakage current $I_{CBO}=4\mu A$ and base current as $50\mu A$. (3.5)

Q4 (a) Draw the equivalent small signal model for CC configuration of a transistor (7.5)

amplifier using h-parameter and also find current gain, input resistance, voltage gain and output impedance.

(b) State and prove Miller's theorem. (4)

(c) Explain FET as VVR. (3.5)

Q5 (a) Draw the hybrid pi-model of common emitter transistor model. Find transconductance (g_m) and input conductance using hybrid pi-model for the same. (7.5)

(b) Draw the small signal equivalent model for source follower configuration for JFET amplifier also deduce the input impedance, output impedance and voltage gain of the circuit. (7.5)

Q6 (a) Discuss the discrete transistor voltage regulator. What are their advantage and disadvantages compared to IC voltage regulator? (5)

(b) Construct and explain the working of voltage multiplier circuit using diode and capacitor. (5)

(c) Draw circuit for self biased CE amplifier using thermistor and sensistor compensation. Explain in each circuit how bias compensation is achieved (5)

Q7 (a) Draw and explain drain characteristics (with and without external bias) and transfer characteristics of the JFETs. (7.5)

(b) For an N-channel JFET I_{DSS}=8.7mA, V_P= -3V, V_{GS}= -1V. Find the value of I_D, g_m, and g_{mo}. (7.5)

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