

Roll No.

Total Pages : 5

322301

December, 2019

M.Tech. (VLSI) - III SEMESTER

VLSI Interconnect (MVLE304)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Data Sheet for 180 nm and 130 nm technology node must be provided.*

PART - A

1. (a) Define the term Repeater? (1.5)
- (b) How many types of interconnects are possible in Literature? Define each of them. (1.5)
- (c) Define the transmission line model used in SPICE. (1.5)

- (d) Define scaling mechanism for Gate and interconnects. (1.5)
- (e) VLSI interconnect can be modelled using three topologies using RC ladder, pi-network, T-network. From these three topologies which is considered as a best technique and why? (1.5)
- (f) What is the difference between Elmore and Sakurai delay model? (1.5)
- (g) How the area capacitance, fringe, lateral capacitances are related to each other provide mathematical formulation for each? (1.5)
- (h) How the inductance of an interconnect line can be controlled? (1.5)
- (i) How the speed of a VLSI interconnects can be enhanced? (1.5)
- (j) What is the difference between Lumped and distributed networks? (1.5)

PART - B

2. (a) Interconnect data :

(a) 0.18 μm 5-layer aluminum process :

$\rho = 2.7 \mu\Omega\text{-cm}$; Metals 1-4, $T = 0.5 \mu\text{m}$, $H = 0.5 \mu\text{m}$,

$W_{\min} = 0.3 \mu\text{m}$; and Metal 5, $T = 1 \mu\text{m}$, $H = 0.5 \mu\text{m}$,

$W_{\min} = 0.4 \mu\text{m}$

(b) 0.13 μm , 8-layer copper process :

$$\rho = 1.7 \mu\Omega\text{-cm; Metals 1-6, } T = 0.4 \mu\text{m, } H = 0.5 \mu\text{m,}$$
$$W_{\min} = 0.2 \mu\text{m; and Metals 7-8, } T = 0.8 \mu\text{m,}$$
$$H = 0.5 \mu\text{m, } W_{\min} = 0.4 \mu\text{m}$$

Interconnect data is provided in part (a) and (b) : write significant conclusions from this data about interconnect technology on observation. (10)

(b) Using the data of part (a) of Q. No. 02, calculate the resistance (R_{sq})

for Al-Metals 1-4(Layers)

Al-Metal -5 (Layer)

Cu-Metals 1-6 (Layer)

Cu-Metals 7-8 (Layer) (5)

3. (a) Compare the resistance of a 20 mm Metal 5 wire in 0.18 μm technology with a 20 mm Metal 8 wire in 0.13 μm technology (a non-scaled wire). Use the information/interconnect data provided in the Q. No 2(a). Compute the delay for each wire assuming an ideal source and a wire capacitance of $C_{\text{int}} - 0.1 \text{ fF}/\mu\text{m}$. (8)

(b) Compare the resistance of a 20 mm Metal 5 wire in 0.18 μm technology with a 14 mm Metal 8 wire in 0.13 μm technology (a scaled wire). Use the information/interconnect data provided in Q. No. 2 (a). Compute the delay for each wire assuming that the wire capacitance is $C_{\text{int}} = 0.1 \text{ fF}/\mu\text{m}$. (7)

4. Two adjacent Metal 5 wires in 0.18 μm technology is spaced out from 4λ to 40λ in 4λ increments. Plot the capacitance per unit length of these wires as a function of spacing, assuming that they are shielded above and below. Use minimum width dimensions for the wire. (15)

5. Wires can be placed into short, medium, long, and very long categories. Establish rules of thumb for a Metal 5 wire in 0.18 μm technology that quantify each of these categories based on the following definitions:

1. Short wires do not require any resistance or capacitance calculations if they contribute less than 5% to the delay. What is the maximum short wire length?
2. Medium wires must include capacitance in the delay calculation, but do not require any resistance information. What is the maximum medium wire length?

3. Long wires require both resistance and capacitance information but do not require buffer insertion. What length of wire can remain unbuffered?
4. Very long wires require buffer insertion. (15)
6. Derive a mathematical formulation for total delay in case of long wires driven by a CMOS inverter of Length 'L' and 'N' buffers are inserted at a regular interval. And to find the optimal value of 'N' and 'M' for long interconnects, whereas N is number of buffers inserted and M is size of each buffer inserted. (15)
7. (a) Define low swing techniques applied in interconnect applications. Further explain about current mode interconnect technique, how it is different from voltage mode technique? (5)
- (b) Define capacitive/crosstalk noise with suitable example. (05)
- (c) Analytical Power expressions for: Dynamic Power, Static Power, Short circuit Power Dissipation in CMOS ICs. (05)
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USEFUL DESIGN PARAMETERS (simplified)

Name	Symbol	0.18 μ m		0.13 μ m		Units
		NMOS	PMOS	NMOS	PMOS	
Channel Length (rounded for convenience)	L	200nm	200nm	100nm	100nm	nm
Supply Voltage	V _{DD}	1.8	1.8	1.2	1.2	V
Oxide Thickness	t _{ox}	35	35	22	22	Å
Oxide Capacitance	C _{ox}	1.0	1.0	1.6	1.6	μ F/cm ²
Threshold Voltage	V _{TO}	0.5	-0.5	0.4	-0.4	V
Body-effect term	γ	0.3	0.3	0.2	0.2	V ^{1/2}
Fermi Potential	2 ϕ_F	0.84	0.84	0.88	0.88	V
Junction Capacitance	C _{jo}	1.6	1.6	1.6	1.6	fF/ μ m ²
Coefficient						
Built-in Junction Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	-
Nominal Mobility (low vertical field)	μ_o	540	180	540	180	cm ² /V-s
Effective Mobility (high vertical field)	μ_e	270	70	270	70	cm ² /V-s
Critical Field	E _c	6 × 10 ⁴	24 × 10 ⁴	6 × 10 ⁴	24 × 10 ⁴	V/cm
Critical Field × L	E _c L	1.2	4.8	0.6	2.4	V
Effective Resistance	R _{eff}	12.5	30	12.5	30	k Ω /f

Name	Symbol	Value	Units
Gate Capacitance Coefficient	C _g	2	fF/ μ m
Self Capacitance Coefficient	C _{eff}	1	fF/ μ m
Wire Capacitance Coefficient	C _w	0.1-0.25	fF/ μ m
Al Wire Resistance	R _{Al}	25-60	m Ω /f
Cu Wire Resistance	R _{Cu}	20-40	m Ω /f
Wire Inductance	L _{eff}	40-50	pH/ μ m

USEFUL PHYSICAL AND MATERIAL CONSTANTS

Name	Symbol	Value	Units
Electron Charge	q	1.6×10^{-19}	C
Boltzmann's Constant	k	1.38×10^{-23}	J/°K
Room Temperature	T	300	°K (27°C)
Thermal Voltage	$V_{th}=kT/q$	26	mV (at 27°C)
Dielectric Constant of Vacuum	ϵ_0	8.85×10^{-14}	F/cm
Dielectric Constant of Silicon	ϵ_{si}	$11.7\epsilon_0$	F/cm
Dielectric Constant of SiO ₂	ϵ_{ox}	$3.97\epsilon_0$	F/cm
Intrinsic Carrier Concentration	n_i	1.45×10^{10}	/cm ³ (at 27°C)
Carrier Saturation Velocity In Silicon	v_{sat}	8×10^6	cm/s
Aluminum Resistivity	ρ_{Al}	2.7	$\mu\Omega\text{-cm}$
Copper Resistivity	ρ_{Cu}	1.7	$\mu\Omega\text{-cm}$
Tungsten Resistivity	ρ_W	5.5	$\mu\Omega\text{-cm}$

ENGINEERING SCALE FACTORS

G	giga	10^9
M	mega	10^6
k	kilo	10^3
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

METER CONVERSION FACTORS

$$1 \mu\text{m} = 10^{-4} \text{ cm} = 10^{-6} \text{ m}$$

$$1 \text{ m} = 10^2 \text{ cm} = 10^6 \mu\text{m}$$

$$0.1 \mu\text{m} = 100 \text{ nm}$$

$$1 \text{ \AA} = 10^{-8} \text{ cm} = 10^{-10} \text{ m}$$