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Total Pages : 6

322104

December, 2019

M.Tech. (VLSI) - I SEMESTER

Device Modelling for Circuit Simulation (MVLE110)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Data sheet is required for 130 nm and 180 nm technology node.*

PART - A

1. (a) Write the spice command for ac, dc, transient, noise, temp analysis with full syntax. (1.5)

(b) Transconductance of MOSFET is greater in linear or in saturation region, justify your statement. (1.5)

(c) How many types of SPICE MOS models are available in literature, write the full name of at least five models? (1.5)

(d) How many types of power dissipation are possible in CMOS integrated circuits, write the mathematical formulation for each? (1.5)

(e) Explain series and parallel operation of pass transistor logic circuit. (1.5)

(f) Write the mathematical model for sub-threshold current equation in a MOSFET. (1.5)

(g) Define the MOSFET capacitance Model in different region of operation. (1.5)

(h) Define logical effort and how it helps in improving the performance of integrated circuits. (1.5)

(i) How channel length modulation is measured? (1.5)

(j) What is the need for modelling a system? (1.5)

PART - B

2. The circuit of Fig. 1 shows different implementations of an inverter whose output is connected to a capacitor, do all calculation in 0.13 μm. (15)

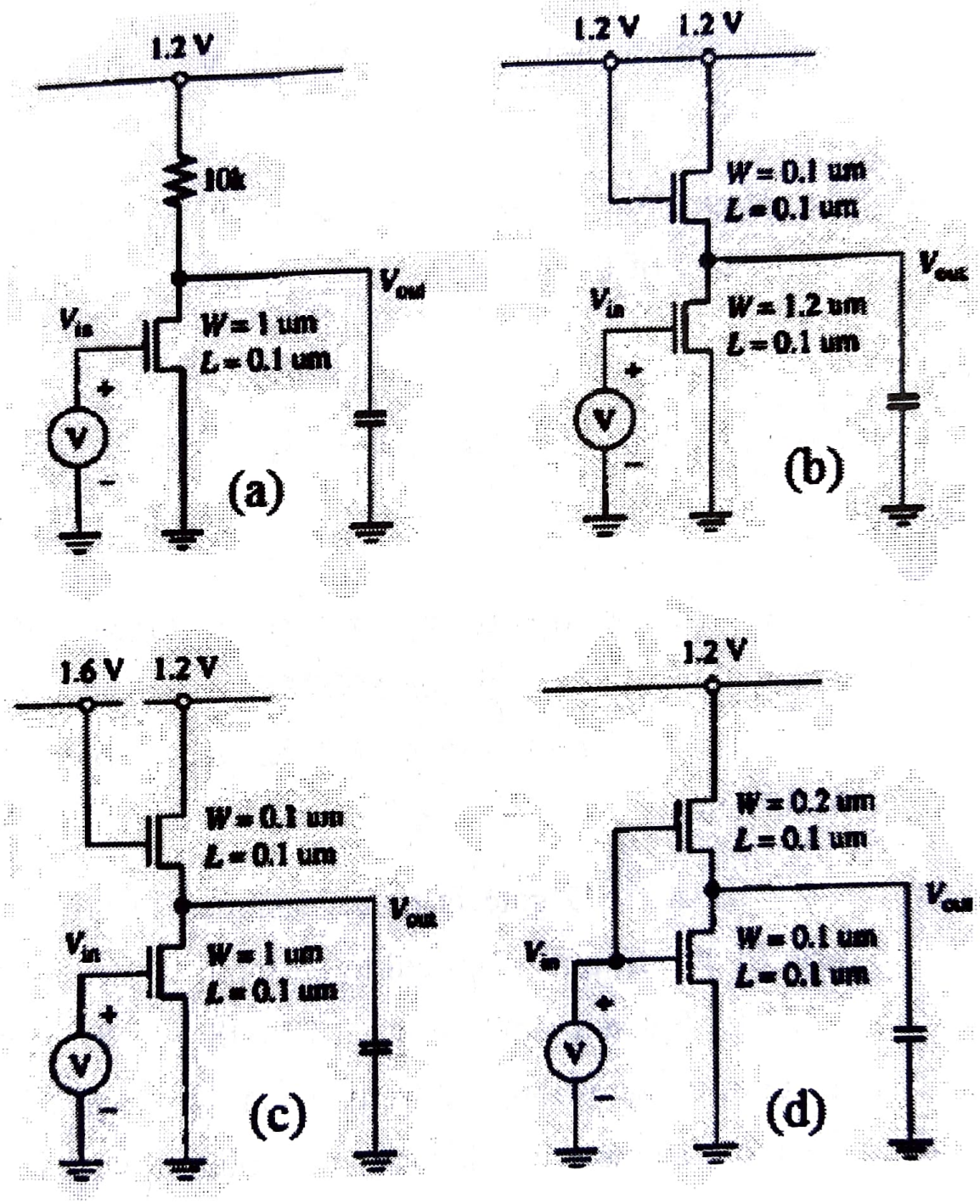

Fig. 1

(a) Which one of the circuits consumes static power when the input is high?

(b) Which one of the above circuits consumes static power when the input is low?

(c) V_{OH} of which circuit(s) is 1.2 V? (d) V_{OL} of which circuit(s) is 0 V?

(d) The proper functionality of which circuit(s) depends on the size of the device?

3. Calculate V_{OH} and V_{OL} of the circuits in Fig. 1 (15)

4. (a) Derive the formulation for transconductance with and without body bias for MOSFET. And address the merits of both the case with mathematical justification. (8)

(b) An 8 input AND gate is to be designed to drive a load of 200 fF but is limited to an input capacitance of 20 fF. Since a single 8 input CMOS NAND gate is out of the question, choose two configurations that are more suitable and identify the solution with the fastest speed. (7)

5. In each of the circuit of Fig. 2, determine the self capacitance at the output assuming step changes at the input shown. (15)

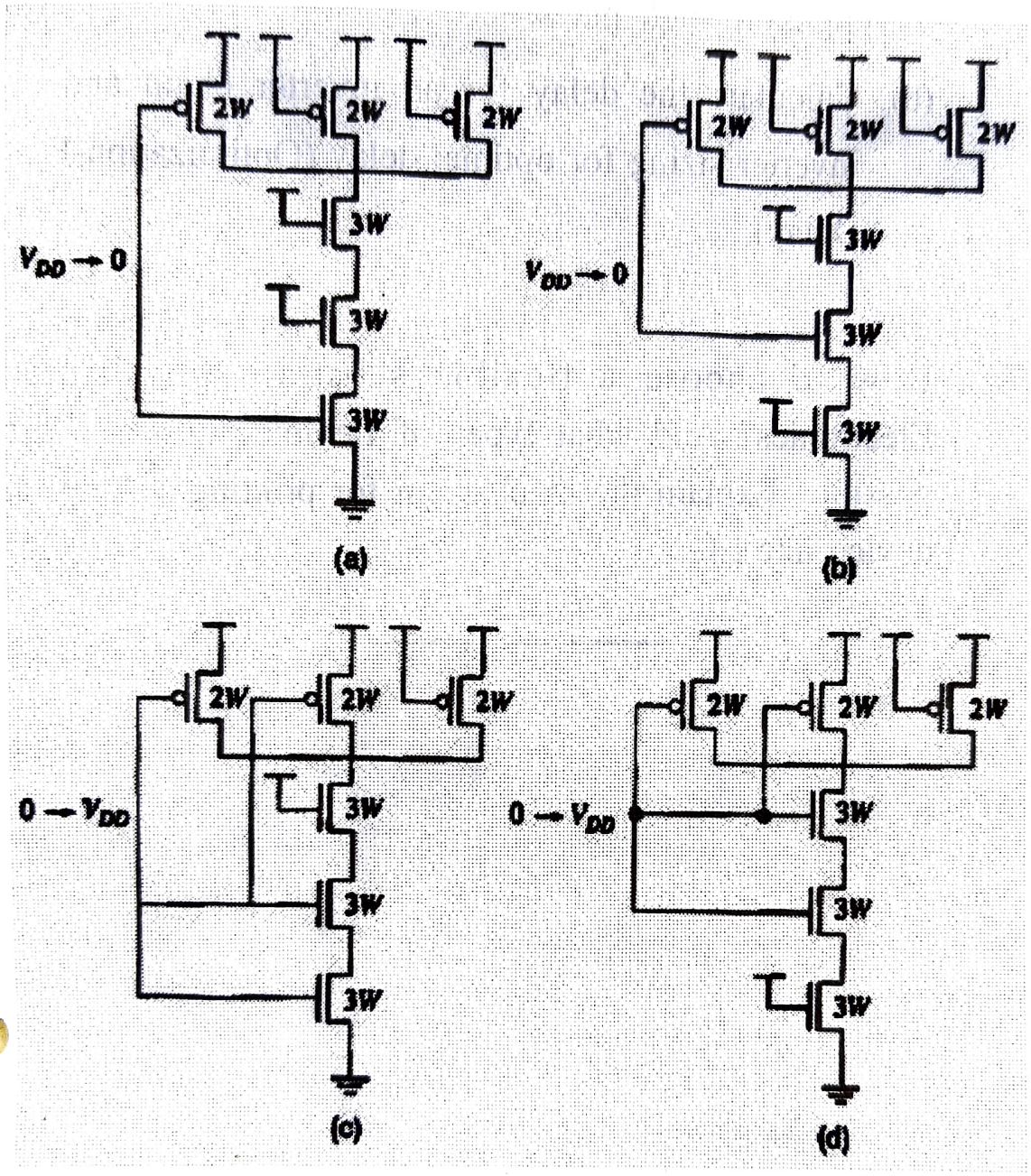

Fig. 2

6. (a) Derive the value of logic effort for gates with equal delays for inverter, NAND and NOR and calculate the same for multi input case for one, two and three input signal to logic gates. (8)

(b) Calculate the delay for an inverter chain and do inverter sizing for optimal delay (Optimization-FO4 Delay). (7)

7. How to choose a flexible substrate for Printed Electronics? And what types of flexible substrates are possible. Explain the mechanism for printing a simplest device like LED. (15)

USEFUL PHYSICAL AND MATERIAL CONSTANTS

Name	Symbol	Value	Units
Electron Charge	q	1.6×10^{-19}	C
Boltzmann's Constant	k	1.38×10^{-23}	J/°K
Room Temperature	T	300	°K (27°C)
Thermal Voltage	$V_{th}=kT/q$	26	mV (at 27°C)
Dielectric Constant of Vacuum	ϵ_0	8.85×10^{-14}	F/cm
Dielectric Constant of Silicon	ϵ_{si}	$11.7\epsilon_0$	F/cm
Dielectric Constant of SiO_2	ϵ_{ox}	$3.97\epsilon_0$	F/cm
Intrinsic Carrier Concentration	n_i	1.45×10^{10}	/cm^3 (at 27°C)
Carrier Saturation Velocity In Silicon	v_{sat}	8×10^6	cm/s
Aluminum Resistivity	ρ_{Al}	2.7	μΩ–cm
Copper Resistivity	ρ_{Cu}	1.7	μΩ–cm
Tungsten Resistivity	ρ_W	5.5	μΩ–cm

ENGINEERING SCALE FACTORS

G	giga	10^9
M	mega	10^6
k	kilo	10^3
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

METER CONVERSION FACTORS

$1\ \mu m = 10^{-4}\ cm = 10^{-6}\ m$
$1\ m = 10^2\ cm = 10^6\ \mu m$
$0.1\ \mu m = 100\ nm$
$1 Å = 10^{-8} cm = 10^{-10} m$

For 322104(MVLE 110)

USEFUL DESIGN PARAMETERS (simplified)

		0.18µm		0.13µm		
Name	Symbol	NMOS	PMOS	NMOS	PMOS	Units
Channel Length (rounded for convenience)	L	200nm	200nm	100nm	100nm	nm
Supply Voltage	V_{DD}	1.8	1.8	1.2	1.2	V
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	$\mu F/cm^2$
Threshold Voltage	V_{TO}	0.5	-0.5	0.4	–0.4	V
Body-effect term	γ	0.3	0.3	0.2	0.2	$V^{1/2}$
Fermi Potential	$2\lvert\phi_F\rvert$	0.84	0.84	0.88	0.88	V
Junction Capacitance Coefficient	C_{jo}	1.6	1.6	1.6	1.6	$fF/\mu m^2$
Built-in Junction Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	–
Nominal Mobility (low vertical field)	μ_o	540	180	540	180	$cm^2/V\text{-}s$
Effective Mobility (high vertical field)	μ_e	270	70	270	70	$cm^2/V\text{-}s$
Critical Field	E_c	6×10^4	24×10^4	6×10^4	24×10^4	V/cm
Critical Field x L	E_cL	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	kΩ/□

Name	Symbol	Value	Units
Gate Capacitance Coefficient	C_g	2	fF/µm
Self Capacitance Coefficient	C_{eff}	1	fF/µm
Wire Capacitance Coefficient	C_w	0.1–0.25	fF/µm
Al Wire Resistance	$R_□$	25–60	mΩ/□
Cu Wire Resistance	$R_□$	20–40	mΩ/□
Wire Inductance	L_{eff}	40–50	pH/µm