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322102

December, 2019

M.Tech. I SEMESTER (VLSI)

Microcontrollers and Programmable Digital Signal Processors (MVL102)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART - A

1. (a) What is the difference between Embedded Systems and the System in which RTOS is Running? (1.5)

(b) What do you mean by Interrupt Latency? (1.5)

(c) What are Little Endian and Big Endian Types of Storage? How can you Identify which Type of Allocation a System Follows? (1.5)

(d) What is Watchdog Timer? (1.5)

(e) What is ILP? (1.5)

(f) What is the purpose of pipelining? (1.5)

(g) Why VLIW instructions are not binary compatible? (1.5)

(h) Which are the oscillators supported by LPC? (1.5)

(i) Compare flexibility and performance of FPGA versus DSP. (1.5)

(j) What is the role of link register in ARM? (1.5)

PART - B

2. (a) Explain in brief RTC module in ARM. (7)

(b) How Interrupts are handled in ARM? How external lines interact with NVIC? (8)

3. (a) Draw MAC execution hardware of DSP and show its working. (8)

(b) How is an Nth order FIR Filter is implemented in DSP? (7)

4. (a) Draw reset and wake up timer for LPC and show its working. (8)

(b) How is the SPI protocol implemented in LPC? (7)

5. (a) What is 3 stage and 5 stage pipelining in ARM? (7)

(b) What is the function of these instructions in ARM : UMULL, BL, LDRSH, ADR? (8)

6. (a) Draw schematic of VLIW architecture. What is FU connectivity? (8)

(b) What is circular buffer addressing mode in DSP? What advantages it offers? (7)

7. (a) Enlist Code Composer Studio capabilities and briefly explain. (7)

(b) How branching and subroutine instructions are implemented in ARM? (5)