YMCA UNIVERSITY OF SCIENCE AND TECHNOLOGY, FARIDABAD

M.TECH EXAMINATION (UNDER CBS) DEC-2017

Digital VLSI Design (E 16 V 603)

Time: 3 hrs **M.Marks:75**

NOTE: PART- A is compulsory and in PART- B, four questions out of six are to be attempted.

PART-A

Q.1(a) How pass transistor logic differ from simple NMOS/PMOS logic? 1.5x10

(b) Derive the expression of threshold voltage for MOS transistor and explain the significance of different parameters in the equation.

(c) Briefly explain the following terms(i) punch through (ii) impact ionization

(d) Justify the statement; "there is no short circuit power dissipation in a static CMOS circuit if dissipation in a static CMOS circuit if Vdd < (Vtn + Vtp)

(e) Derive the expression of rise time and fall time in CMOS inverter.

(f) Why we need scaling and what are its effect in long channel and short channel.

(g) Show how domino CMOS logic gate can be cascaded with static CMOS logic gate also mention limitations for the same.

(h) How one nMOS and one pMOS transistor are combined to behave like an ideal switch?

(i) Why is it necessary to insert a buffer after not more than four pass transistors in cascade?.

(j) What is leakage power dissipation? On what parameters does it depends.

PART-B

Q.2(a) Describe twin tub process for fabrication of the CMOS transistor. What is the latch up problem that arises in bulk CMOS technology? How is it overcome? (7)

(b) Differentiate enhancement mode and depletion mode inverters. What are the key characteristics of MOS dynamic circuits? Explain the basic operation of a 2-phase dynamic circuit?. How 2-phase clocks can be generated using inverters? (8)

Q.3(a) Draw the characteristics curve for NMOS and derive the expression for the drain current for NMOS. What is noise margin? Find out the noise margin from the actual characteristics of the NMOS inverter. (7)

(b) Give the schematic diagram of a Bi-CMOS inverter. Explain its operation. Compare the switching characteristics of a BiCMOS inverter with respect to that for static CMOS for different fan out conditions. (8)

Q.4(a) Consider a process technology for which L_{min}=0.4μm,t_{ox}=0.4 nm, μ_n=450 cm^2/v.s, ε_{ox}=3.45x10^{-11} and v_t=0.7V. (i)Find C_{ox} and k'_n (ii) For a MOS with W/L= 8 μm/0.8 μm, calculate the values of V_{GS} and V_{DSMIN} needed to operate the transistor in the saturation region with a dc current I_D=100 μA. For the same device as (ii)find the value of V_{GS} required to cause the device to operate as a 1000 Ω resistor for very small V_{ds}. (7)

(b) Design a stick diagram using CMOS logic design for the function F(A,B,C)= A+B+BC . (8)

As you move to a new process technology with a scaling factor S = 1.4, how the drain current, power dissipation, power density, delay and energy requirement changes for the constant field scaling?

Q.5(a) What is transmission gate? Why it is preferred over NMOS/PMOS switch? Design 4:1 multiplexer using transmission gates. (7)

(b) Using CMOS combinational logic design draw circuit and stick diagram for two input OR gate find the W/L ratio for each MOS transistor used in the circuit. (8)

Q.6(a) Design a scaled chain of inverters such that the delay time between the logic gate (C g = 100 fF) and a load capacitance 2 pF in minimized. Find out the number of stages and stage ratio. (7)

(b) How do you realize pseudo nMOS logic circuits. Compare its logic circuits. Compare its advantage and disadvantages with respect to standard static CMOS circuits CMOS circuits. (8)

Q.7(a) Discuss the design of CMOS parity generator. (7)

(b) The following parameters are given for an nMOS process: tox 500Å, N A = 1x10^{16}cm-3, ND = 1x10^{20}cm-3, N_{OX} = 2x10^{10}cm-1. (i) Calculate V_t for an unimplanted transistor, (ii) what type and what concentration must be implanted to achieve V_t = +1.5V and V_t = - 2.0V? (8)