Roll No._____

YMCA UNIVERSITY OF SCIENCE AND TECHNOLOGY, FARIDABAD

M. TECH EXAMINATION

VLSI ARCHITECTURE (E-16V 705 A)

Time: 3 hrs M. Marks: 60

Note: Attempt all the questions in part I with brief answers (word limit 20 to 40).
Attempt any four questions from part II.

Part – I (Each Question carry 2 marks)

1. a) What is dynamic scheduling? Discuss various concepts and challenges in ILP.
   b) Explain with justification various hardware support to expose parallelism.
   c) Write about Flynn's classification of computers architecture.
   d) Explain forbidden latencies and initial collision vector.
   e) List out various data dependence with examples.
   f) What is the difference between network diameter and bisection bandwidth?
   g) Explain Admahl's Law. How can communication latency be calculated?
   h) Differentiate between directory based protocol and snooping protocol.
   i) With the help of diagram explain the interior design of processing element.
   j) Explain internal data forwarding by replacing memory access operations with R-T operations.

Part – II (Each Question carry 10 marks)

Q.2 a) Explain dynamic scheduling with an example. How is it beneficial in removing data hazards?

Q.2 b) Characterize the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessors and multicomputer based on their structures, resource sharing and interprocessor communications. Also, explain the difference among UMA, NUMA and COMA and NORMA computers.

Q.3 a) Analyze the data dependences among the following statements in a given program:

S1: LOAD R1,1024
S2: LOADR2,M(10)
S3: ADD R1,R2
S4: STORE M(1024),R1
S5: STORE M(R2),1024

Where R(i) means the content of register Ri and Memory(10) contains 64 initially. Draw a dependence graph to show all the dependences. Are there any resource dependences if only one copy of each functional unit is available in CPU?

Q.3 b) Explain the permutation function of parallel processing. Also define barrel shifter, Mesh and Torus.

Q. 4 a) With the help of functional units and data path explain Superscalar RISC microprocessor.

Q.4 b) Explain need of various components in distributed shared memory architecture. Also discuss various advantages and disadvantages of distributed shared memory over symmetric shared memory

Q.5 a)What is reconfigurable computing? In terms of granularity, what type of reconfigurable architecture does FPGA belong to?

Q.5 b)What is the architecture of FPGA? What is/are the reconfigurable part (s) in FPGA? Explain in brief how do we reconfigure FPGA?

2.6 a) Explain pipeline unit for fixed point multiplication of 8-bit integers using CSA and CPA.
2.6 b) Explain the relationship between integer unit and floating point unit in most processors with scalar and superscalar organizations.

2. 7 Write short notes on:
(i) Grain packaging and scheduling
(ii) Static and Dynamic reconfiguration
(iii) VLIW Architecture