University Roll No._____

YMCA UNIVERSITY OF SCIENCE & TECHNOLOGY, FARIDABAD

M.Tech Examination (Under CBS)

Sub: AVLSI Design (E-16V 602)

Time: 3Hr Max Marks 60

Note:-

1. *There is two parts in the question paper, namely Part-I and Part –II, Part –I is compulsory and in part –II, there is six questions. Out of six, four question to be attempted.*
2. *In part-I there are ten questions, each question of 2 Marks and in Part-II each question is 10 Marks.*
3. *In Case of numerical problems, assume data wherever not provided.*

Part-I (2x10 = 20)

Q.No.1 Short answer type (word limit 20-40 words only).

(a) Define Noise margin and how it is calculated from the graphical characteristics of inverter.
(b) In which technology Intel i3 and i5 processors are fabricated?
(c) Define the analog octagon.
(d) Prove the equivalency between T and pi small signal model for MOSFET.
(e) Explain the operation of C.S amplifier, when the load is (a) resistive load (b) Diode load (c) current source load.
(f) For Common gate configuration calculate its input impedance.
(g) Define Analog IC design flow.
(h) For Wilson current mirror calculate the output resistance.
(i) Compare the BJT and MOSFET based source follower configurations.
(j) Explain how technology scaling impacts gain and bandwidth?

Part-II

Q.1 a) For fig 1. using small signal model analysis calculates the output resistance and gain.

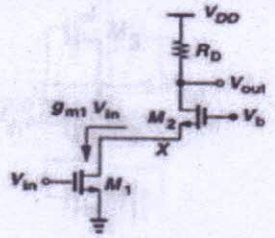


Fig. 1

b) What is the need of Darlington configuration and how it works? Derive the relationship for current gain for the Darlington pair.

Q.2 a) Analyze the circuit shown in Fig. 2 to determine the voltage at all nodes and the currents through all branches. Let $V_t = 1V$ and $k_n'\left(\frac{W}{L}\right) = 1mA/V^2$. Neglect the channel-length modulation effect i.e., assume $\lambda = 0$.

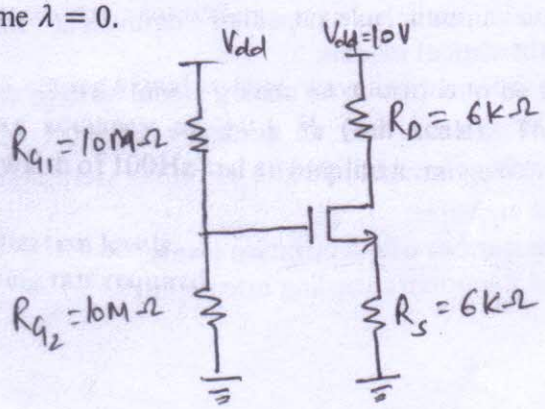


Fig. 2

b) What is the need of cascode configuration? Explain in detail with mathematical justification.

Q.3 a) Calculate the frequency response and gain of uncompensated two stage CMOS op-amp.

b) Consider a process technology for which $L_{min} = 0.4\mu m, t_{ox} = 8nm, \mu_n = \frac{450 cm^2}{V.s}$, and $V_t = 0.7$.

i. Find C_{ox} and k_n'.

ii. For a MOSFET with $\frac{W}{L} = 8\mu m/0.8\mu m$, calculate the value of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\mu A$.

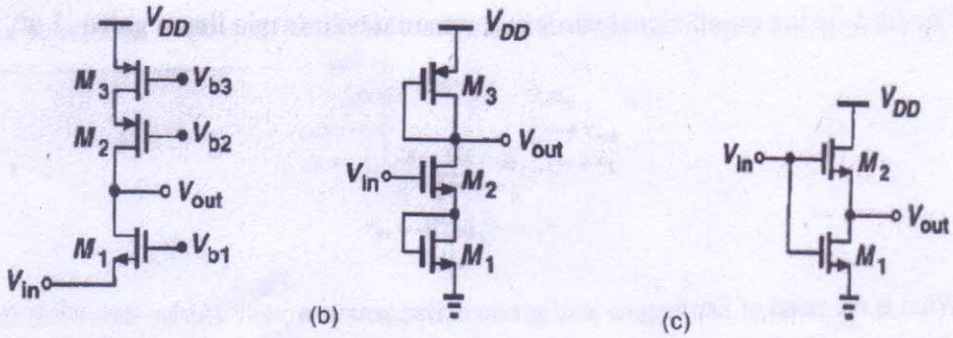
For the device in (b), find the value of V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS}.

Q.4a) Find the midband gain A_M and the upper 3-db frequency f_H of a CS amplifier fed with a signal source having an internal resistance $R_{sig} = 100k\Omega$. The amplifier has $R_G = 4.7M\Omega, R_D = R_L = 15k\Omega, g_m = \frac{1mA}{V}, r_o = 150k\Omega, C_{gs} = 1pF$, and $C_{gd} = 0.4pF$.

b) Derive the r_{out} for cascode current mirror and plot its output characteristic comparative to basic and Wilson current mirror.

Q. 5a) For an n-channel MOSFET with $t_{ox} = 10nm$, $L = 1.0\mu m, W = 10\mu m, L_{ov} = 0.05\mu m$, $C_{sb0} = C_{db0} = 10fF, V_0 = 0.6V, V_{SB} = 1V, and\ V_{DS} = 2V$, calaculate the following capacitance when the transistor is operating in saturation: $C_{ox}, C_{ov}, C_{gs}, C_{sb}, C_{db}$.

b) Calculate the small signal voltage gain the given below Fig. 3 (a) to (c).



Q.6 Write a short Note on :

(a) Explain switched capacitor equivalent resistor circuit with the help of mathematical models.

(b) The information in an analog signal voltage waveform is to be transmitted over a PCM system with an accuracy of ±0.1 % (full scale). The analog voltage waveform has a bandwidth of 100Hz and an amplitude range of -10 to +10 volts.

i. Find the step size.
ii. Find the number of quantization levels.
iii. Find the minimum sampling rate required.