MODELING AND SIMULATION OF LOW POWER VLSI INTERCONNECT

THESIS

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JANUARY, 2018

DECLARATION

I hereby declare that this thesis entitled "**MODELING AND SIMULATION OF LOW POWER VLSI INTERCONNECT***"* by **SUNIL JADAV**, being submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under faculty of Engineering & Technology, YMCA University of Science & Technology Faridabad, during the academic year 2017-2018, is a bonafide record of my original work carried out under guidance and supervision of Dr. Munish Vashishath, Department of Electronics Engineering, YMCA University of Science and Technology, Faridabad and Dr. (Mrs.) Rajeevan Chandel, Professor, ECE Department, National Institute of Technology (NIT), Hamirpur, Himachal Pradesh and has not been presented elsewhere.

I further declare that the thesis does not contain part of any work which has been submitted for the award of any degree either in this university or in any other university.

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CERTIFICATE

This is to certify that this Thesis entitled **"MODELING AND SIMULATION OF LOW POWER VLSI INTERCONNECT"** by **SUNIL JADAV**, being submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under faculty of Engineering & Technology YMCA University of Science & Technology Faridabad, during the academic year 2016-2017, is a bonafide record of work carried out under my guidance and supervision.

I further declare to the best of my knowledge, that the thesis does not contain part of any work which has been submitted for the award of any degree either in this university or in any other university.

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ABSTRACT

Very large scale integration (VLSI) technology has significant role in technological advancements in present day integrated circuits. In various electronics gadgets, wireless systems and modern integrated circuits, VLSI interconnects play an important role and are a crucial component. Presently, copper (Cu) is used as interconnect material in VLSI chips. Cu wire is fabricated using Damascene process. This conventional process gives Cu wire up to 1/8 aspect ratio (height to width ratio). With downscaling of metal oxide field effect transistor (MOSFET), there is also need of scaling of the interconnect dimensions. As interconnect sizes shrink, copper resistivity increases due to grain boundary and surface scattering effects and wires become more and more vulnerable to electro-migration due to the higher current densities. This process cannot be used below 45nm technology node. Carbon nanotubes (CNTs) have been suggested as futuristic material for interconnects in VLSI due to having better thermal capacity, mechanical strength and current carrying capacity. At higher current carrying capacity, the problem of electro-migration can be reduced. When graphene sheet is rolled up into cylinder, carbon nanotube is formed. As resistivity of Cu increases with technology scaling, this drives us to look for new interconnect material for future VLSI generations. Mixed carbon nanotube (CNT) bundle has superior properties like current carrying capacity and conductivity as compared to Cu interconnect. Mixed carbon nanotube is the mixture of single wall carbon nanotubes (SWCNTs) and multi-wall carbon nanotubes (MWCNTs) due to the nature of the bottom-up fabrication process.

In this thesis work, the impedance equations, impact of resistance (R), capacitance (C) and inductance (L) of the Copper &CNT bundle due to various process parameters like as average diameter, tube density, probability of metallic tubes and inner to outer diameter ratio of the bundle has been analyzed. The optimized values of these parameters have been considered. These optimized values are used in model verifications. The calculated results show that bundle has smaller values of R and C compared to its copper interconnects counterparts.

The various conventional circuit level and mathematical techniques of modeling the VLSI interconnect delay for global interconnects are reported in this thesis. The first

technique is to reduce interconnection delay by replacing Al wires by copper with thicker and wider lines in the upper levels for global interconnects. The second technique is adopted using cascaded drivers. The size of these drivers is increased in successive manner until the last device is large enough to drive the line and by using repeaters that divide the interconnection into smaller subsections. The concept of optimum number of repeater insertion for performance improvement of on-chip RLC interconnects is discussed. Power–optimal and voltage scaled repeaters insertion methodology for global interconnect for high throughput and low–power interconnect are reported. Hence, there is a limit to the performance improvement that can be obtained with repeaters in deep submicron designs in terms of power and delay and all the preceding methods also introduce area penalties for improvement of performance. Due to the advancement in technology, chip size is reducing and on-chip interconnection complexity is increasing. Hence, the performance improvement by using traditional methods in future technologies is not advantageous. The increasing speed requirement in VLSI circuits at future technology nodes demands for alternative signal transporting technique that may provide an attractive solution to some of the challenges caused by aggressive interconnect scaling. Current mode signaling has been explored as an alternative for data transmission over interconnects. Modeling of on-chip VLSI interconnects is reported in this thesis by incorporating the inductance effect in terms of effective line impedance. Three mathematical models are reported in this work for modeling the interconnect line delay for current and voltage mode schemes.

Global on-chip interconnects are limiting factor in modern high performance VLSI systems due to signal delay, power dissipation and wire bandwidth constraints. This research work addresses these limitations with a fundamental change in signalling technique by the use of current mode signalling. This work is intended to establish the theoretical formulation for the current mode signalling scheme while formulating its impact on signal delay, power dissipation and bandwidth. The above work is implemented analytically and also verified by simulation.

A simple and accurate closed-form delay expression for inverter driven on chip interconnects with a receive-end termination is presented. The solution can be used for both resistive and capacitive termination to adequately model current and voltage

mode sensing scheme. This model is also further extended to consider fast linear ramp signals.

Additionally, an approximate power dissipation model for current mode signalling is developed to understand the design trade-offs between current and voltage sensing. A comparison for power dissipation between voltage and current mode is also presented in this research work.

By using transmission line approach the *RLC* interconnect delay model is formulated for higher order system up to third and fifth order. For accurate results, higher order delay modelling is targeted using Fourier series method for ramp type signals.

This work investigates a low power, high speed, high throughput, area efficient current mode signalling technique. To explore current mode signalling technique a complete design of driver & receiver with decoding circuit is required. The proposed models show better performance in term of performance parameters delay, power, throughput, and energy per bit over conventional model. Based on the results and derived formulation a comparison between current mode(CM) and voltage mode (VM) with repeater insertion for long global deep-submicron interconnects is also presented with the proposed models.

The implication of low swing in SRAM architecture is also investigated by targeting the one SRAM column circuits. It is observed that the low swing on the data line is dependent on the cell read current and the cell read current depends upon the 6T SRAM access and pull down transistors. The transistors of 6T SRAM are optimised for minimum read and write delay as well as for power dissipation. Further the termination circuit modelling and simulative verification of low input impedance circuits are presented. The present research work shall be highly beneficial to VLSI designers and electronics engineers for performance enhancement of electronic circuits.

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LIST OF SYMBOLS AND ABBREVIATIONS

λ	Mean free path
ζ	Damping Factor
μ	Micro
Ω	Ohm
a	Atto
A	Ampere
C	Capacitance
Cu	Copper
CNT	Carbon Nanotube
L	Inductance
N	Nano
p	Pico
W	Watt
VM	Voltage Mode
CM	Current Mode
SWCNT	Single Walled CNT
MWCNT	Multi Walled CNT
FDTD	Finite Difference Time Domain
CMS	Current Mode Scheme

Chapter 1

INTRODUCTION AND PROBLEM FORMULATION

1.1 PREAMBLE

The diminishing interconnect cross-section, enhances the resistance. This is owing to the fact that the wire size becomes equal to the grain size of copper (Cu). Due to this, grain boundary scattering of electrons in Cu becomes a critical problem, which ultimately leads to increment in resistivity [1-4].With these issues, downgrading of the system resistance-capacitance (*RC*) time constant of on-chip interconnect emerges critically. Consequently, the uninterrupted performance degradation of on-chip copper and low dielectric interconnects is one of the immense challenges to keep Moore's law cognizant. On the other hand scaling of device dimensions provides significant delay improvement as seen in **Fig. 1.1.**

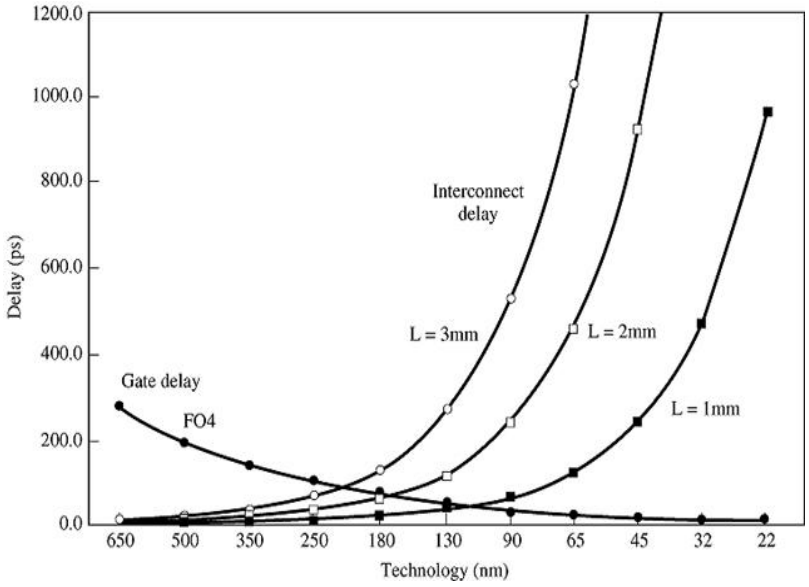


Fig. 1.1 Gate delay and global interconnect delay at different technology nodes.

Further for long or global interconnect, the up-scaling of interconnect dimensions degrades not only the response time but also affects other performance measures namely, power consumption, delay, reliability and bandwidth. The on-chip power consumption issue is linked with accrual number of repeaters to mitigate large *RC* time constant of aluminium or copper (Al, Cu) interconnects [5], switching factor, increment of operating clock and bus frequency. The reliability argument is very significant since upcoming systems need larger current per micro meter with the decrease interconnect cross-section, to preserve or elevate the operating clock frequency. This is straight away connected with the electro-migration

problem in interconnects, thereby forming hillocks and voids [6] as shown in **Fig.1.2**.Formation of voids and hillocks are damaging to on-chip signalling. This is because these are causative for open-circuit and short-circuit between closely placed wires. This is one of the major reasons of failure of system functionalities. Many methodologies have been proposed by the researchers such as metallization stack structure, calcium doping copper surfaces, grain boundary blocking etc. for reduction of electro-migration in copper interconnect lines, as this problem dominates in deep sub-micron (DSM) regimes [6-9].

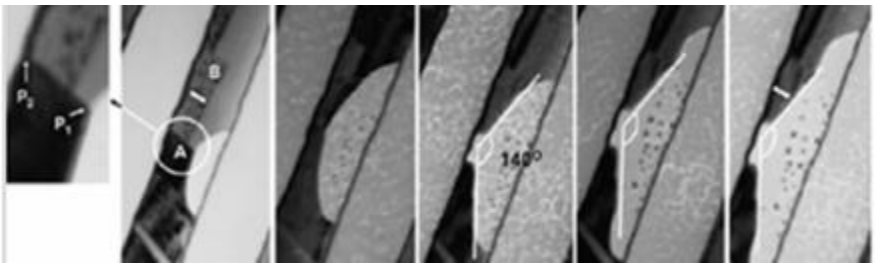


Fig. 1.2 Void growth recorded due to high current density in Cu interconnects at temperature (~250℃).

Further, the accumulating number of cores and memory units per system is increasing in highly scaled technology nodes. Though the number of interconnections between multiple cores/memory units is not increased as is expected, but this way integration of cores requires high bandwidth and low latency of adjacent modules links between cores as shown in **Fig. 1.3.** This makes bandwidth a much significant design parameter. The cost of cores depends on die area that hangs out consistent.

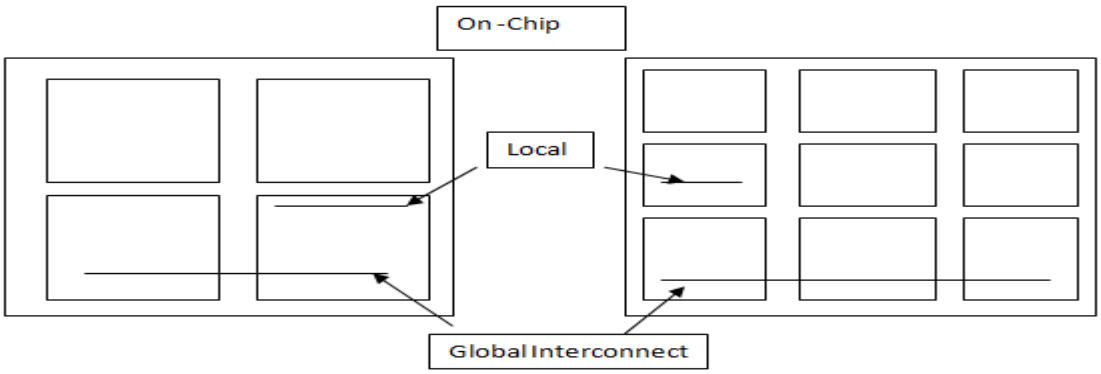


Fig.1.3 Scenario of global interconnects at future technology nodes.

A serious problem develops when a network on a chip communicates with other modules in complex designs. The problem is overcome by global interconnects which support this communication between different system on chip (SoC) modules. In future SoC systems the global interconnects will be required to supports higher bandwidths.

It becomes important to consider unique interconnect techniques which can mitigate the above mentioned complications of copper and low dielectric interconnects. Single and multi-wall carbon nanotubes (CNT), graphene sheets and high speed optical interconnection have been investigated as favourable substitutes to counter the above complications [10-11]. Carbon nanotubes showed superior behaviour over copper due to the ballistic nature of electrons in micro size graphene sheet. This results in high conductivity, and strong carbon bonding in gaphene nanoribbons generates higher electro-migration tolerance capacity [12].

Further it has been observed that optical transmission of data in interconnects contradicts from the CNT and Cu wire signalling schemes. This is due to a large amount of delay and power consumption in the terminating network rather than the waveguide. Outcome of optical interconnection behaviour regarding power dissipation is totally static and not dynamic [11] [13-14]. These technologies when coupled with supportive wire structures, presents new techniques for data transmission at speed of light, with minimum energy loss. But this optics technology having relatively large transmission medium (waveguides) possesses major shortcoming due to high pitches.

These technologies are promising candidates for matching to future interconnects requirements. These are experimentally limited by fabrication machineries. Hence, new low swing design techniques are very much required for interconnect circuit schemes. Of these the potential candidates are namely,(i)capacitive driven interconnects [15-20] and (ii)current mode signalling schemes, which are highly practical and promising [21-29].

In the present research work the mathematical modelling of on-chip interconnects with current mode schemes and its simulative analysis are presented. Combination of both the techniques is also dealt-with in this research work.

By using both the techniques, it is expected to achieve the future demand of high speed data transmission with low swing and low energy per bit on interconnect with tremendous improvement in system throughput. The technique of low impedance termination is utilised for achieving smaller delay and low swing. Problem of static leakage in current mode system has been minimised by proposing design techniques. Further it explores the applicability of low swing strategies by implementing SRAM architectures. The cell read/write currents are controlled for low swing and bit-line/data-line capacitances. It is found that the actual value

of cell ratio (width of pull down transistor/width of access transistor) depends on the desired rate of change of the bit-line/data-line voltage swing.

1.2 PROBLEM FORMULATION

This thesis presents mathematical modelling and simulations of *RLC* interconnect line by incorporating the effect of inductance in terms of line impedance. Due to results of it $R_{eff}C_T$ interconnect models are proposed for current and voltage mode schemes.

Higher order modelling of RLC interconnect line is also addressed. Fourier series technique is utilised on exact transfer function of transmission line. In this thesis it has been targeted up-to third and fifth orders of system function for copper and carbon nano-tube (CNT) type of materials. Various other parameters such as overshoot, undershoot, delay & damping factors are investigated for both the materials.

1.3RESEARCH OBJECTIVES

The main objectives to accomplish the above research problem are enlisted below:

- To study and analysis of various interconnect design techniques.
- To formulate and simulate analytical model for voltage and current mode interconnects.
- To perform the comparative performance analysis of both the models.
- To analyse the power consumption in current and voltage mode systems.
- To analyse the carbon nanotubes as current mode interconnects.
- To analyse leakage current and low input impedance for current mode scheme.

Mathematical analysis and graphical plots for the present research work have been carried out by using SPICE Tanner EDA tool, CNIA, and MATLAB 2009 [114].

1.4ORGANISATION OFTHE THESIS

Chapter1,Introduction:This chapter presents detail of the existing technology based on either circuit, material and process level for VLSI interconnects and associated signalling solution is presented. Future intermediate and global interconnects requirements are described while

focussing on signal delay propagation, power dissipation, bandwidth, throughput and area. In this chapter the objectives of research are followed by problem formulation are presented.

***Chapter 2,Literature Review*:** It provides on comprehensive literature review of interconnects with repeaters and optimal numbers of repeaters followed by current mode signalling and materialistic view of various type of on –chip VLSI Interconnects are reported. Base on the prolongation provided by ITRS, prospective global wire tendency are specify by concentrating on power dissipation, delay and bandwidth. The reflex of Cu and low k dielectrics, delay deterioration and coupling capacitance due to adjoining wire are discussed and presented. Further the impact & problem due to scaling are addressed, Future interconnect materials are also focussed with targeting the synthesis & properties of CNT material. Equivalent circuit models of SWNCT are also discussed and presented. Signalling schemes and extant solutions to problems related to global interconnects are investigated.

***Chapter 3,Modeling of RLC Equivalent RC Delay Model*:**The chapter presents the proposed *RLC* Equivalent *RC* delay models for global VLSI interconnects. The theoretical basis for the voltage and current-mode signalling is presented in detail. Propagation delay and power dissipation are addressed for current/voltage mode signalling in deep sub-micrometer global interconnect by conversion of line series resistance into equivalent impedance. Analytical voltage and current mode interconnect comparison for delay, bandwidth, energy per bit, dc coefficient on the line is calculated & presented.Which is further investigated for CNT type of materials at scaled technologies & impact studied on interconnect lines. The dominance of static power over voltage mode is estimated and proved. Further the performance is improved by developing the optimum bulk signal model for reduction of standby and sub-threshold leakage in terms of various parameters, and static leakage control is presented with current mode driver circuits.

***Chapter 4, Modeling of Higher Order System Using Transmission Line & Fourier Method*:**Focuses on modelling of transfer function using first and higher order systems with transmission line and Fourier methods. Further the results are calculated for Cu and CNT like materials and comparison for third and fifth order delay is estimated. And impact of inductance, overshoot, undershoot are presented with technology scaling & challenges.

Chapter 5, Modeling & Utilization of Low Swing on Data-lines & Low Impedance Receiver: Modelling of low swing on data-line/bit-lines in memory operation is dealt-with in this chapter. The applicability of low swing is presented by modelling of read/ write operation of memory architecture. Modelling and simulation of receiver circuitry is also estimated and discussed.

Chapter 6, Conclusion & Future Scope: This chapter summaries the main results of the analyses of the present thesis. The major contributions and outcome of the research work are highlighted, followed with future scope of research work.

Chapter 2

LITREATURE REVIEW

2.1 INTRODUCTION

Interconnects are the backbone of any integrated electronic circuit. These are an integral part of any on-chip system. By employing fast and efficient transmission of data on the chip interconnects plays a key role in the performance of the entire system. This chapter provides a review of the VLSI interconnects which can be developed by using various materials along with different signaling techniques. Interconnect has been modeled as a single lumped capacitance for performance analysis of on-chip interconnects [30]. With the scaling of technology and increased chip sizes, the cross-sectional area of wires has been scaled down along with the increase of interconnect length [37]. The resistance of interconnect therefore increases significantly. This requires the use of more accurate RC delay models [31].With increase in length, interconnect delay increases quadratically due to linear increase in both interconnect resistance and capacitance [32-33]. The long interconnections lead to high propagation delays. Buffers are needed to drive the high capacitive nodes in order to keep track with the required speed. A large number of buffers termed as repeaters are required to be inserted at regular intervals of distance in interconnect due to the limitation of a single buffer [32].

2.2 INTERCONNECTS WITH REPEATER INSERTION

Several methods have been introduced to reduce interconnect delay so that their impedances do not dominate the delay of a critical path. Sakurai, Elmore and Bakoglu present a method in which the delay of repeater is characterized by the input capacitance and output resistance based on the geometric size of the repeaters [32-34]. Bakoglu equalizes the delay of the repeaters and the interconnect delay to optimize the number and size of repeaters for a specific resistance-capacitance (RC) interconnect model. Wu and Shiau describe a repeater implementation to reduce interconnect delay [35-36]. Their method uses a linearized form of the Shichman-Hodges equations [37] at a specific operating point to determine the proper repeater insertion locations.

Dhar and Franklin present a mathematical treatment for optimal repeater insertion to enhance the data rate of system on chip [38-40]. The method for enhancing the data rate of global VLSI interconnects is also proposed in [41-42]. Latched repeaters are used for insertion with interconnects for synchronous pipelines structures like the First in First Out (FIFO). Due to the use of this technique the clock frequency of integrated circuits and communication system can be increased. Similar analogy is also presented and named as "Elastic interconnects" technique [43]. In this technique repeater placed in global wires are capable of compressing and decompressing the data. Another mechanism of regenerative repeaters insertion is adopted to minimize the propagation delay is reported [44].Parallel regeneration repeaters use bidirectional buffering for sensing the initial transition. These repeaters are idealistic for Microprocessors & Microcontrollers where bidirectional buses are used. These are classified as dynamic or static repeaters [44]. Dynamic repeaters gated clock consumes to charge the line up to supply voltage. While in static repeaters the pre-charge device is completely separate and replaced by inverse of pull down circuitry.

Other repeater insertion methods are described in [45-48]. Ismail and Friedman extended previous research in repeater insertion by considering the line inductance. They demonstrated that on-chip inductance can decrease the delay, area and power of the repeater insertion process as compared to an RC line model [49-51]. Even in recent times for performance improvement of interconnects, the techniques of low swing transceiver, large size repeater, temperature impact and reconfigurable interconnect design for ultra dynamic voltage scaling system have been targeted using CNT based material in [52-58]. Rusu and Gowan claimed for 32% of power is consumed by the Global clock network in ALPHA 21264 at maximum operating frequency of 600MHz in 350nm process [59-60]. Mclnerney states that about 13k nets are required at the top level Itanium processor, out of these 11k require a repeater insertion [61]. Further out of 11k, about 7.5k needs buffered repeaters. With these conventional techniques there is limit to the performance improvement. Hence voltage scaled repeaters have been presented for low power and high speed signal transmission [63-64]. But, the problem of area overhead and power remains. Hence, researchers started to explore other technique either from signaling point of view or by shifting the material technology. If researchers proceed for shifting material technology then it will be a revolution in semiconductor technology which was going to be very expensive and challenging. Hence, technology researchers decided to work on Circuit Level Techniques of Signalling. The

achievements of researchers using signalling techniques like current mode signalling are presented with exhaustive survey in the next section.

2.3 REVIEWS OF CURRENT MODE SIGNALLING

Further a literature review of current mode signaling approaches is presented in an effort to identify design tradeoffs and associated circuit complexity. A new GaAs current mode chip to chip interconnection circuit is presented that provides high signal transfer speed with 50Ω active termination and reduced input voltage swing. The power dissipation is shown to be 1/8 of an ECL input/output. The ternary logic version can reduce wiring by half and eliminates clock and skew problems by low power dissipation [64]. Thrice improvement in speed can be achieved by using the current mode approach rather than the conventional voltage-mode operation as reported in theoretical analysis [65].

A novel circuit for current sensing receiver can be used for uni-directional and bi-directional communication. Simulation results show an improvement of 32% in speed and 27% less power consumption at high data rates for 0.13μm CMOS technology for 10mm long on-chip wires. Bashirullah et al. have addressed propagation delay and power dissipation for current mode signaling in deep sub-micrometer global interconnects[21]. Based on the effective lumped element resistance and capacitance approximation of distributed RC lines, accurate closed-form expressions of delay and power dissipation were presented. A new power dissipation model for current –mode signaling is developed to understand the design tradeoffs between current and voltage sensing. Based on the results and derived formulations, a comparison between voltage and current mode for long global interconnect in 0.18μm technology is presented. Katoch et al. [66] have presented three current mode circuits technique (a) Single Ended Current Mode Circuit (b) Differential Current Mode Circuit (c) Pulsed Base Current Mode Circuit. The first two circuits are very suitable in applications where high data activity is expected. The third circuit has a lower static current consumption and also offers 2 times speed advantage. It is suitable for low latency application where low data activity is expected. Venkatraman et al. have proposed a multi-valued current mode technique for on-chip interconnects [67]. Monte Carlo Analysis investigates that the proposed multi-level current signaling system is robust in the presence of process induced parameter variation. Individual parameter sensitivity analyses show that the total average power is most influenced by supply voltage and effective gate length. The delay is most influenced by

interconnects resistance and capacitance. The multi-valued current mode technique is explored by Joshi [68]. Joshi et al. have proposed a novel multi-valued current mode driver and a receiver for very low line voltage swing. It is reported that there is 50% reduction in latency and upto 100 times reduction in power over voltage mode buffer insertion technique. Data rates upto1Gb/s are also reported. A delay insensitive and high performance long on-chip communication using level-encoded two phase dual-rail (LEDR) encoding and current mode signaling are presented[69-70]. Hence, more than two times throughput improvement is achieved at global lengths of the wires compared to on-chip interconnect implemented using LEDR and voltage mode signaling. Chandel et al., B.K. et al., X.C. et al., and Zhao et al. investigated current mode signalling technique using finite difference time domain (FDTD) technique with copper and CNT material satisfactory performance for global interconnect [28-29], [71-78] are reported.

The design of on-chip interconnects needs to be focused. This is due to the dominating drawbacks of long interconnect namely, signal delays, power dissipation and crosstalk signals, for complete system performance. Hence it is mandatory for the forthcoming on-chip interconnect designs to validate the high transmissions speeds, reliability, bandwidth and throughput requirements. This is because CMOS IC technology is scaling down every twelve months and named as per "shifted Moore's Law". It is thus very clear that global interconnect advancement is essential for future technology integrated circuits by doing necessary modification in signaling and material technology. In terms of material, the use of Cu and low dielectric interconnect has diminished some of the problems related with signal sharing but still some of the modifications are required. Hence, the some changes are required at the architectural and others in terms of new design approaches. To reduce the bandwidth problem in deep sub-micron (DSM) regime, new design technique of steep signaling are required to achieve the future clock signals provided by international technology road map for semiconductors (ITRS) [79].

In this review impact of scaling on global interconnects with specifically different wire model is presented. Materialistic performance comparison of various interconnects materials especially Al versus Cu, Cu and low dielectric interconnects is carried out. Further single and multi-walled carbon nanotube bundles and lastly optical interconnects signal transmission with the speed of light are reported. The reported literature relate to various signaling

schemes mainly focuses on delay, throughput, bandwidth, power and signal swing issues, rather than process fabrication threats.

2.4 TECHNOLOGICALVIEW OF Al/Cu/CNTAND SCALING

VLSI chips of 1970s and 1980s used poly-Si and aluminum for on-chip interconnects. Chips used to have much lesser number of interconnect levels than the present technology nodes. Gate delays were the speed limiting elements, with interconnect delays being very less. Poly-Si was used in the lower levels since it is also the gate material and can be deposited by the self-aligned CMOS integration process. Aluminum was used for higher levels (chips had only 2-4 interconnect levels at these nodes).

Aluminum has been used because it has good conductivity and is easy to deposit on the VLSI chips. The aluminum deposition has minimum interference with silicon, and so aluminum could be used as the interconnect material with no major problems at these nodes. Copper, however possesses a better conductivity than aluminum, but the fabrication process is complex. Copper could not be dry etched like aluminum and it also contaminated Silicon by diffusion. Once these limitations were overcome with advances in technology, copper is used for interconnects along with low-k dielectrics for the inter-level dielectric (ILD).

Copper as an interconnect material has been used only since 1998 when IBM demonstrated the first microprocessor made of copper interconnects. Aluminum also has a problem of electro-migration at large current densities. This is mitigated by copper because of heavier copper atoms. The fabrication process for copper interconnects is more complicated than for aluminum.

With the evolution of the Damascene process, copper came into use for on-chip interconnects. This conventional process to fabricate the Cu wire gives the wires up to 1:8 aspect ratios. This process can’t be used in very deep sub-micron (VSDM) Technologies. The problem with copper is that copper atoms ionize, penetrate into the dielectric and then accumulate in the dielectric as copper ions. The presence of these charges degrades the performance of the dielectric giving rise to leakage currents. This necessitates the use of barriers/liners made of Tungsten, Titanium and Tantalum alloys between the copper interconnect and the dielectric to prevent migration of copper ions [80].

The adequacy of near-term interconnect technology (copper wires) to continue for meeting the performance requirements for ICs fabricated for succeeding technology generations varies with the intended function of the interconnect net and the technology used to fabricate the Cu wires. As requirements increase, it is increasingly necessary that interconnects be considered as part of a system that includes the package and the silicon chip to satisfy the total technology needs for the IC. **Fig. 2.1** shows the typical cross section of different metal layers in a high performance microprocessor chip. The hierarchical scaling of interconnects can be seen, i.e. the lowest levels of interconnects are thin and they get wider in the top layers. This is because different levels are used for connecting different classes of signals

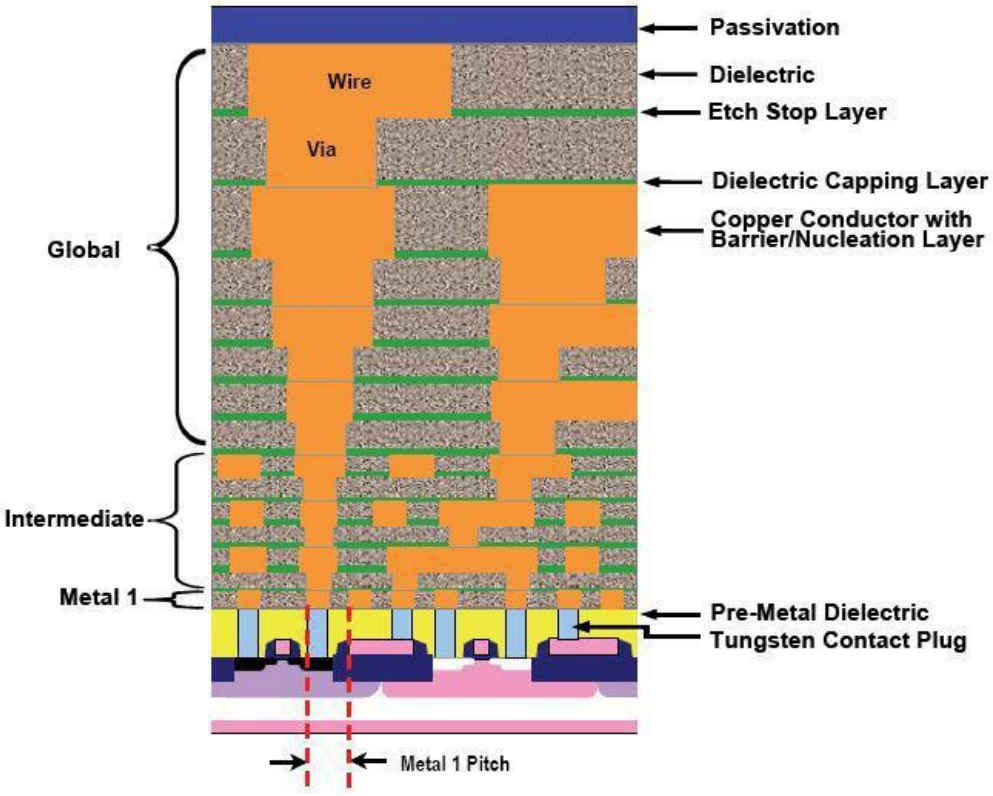


Fig. 2.1 Cross-sectional view of hierarchical scaling [79].

2.4.1 Problems With Interconnect Scaling

The problem of copper reacting with silicon is eliminated by using barriers. However, by down-scaling other problems crop up with copper interconnects. This is because of the small feature sizes and quantum mechanical effects which dominate at these sizes[80]. The main effects are given below.

Grain boundary scattering

Grain boundaries in copper increase with decreasing line width [81]. Electrons can scatter at these grain boundaries as shown in **Fig. 2.2**.

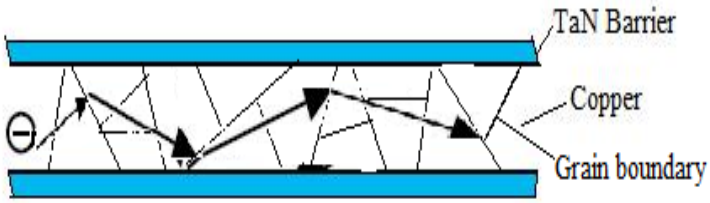


Fig. 2.2 Grain boundaries scattering in Cu wire.

Surface scattering

There is considerable scattering at the Cu-Barrier interface [81]. As the interconnect size decreases, the effective surface area per unit volume of the interconnect increases and hence surface scattering increases as shown in **Fig. 2.3**.

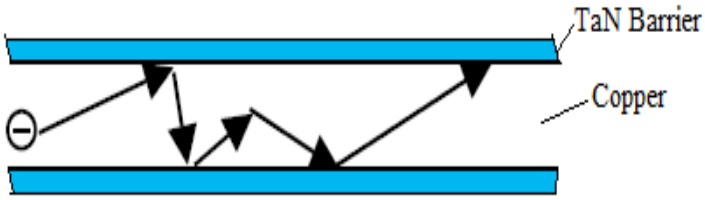


Fig. 2.3 Surface scattering in Cu wire.

Electro-migration

When the current density in conductors becomes very high, there is momentum transfer between the electrons and the atoms of the conductor [81]. This leads to diffusion of the conductor atoms due to which interconnects break and stop conducting as shown in **Fig. 2.4**.

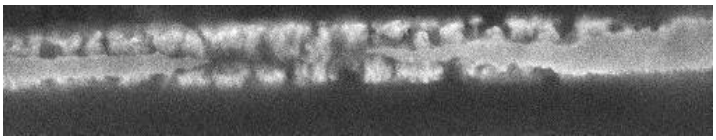


Fig. 2.4 Electro-Migration in Cu wire.

Because of both types of scattering i.e. grain boundary scattering and surface scattering, resistivity of Cu begins to increase which is shown in **Fig. 2.5**. The effective resistivity of copper therefore increases with a decrease in feature size. This leads to greater RC delays and the speed of the interconnect decreases.

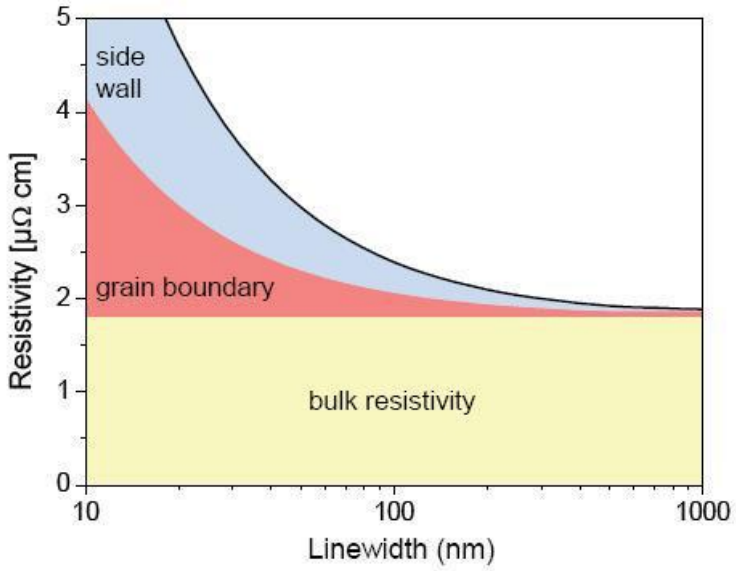


Fig. 2.5 Copper resistivity with decreasing feature size.

The adequacy of near-term interconnect technology (copper wires and low-κ dielectrics) to continue meeting the performance requirements for ICs fabricated for succeeding technology generations varies with the intended function of the interconnect net and the technology used to fabricate the Cu wires. As requirements increase, it is increasingly necessary that interconnect be considered as part of a system that includes the package and the silicon chip to satisfy the total technology need for the IC [79].

The increasing RC delay is one of the most crucial parameters especially for high performance products. While scaled wires in the local and intermediate wiring levels are less critical and show only a moderate increase in RC, the fixed length interconnects in the semi-global and global wiring levels are much more sensitive and need the introduction of repeating inverters to keep the RC delay within viable limits. However, the introduction of these repeaters requires additional chip area and increases the power consumption. In some designs this increased RC delay can be handled by modifications such as modular architectures to reduce the need for fixed line lengths. One recent approach in this direction is the dual- or multi-core architecture in state-of-the-art microprocessors. Parallel data processing in the multi-cores allows comparable or even higher processor performance at lower core frequencies and reduced power consumption as compared to a single core high performance processor. However, such significant modifications to circuit architecture suffer from the disadvantages of needing new design tools and software and are not generally applicable to all designs.

While RC delay is a major factor for many digital applications, capacitive coupling in the local and intermediate levels is a highly sensitive issue for low power applications. Crosstalk and noise associated with decreasing geometries and increasing currents are becoming a larger problem for both digital and analog circuits. These trends are a strong function of design strategy, and shall be considered in that context.

In addition to the problems with scaled wires for clock and signaling, an equally difficult problem for interconnect is circuit power distribution. Increasing supply current, related to the decreasing V_{dd}, causes an increased voltage drop between the power supply and the bias point for fixed length wires. This problem cannot be solved as easily as the repeater solution for the fixed length clock and signal wires.

Due to scaling, integrated circuits become more complicated and the active devices on a chip become smaller and more numerous. The interconnections on the chip will also grow in complexity and length. The problem of power dissipation and delay in wire will increase.
Cu has a bulk resistivity of 1.9 μΩ-cm, and ITRS assumes that the effective resistivity for Cu/barrier interconnects will remain at 2.2 μΩ-cm for the future. However, as the diameter of Cu wire approaches the mean free path (~40nm) of electrons in the wire, its resistivity will increase dramatically due to electron scattering effects.

In addition, ITRS predicts that maximum current density (J_{max}) required for intermediate wiring will increase to 3.0×10^6 A/cm^2 by the end of 2010 and this will be reach 6.9×10^6 A/cm^2, at 18nm technology node. The maximum current density Cu can handle is about 10^6 A/cm^2 before electro-migration effects make lifetime unacceptable. Thus, new interconnect materials must be used. Current density and effective resistivity for future has been shown in **Table 2.1.**

TABLE 2.1

ITRS-Projected Current Densities and Conductor Effective Resistivity [79]

Year of production	2010	2012	2013	2015	2016	2017
J_{max}(A/cm^2)	3.0×10^6	3.7×10^6	4.3×10^6	5.1×10^6	5.8×10^6	6.9×10^6
Wire resistivity (μΩ-cm)	2.2	2.2	2.2	2.2	2.2	2.2

2.5 FUTURE ON-CHIP INTERCONNECTS

In addition, at 0.13μm technology approximately 51% of microprocessor power was consumed by interconnects. The projection is that without changes in design philosophy, today up to 80% of microprocessor power will be consumed by interconnects [82]. This dramatic increase of the interconnect impact on performance and power shows clearly the challenges created by the scaling of the conventional metal/dielectric system. In the last few years IC manufacturers have recognized the difficulty of addressing interconnect performance limitations. They have implemented design and architecture improvements to address interconnect limitations. With these advances, interconnects remains a critical bottleneck for many applications. This creates an increasing opportunity for developing and introducing alternative technology solutions beyond metal/dielectric, interconnects.

The alternate interconnect technology options being considered offer more far-reaching opportunities than this original intent. These additional opportunities include the use of alternate interconnects to reduce cost, to improve performance or utility, and other features of current IC applications. The other alternatives are discussed in the following sub-sections.

2.5.1 3D Interconnects

In integrated circuits the burden of high frequency signal propagation can be reduced by implementing stacking of active components using 3D interconnects. 3D interconnects are found to be one of the alternatives to replace on-die interconnects for both high performance and density reasons.

The outcome of using 3D interconnect is that it replaces on-die interconnect for minimum delay and power. While the advantage of delay and power will depend on the details of a specific 3D implementation, it is true that for global interconnects, power and delay of interconnects including optimized number of buffers named as repeaters depends linearly on the line length [79]. A second advantage of 3D interconnect is that it allows the communication between different circuit functions. A memory-intensive processor operation is one the cases illustrated in [82]. A memory can be easily placed closer to processor due to the help of 3D Interconnects and reasonable amount of power can be saved by shortening the wires. The 3D integration method used for this application will require high-density die-to-die connections.

2.5.2 Optical Interconnects

Number of solutions has been proposed for system on chip interconnects (signaling and clock distribution) and input and output devices. With the help of efficient driver the signal can be propagated on –chip optical interconnect with the speed of light and the larger bandwidth of waveguide can be utilized. For running of any input/output application with larger bandwidth, optical solutions which mainly focus on the aggregate bandwidth and/power saving per bit, this overcomes the limitations imposed by losses in present interconnects packages(metal contacts and dielectric). This technique of signaling helps in avoiding or minimizing the need for high power equalization circuits and pre-emphasis hardware.

Delay and power considerations in optical interconnects are not expected to fully replace the lower metal-dielectric interconnect layers in microprocessors due to high pitch constraints. The main focus is on cost efficient implementations that take advantage of the unique properties of optical architectures to increase overall system performance (i.e.,not on total Cu/low k replacement). Such optical solutions shall be viable, only when CMOS technology development proves its compatibility with optical components. This is of prime importance. At the present time significant progress has already been made in this area and found that this area is not significantly developed or mature to define an intersection of the present existing interconnects technology roadmap.

The merits of using optical interconnects are near speed-of-light data propagation and huge bandwidth. However, there are other advantages. Among these one of the advantages is that signals propagated have a minimum transmission crosstalk, and the ability to convert transmission within a waveguide, and multi-wavelength capability. Due to minimum photons interaction, minimum crosstalk occurs between signal paths and ability for light to propagate in waveguides, provides significant design flexibility for advancement of optical technology. Due to the capabilities to accommodate multiple wavelengths for a single optical path increases the data carrying capacity. It also provides bandwidth densities not achievable by electrical means.

2.5.3 RF/Microwave Interconnects

RF or microwaves can be used as radical alternative to the metal/dielectric interconnect for transmission of signals from one part of a chip to another [82-83]. LAN on a chip, with trans-receivers, antennas and appropriate signal generation and detection circuitryis the option for

radio technology. Such type of transmission can be considered as a “free-space transmission” through integrated circuit structures. Another solution is that the radio and microwave signal can be capacitively coupled in a waveguide (package lid). Depending upon the nature of data signal such as a sinusoidal signal or as a coded digital signal, can be employed with RF/microwave systems. Each has its own merit and demerits, depends upon requirements. Once this type of technology developed, it will really help to near future internet of things (IoT) technology. The coming decade is of IoT technologies.

2.5.4 Carbon Nanotube (CNT) Interconnects

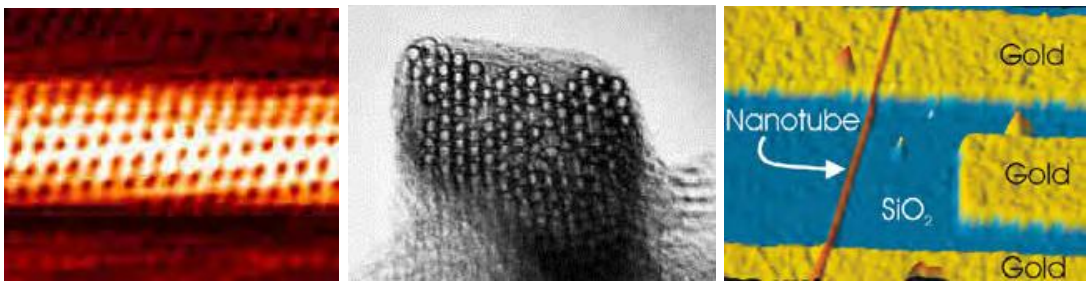
Carbon nanotubes (CNTs) are considered a potential solution to improve the performance of on-chip interconnects in terms of speed, power dissipation and reliability. Carbon nanotubes are rolls of graphene sheets, which are one atom thick carbon layers. CNTs have aroused major research interest in their applicability as very large scale integration (VLSI) interconnects for future generations of technology because of their desirable properties such as large electron mean free paths, excellent mechanical strength, high thermal conductivity, and large current carrying capacity. As interconnect dimensions scale and copper resistivity increases due to size effect, CNT interconnects become more attractive.

Carbon Nanotubes have been proposed as solutions to many problems in various industries. Their high electrical and thermal conductivity, as well as their ability to be deposited in either metallic or semiconducting states, has attracted interest for possible applications in interconnected structures.

A)Types of Nanotubes

Carbon nanotubes are cylindrically rolled up sheets of graphene. Graphene is a single atomic layer of graphite, which is made of carbon atoms arranged in a hexagonal honeycomb pattern. Carbon nanotubes have a diameter of 0.5 to a few nanometers. They exist as Single-Wall Carbon Nanotubes (SWNT) which are a single atom thick or Multi-Wall Carbon Nanotubes (MWNT) which are concentric SWNTs. It has a larger electron mean free path (in μm) than the mean free path of Cu(nm) [79]. They can behave as metals or semiconductors depending on the way in which they are rolled [82].

Carbon nanotubes have excellent electrical properties that make them one of the most promising building blocks for future nanotechnologies. The performance of individual devices, in particular field-effect transistors, compared with standard CMOS devices. However, there are still some serious issues that remain to be solved before a viable technology could be developed. In particular, the main concern regards the controlled synthesis and positioning of nanotubes. The combination of their electrical properties with their chemical, mechanical and thermal properties has already opened very promising routes toward new type of applications in electronics. CNT interconnects are expected to meet many of the requirements for technologies below the 45nm node in terms of mechanical strength, thermal conductivity and electrical performances [84]. Some real-world nanotubes have been shown in **Fig. 2.6.**



(a) (b) (c)

Fig. 2.6 (a) AFM image of chiral tube of 1.3 nm diameter. (b) TEM image of a crystalline nanotube bundle. (c) A single nanotube as interconnect between gold electrodes

A carbon nanotube is realized by rolling-up a sheet of a mono-atomic layer of graphite (Graphene) as shown in **Fig. 2.7**. The rolled graphene may become either metallic or semiconducting, depending on its chirality, i.e. the way in which it is rolled up. A single-wall carbon nanotube (SWCNT) is made by a single sheet of graphene [85] whereas a multi-wall carbon nanotube (MWCNT) is made by nested sheets. Both types of CNTs i.e. SWCNT and MWCNT have been shown in **Figs. 2.8** and **Fig. 2.9**. Mixture of both above CNTs is called mixed carbon nanotube bundle as shown in **Fig. 2.10.**

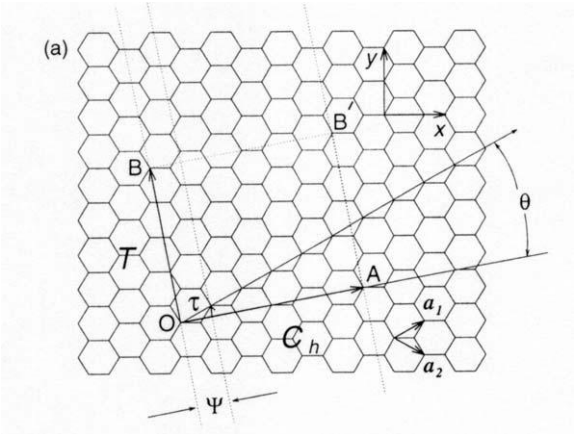


Fig.2.7 A Graphene sheet [85]

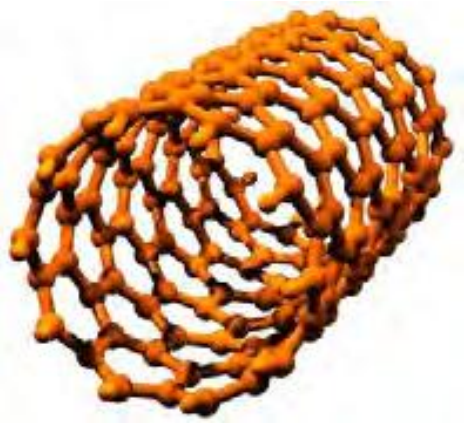


Fig. 2.8 SWCNT

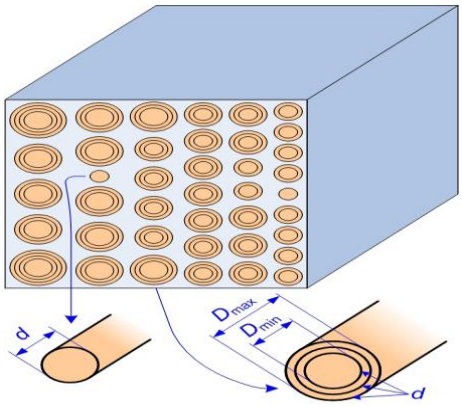


Fig. 2.9 MWCNT

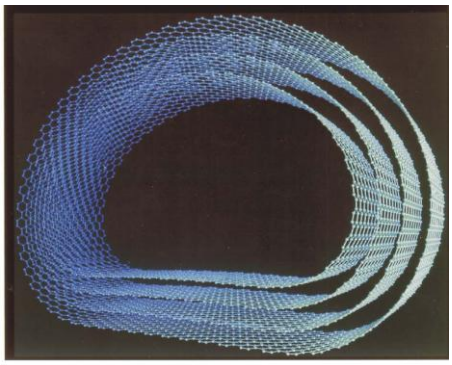


Fig. 2.10 Mixed CNT bundle

SWCNTs consist of only one graphene shell, and their diameter may vary from 0.4 nm to 4 nm with a typical diameter of 1.4 nm [82-83]. MWCNTs consist of several concentric graphene cylinders, and their outer diameters may vary from a few to 100 nm [83] [86], and the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite [83].

Two vectors C_h and T, whose rectangle defines the unit cell of the "unpacked" nanotube, can be defined as shown in **Fig 2.7.** C_h defines the circumference on the surface of the tube connecting two equivalent carbon atoms, $C_h = na_1 + ma_2$, where a_1 and a_2 are the two basis vectors of graphite and n and m are integers. n and m are called indices and the nanotube is represented by these numbers as (m, n). The indices determine the chiral angle

θ=tan^{-1}[$\sqrt{3}n/(2m+n)$]. The chiral angle is used to separate carbon nanotubes into three classes differentiated by their electronic properties which have been given below.

(i) Armchair (n=m, θ =30°)
(ii) Zig-zag (m=0, n>0, θ =0°)
(iii) Chiral (0<|m|<n, 0<θ<30°)

Armchair carbon nanotubes are metallic (a degenerate semimetal with zero bandgap). Zig-zag and chiral nanotubes can be semimetals with a finite bandgap if n- m/3 = i (i being an integer and m≠n) or semiconductors in all other cases [85]. The bandgap for the semi-metallic and semiconductor nanotubes scales inversely with the tube diameter, giving each nanotube an electronic behavior unique to itself.

2.6 CARBON NANOTUBE SYNTHESIS

Carbon nanotubes were initially observed by Iijima in carbon soot made from arc-discharge. Large scale manufacturing techniques even today are based on the same principle which was used by Iijima. The proposed applications of CNTs will not be realized until nanotube growth is optimized and controlled. For composite applications, high-quality CNTs are required at the kilogram or ton level, which requires growth methods that are simple, efficient and cost-effective. For device applications, the layout of CNTs will rely on self-assembly or controlled-growth strategies on substrates combined with micromachining technologies. CNT growth is a high temperature process. Generally, CNT growth occurs when a metallic catalyst serves as a seed into which high-energy carbon atoms dissolve resulting in an extruded well-ordered tubular structure. In general, CNTs can be grown by arc-discharge, laser ablation, and chemical vapor deposition (CVD) methods [87]. However, for device applications, growth of CNTs by CVD methods is particularly attractive due to features such as selective spatial growth, large-area deposition capabilities and aligned CNT growth.

2.6.1 Arc-Discharge Method

An arc-discharge process has been developed to prepare high-quality MWNTs and SWNT. In this process, carbon atoms are evaporated with inert gas plasma characterized by high electric currents passing between opposing carbon electrodes (cathode and anode). Usually, the

carbon anode contains a small percentage of metal catalyst, such as cobalt (Co), nickel (Ni), or iron (Fe). In 1992, a standard arc-discharge technique had been used for fullerene synthesis to the large-scale synthesis of MWNTs under a helium atmosphere [88]. The results show that the purity and yield depend sensitively on the gas pressure in the reaction vessel. The length of the synthesized MWNTs is several micrometers with diameters ranging from 2 to 20 nm. The nanotubes are highly oriented and thus highly crystalline. However, such synthesized CNTs are inevitably accompanied by the formation of carbon particles that are attached to the nanotube walls. A subsequent purification process is necessary to achieve high-purity nanotubes. In 1993, production of SWNTs had been reported by an arc-discharge method using a carbon electrode that contained ~2 atomic % cobalt [89]. At high temperature, the carbon and metal catalyst are co-vaporized into the arc, leading to the formation of carbon nanotubes with very uniform diameter (~1.2 nm). However, fullerenes (by-products) also form readily in this process. In order to obtain high-purity SWNTs, a purification process is therefore necessary. Its yield up to 30% by weight[90].

Limitations of tubes tend to be short (50μm or less) and deposited in random sizes and directions [90]. This method carried out at temperatures greater than 3,000°C, which limits the scale-up of CNT production. Furthermore, the CNTs produced by this method is accompanied by by-products, including fullerenes, graphitic polyhedrons, and amorphous carbon in the form of particles or overcoats on the sidewalls of the nanotubes [87]. So purification is essential.

2.6.2 Laser-Ablation Method

In 1996, this method had been reported for synthesis of high-quality SWCNTs [91]. This method utilized double-pulse lasers to evaporate graphite rods doped with 1.2 atomic % of a 50 is to 50 mixture of Copper and Nickel powder, which was placed in a tube furnace heated to 1,200°C in flowing argon at 500 Torr and this process was completed with heat treatment in the presence of vacuum at 1,000°C to achieve C_{60} and other fullerenes. The resulting SWCNTs were quite uniform, had a diameter of ~1.38 nm, and formed ropes consisting of tens of individual SWCNTs closely packed into hexagonal crystal structures that were stabilized through van der Waals forces.

Typical yield:Up to 70% [87, 90].

Advantages:Diameter of SWCNTs can be controlled by varying the reaction temperature [87].

Limitations: This method is very costly because it requires very costly laser [87]. By-products are also present there so this method also needs purification.

2.6.3 Chemical Vapour Deposition Method

Chemical vapor deposition (CVD) methods are particularly attractive for CNT growth for electronic device applications [87]. The CVD growth process involves heating the catalyst to a high temperature and introducing hydrocarbon gas or carbon monoxide (CO) into the reactor. The mechanism for CNT growth has been generally assumed to be a dissociation-diffusion-precipitation process in which elemental carbon is formed on the surface of a metal particle followed by diffusion and precipitation in the form of cylindrical graphite [87]. The critical parameters in CVD growth of CNTs are the carbon precursor, catalyst, reactor chamber pressure, and growth temperature. The effect of these process parameters on CNT growth has been investigated extensively and the trends observed provide additional insight into nanotube growth. However, the detailed nanotube growth mechanisms are still not well understood. This method is very simple in which a substrate is placed in an oven at 600^{o}C. On the addition of hydrocarbon gas such as methane, this gas decomposes and frees up carbon atoms. These carbon atoms can be recombined in the form of nanotubes [90].

Typical yield: 20-100% [90].

Advantages: CVD is the easiest of the three methods to scale up to industrial production. It may be able to make nanotubes of great length [90].

Limitations: Usually MWCNTs are obtained by this method and are often riddled with defects [90].

2.6.4 Properties of CNTs

Carbon nanotubes have very extra ordinary properties which has been discussed in **Table 2.2**

TABLE 2.2

Properties of Carbon Nanotubes [90]

PROPERTIES	**SWCNTs**	**COMPARISON with other materials**
Size	0.6 to few nm in diameter	Electron beam lithography can create lines 50nm wide, a few nm thick
Density	1.33-1.40 gm/m^3	Aluminum has a density of 2.7gm/cm^3
Tensile Strength	45 billion pascals	High-strength steel alloys break at about 2 billion pascals
Resilience	Can be bent at large angles and restraightened without damage	Metals and carbon fibers fracture at grain boundaries
J_{max}	Nearly 1 billion A/cm^2	Cu burns out at 1 million A/cm^2
Field Emission	Can activate phosphors at 1-3V if electrodes are spaced 1µm apart	Molybdenum tips require fields of 50-100V/ µm and have very limited lifetimes
Heat Transmission	Predicted to be as high as 6000W/m-K at room temperature	Nearly pure diamond transmits 3320W/m-K
Temperature Stability	Stable up to 2800^{o}C in vacuum, 750^{o}C in air	Metals wires in microchips melt at 600-1000^{o}C
Cost	$1500/gm	Gold is very cheaper than CNTs

2.7 CARBON NANOTUBE AS INTERCONNECTS

Carbon nanotubes interconnect are considered potential solutions for most of the problems faced by copper interconnects. CNTs have many desirable properties such as large electron mean free paths, large mechanical strengths, and high thermal conductivity and can support very large current densities. As discussed previously, with the scaling of interconnect dimensions, the resistivity of copper increases due to size effects, and it is proposed that CNT interconnects can replace copper from the 45 nm technology node.

2.7.1 Comparative Review of CNT and Cu

From a material point of view, CNTs are superior to copper because of the following reasons [79]:

- **Ballistic Transport:** Due to the one dimensional nature of CNTs, the phase space for electron scattering in CNTs is very limited and the electron mean free path is very large (of the order of 1 μm) in comparison to the mean free path in copper which is of the order of 20-40 nm. Electrons can travel large distances without getting scattered and this allows ballistic transport of charge carriers in CNTs.

- **Resistance to Electro-migration:** CNTs being made of graphene sheets have strong sp^2 hybridized carbon atoms which leads to a very high mechanical strength. As a consequence of this, CNTs can carry large currents without suffering any physical damage. CNTs can support current densities up to 10^9 A/cm^2 in comparison to copper which can carry currents only up to 10^6 A/cm^2 before electromigration sets in. Since the ITRS requirement for current densities is increasing with scaling, CNTs would be ideal candidates for interconnects.

- **Thermal Conductivity:** The longitudinal thermal conductivity of CNTs is very high, in the order of 6000 W/m-K in comparison to that of bulk copper, 400 W/m-K. CNTs can therefore conduct heat at a much faster rate than copper and limit any buildup of temperature along the interconnect. The low-K dielectrics used as ILD have large thermal expansion coefficients, temperature buildup leads to reliability problems. This can be mitigated by using CNTs as interconnects.

2.7.2 Integration of CNT Interconnect

CNTs can potentially replace Cu/low-K interconnects at most levels of interconnect hierarchy except in places where low-resistance short interconnects are needed [92]. For instance, to distribute power and ground in the first interconnect level, CNT interconnects would be significantly more resistive than minimum-size copper wires. They can bring significant performance advantages when replacing the long global interconnects where the RC delay of interconnects is important. SWCNTs can be integrated for on-chip interconnect applications in the following forms which are given below.

- **SWCNT Bundles:** A bundle of densely packed SWCNTs with the same dimensions as Cu/low-K interconnects with high-quality contacts with the electrodes would be an ideal candidate for replacing Cu/low-K interconnects to lower the interconnect resistance and address the problem of size effects in copper wires. This integration option provides significant delay improvements for long interconnect where the RC delay is dominant [83] [93- 94].

- **Few-layer of SWCNT interconnects:** A few-layer arrangement of SWCNTs can reduce the capacitance of the CNT-based interconnects by as large as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects where the delay is dominated by capacitive loading of interconnects and not their resistance [93].

- **Large-Diameter MWCNTs:** It has been proven both theoretically and experimentally that all shells within MWCNTs can conduct if proper connections are made to all of them [95, 96]. There are reports of very large mean free paths in high-quality MWCNTs [95]. Theoretical models suggest that long large-diameter MWCNTs can potentially outperform Cu and even SWCNTs if the level of disorder in these tubes can be kept as low as those in SWCNTs and all shells can be properly connected to metal contacts [97]. These MWCNTs would be suitable for semi-global and global interconnects.

SWNTs are one-dimensional conductors. Since their dimension along the cross section is much lesser than their Fermi velocity, the Density of States (DOS) resembles a one-dimensional system, thereby leading to totally different electrical transport properties. One dimensional conductors show a fundamental resistance which is independent of their length. For one channel of conduction, this resistance is a fundamental constant called the von Klitzing constant, $R_l = he^2 = 25.8K\Omega$, where h is the Planck's constant and e is the charge of the electron.

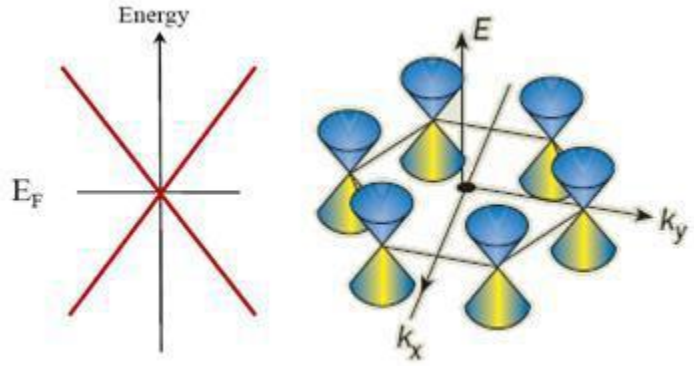


Fig. 2.11 Band diagram of an ideal metallic CNT and phase space of CNTs

Metallic SWNTs are zero-band gap semiconductors as shown by the E-k diagram of **Fig. 2.11**. There are four channels of conduction in parallel and hence the effective quantum resistance becomes $R_l = 4he^2$=6.45 KΩ. Actual transport through CNTs is a quantum phenomenon, but it can also be modeled using circuit models.

2.7.3 Circuit Model of an Isolated SWCNT

The equivalent circuit model for an isolated single-walled carbon nanotube [99] is shown schematically in **Fig. 2.12**. The model and its components are explained in detail in the following subsections.

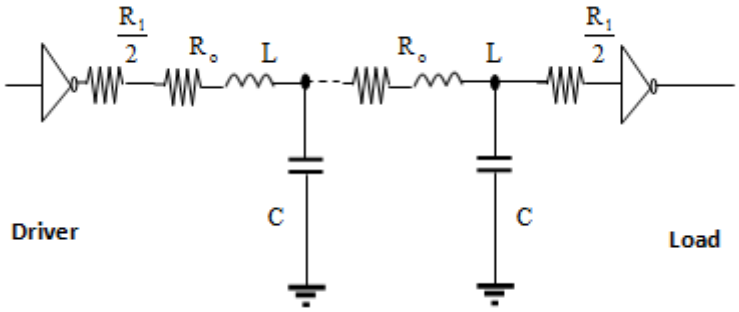


Fig. 2.12 Equivalent circuit model for an Isolated SWCNT

(a) Resistance of an isolated SWCNT

The conductance of a carbon nanotube is evaluated using the two-terminal Landauer-Buttiker formula. This formula states that, for a 1-D system with N channels in parallel, the conductance $G = (Ne^2/h)T$, where T is the transmission coefficient for electrons through the

sample [100]. Due to spin degeneracy and sub lattice degeneracy of electrons in graphene, each nanotube has four conducting channels in parallel (N=4). Hence the conductance of a single ballistic single-walled CNT (SWCNT) assuming perfect contacts (T=1), is given by $4e^2/h = 155$ μS, which yields a resistance of 6.45 kΩ [100]. This is the fundamental resistance associated with a SWCNT that cannot be avoided. As shown in Fig. 2.12, this fundamental resistance (R_l) is equally divided between the two contacts on either side of the nanotube.

$$R_l = \frac{h}{4e^2} \tag{2.1}$$

The mean free path of electrons (the distance across which no scattering occurs) in a CNT is typically 1 μm [101]. For CNT lengths less than 1 μm, electron transport is essentially ballistic within the nanotube and the resistance is independent of length (6.45 KΩ). However, for lengths greater than the mean free path, resistance increases with length as shown in Eq. 2.2, where L_0 is the mean free path and L is the length of the CNT. In the equivalent circuit, this additional scattering resistance would appear as a distributed resistance per unit length to account for resistive losses along the CNT length.

$$R_o = \left(\frac{h}{4e^2}\right)\frac{L}{L_o} \tag{2.2}$$

The total resistance of a CNT is then expressed as the sum of resistances arising from the above two aspects: the fundamental one-dimensional system (CNT) contact resistance and scattering resistance. Evidently the resistance associated with an isolated CNT is too high for realizing an interconnection. Hence, a bundle/rope of CNTs is needed that has much lower effective resistance and may work effectively as an interconnection.

(b) Capacitance of an Isolated SWCNT

The capacitance of a CNT arises from two sources. The electrostatic capacitance *(C_E)* is calculated by treating the CNT as a thin wire, with diameter 'd', placed a distance 'y' away from a ground plane, and is given by the formula in Eq. (2.3) (C_E per unit length) [101] for y>2d. The quantities y and d are shown in **Fig. 2.13.** For d=1 nm, y=1 μm, C_E ≈30 aF/um. This is the intrinsic plate capacitance of an isolated CNT.

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{2.3}$$

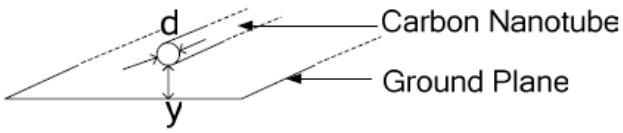


Fig 2.13 Isolated conductor, with diameter 'd', over a ground plane at a distance 'y'.

The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Due to the Pauli Exclusion Principle, it is only possible to add electrons into the nanotube at an available quantum state above the Fermi energy level. By equating this energy to an effective capacitance, the expression for the quantum capacitance (per unit length) is obtained as shown in Eq. (2.4) [101], where h is the Planck's constant and v_F is the Fermi velocity. For a carbon nanotube ($v_F \approx$ 8x105m/s), $C_Q \approx$100aF/um [101].

$$C_Q = \frac{2e^2}{hv_F} \tag{2.4}$$

As a CNT has four conducting channels as described previously, the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$. The same effective charge resides on both these capacitances (C_E and $4C_Q$) when the CNT carries current, as is true for any two capacitances in series. Hence these capacitances appear in series and resultant capacitance (C) has been shown in the effective circuit model shown in **Fig. 2.12**.

(c) Inductance of an Isolated SWCNT

The inductance associated with an isolated SWCNT can be calculated from the magnetic field of an isolated current carrying wire some distance away from a ground plane, as depicted in **Fig. 2.13.** In addition to this magnetic inductance (L_M), the kinetic inductance is calculated in [101] by equating the kinetic energy stored in each conducting channel of the CNT to an effective inductance. The four parallel conducting channels in a CNT give rise to an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are shown in equation. (2.5) and (2.6) below.

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \tag{2.5}$$

$$L_K = \frac{h}{2e^2 v_F} \tag{2.6}$$

For d=1 nm and y=1 um, L_M (per unit length) evaluates to≈1.4 pH/um. On the other hand, L_K (per unit length) for a CNT evaluates to 16 nH/um. Since $L_K >> L_M$, the inclusion of L_K can have a significant impact on the delay model for interconnects.

2.8 Summary

VLSI interconnects have been studied for several decades for low power and high density network on a chip. Understanding of current mode interconnects for microelectronics is a complex and continually evolving challenge. In this chapter, we present an extensive literature review pertaining to the state of the art issues in current mode interconnect signalling and circuit design. Various research papers, books and application notes have been referred, which take care of the various aspects of understanding of current mode interconnect. In particular, this review gives a bibliographical survey of the current research efforts in the area of VLSI Interconnect. The chapter also presents challenges anticipated in the future years to come and enlists scope for research. In a nutshell the various models are reviewed. The focus is on providing an overview of the developments that have taken place in the area of current mode interconnects.Carbon nanotube (CNT) is a future candidate for VLSI interconnects. Its properties are reviewed and impact of scaling is presented. Further the synthesis techniques adopted for development of CNTs are also presented. Equivalent circuit model of SWCNT and its parameters is also highlighted in this chapter.

The literature survey carried out in this chapter emphasizes the importance and need of improved interconnect design for VLSI on-chips. Various research challenges and gaps have been identified. The research objectives so identified have been taken up in the present research work. The various model developed, analyses and results are presented in the succeeding chapters of the thesis.

Chapter 3

MODELLING OF RLC EQUIVALENT RC DELAY MODELS

3.1 Introduction

Amongst different technologies CMOS technology is the most valuable technology for integrated circuits fabrication for VLSI applications such as laptops, mobile phones, digital signal processing, remote sensing, medical processing, automotive digital machineries and various others. CMOS chips consume smaller energy in comparison with the other logic families. Due to this superiority CMOS developed and advanced significantly. CMOS have emerged very attractive and dominatingly important. Hence massive modern integrated circuits are fabricated using MOS processing technologies [102]. Recent CMOS processing, silicon substrate are doped to produce MOS device having a polysilicon gate with a very small oxide layer under the metallic gate contact. The source and drain regions of a transistor are generated by using acceptor/donor nature of impurities by diffusion or ion implantation processes. Some amount of electric force is applied on the gate input to produce the channel between drain and source. When a potential is applied on the drain terminal of the MOSFET, current flows from drain to source. A bundle of metal layers is available to the designer for interconnections of transistors and resistors. The short interconnect layers have higher resistance as compared to the top interconnect layers. Thus the value of parasitic capacitance and inductance differ from one interconnect layer (metallic) to another.

Moore's Law states that the number of MOS transistors on an affordable CPU would two fold in every two years. During the last thirty years, CMOS technology has wrinkled the transistor size into the nanometre regime. With reference to International Technology Roadmap [103], the minimum feature size remains decreasing at the rate of 0.7 times per technology [103]. Due to this regular scaling, superior circuit speeds, lesser power and higher packing densities of transistors are accomplished. In the present time, AMD, Freescale, IBM, ST Microelectronics etc. Are working jointly on 22nm and 32nm technology nodes. They manufacture a number of memory and microcontroller units. They are working well beyond the range of GHz. The response time of an electrical signal in chips depends on gate switching delay and the wire delay. The interconnect delay is more dominant and significant

than the device switching delay. Hence, the modelling of high speed low power on-chip interconnection is very important area of research.

With technology scaling, the interconnect delay dominates the gate delay. As a result of large operating frequencies and technology scaling inductance effect cannot be ignored. Inductance is the property of an electrical conductor by which a change in current flowing through it induces an electromotive force in both the conductor itself and in any nearby conductors by mutual inductance. Inductance behavior is more prominent in long distance as compared tocapacitive behavior provides the limitation in the interconnect circuits. Further voltage and current systems are highlighted in terms of difference in signaling.

In theoretical model of conventional voltage-mode signalling, the receiver provides interconnect with a high impedance termination, which can be as simple as an inverter. The signal logic is sensed based on its voltage and is determined by the switching threshold of the inverter. In voltage mode an inverter drives long line is terminated by the gate of MOS transistor receiver and presents a very large impedance termination & charging the wire capacitance and gate capacitance builds up a voltage along the line.

The main difference between the current-mode and voltage-mode signalling is the termination of the interconnect line. In theoretical representation for current-mode signalling, the line is terminated by a short shunt the wire capacitance. Avoiding the charging of the wire capacitance, current-mode systems saving power and time [21] [64-65]. However, current-sensing requires special circuit techniques compared to conventional CMOS. The biggest challenge in current-mode signalling is designing efficient sensing circuitry [66-70]. A typical inverter can be used to drive an interconnect. The low impedance path to ground causes static power dissipation. The receiving (sensing) circuit is complex in current-mode as MOS transistors are not normally thought of as having a current threshold. Hence, amplify signal and provide low impedance termination.

3.2 Mathematical and Simulative Analogy of RLC and $R_{eff}C_T$ Models

Previous work on distributed resistance –inductance –capacitance model of VLSI interconnect [104-105] is extended in [106] that describes a new physical model for the transient output voltage of a distributed RLC interconnect with a step input and

capacitiveload. The comprehensive model for the transient response of a distributed RLC interconnects is derived in [106]. This model has been compared to SPICE simulation program. After comparison it has been observed that the models have negligible error for a wide range of parameters. The time delay of a lossless line $t_{d,lc}$ has been calculated in [106] by setting $r = 0$ in equation (3.1).

$$\frac{2Z_o}{Z_o + R_{tr}} e^{\frac{-rt_d}{2l}} \left[1 - e^{-\left(\frac{1}{C_L Z_o}\right)(t_d - t_f)}\right] u_o(t_d - t_f) = \frac{1}{2} \tag{3.1}$$

where, Z_o, R_{tr}, C_L, r, l, t_d, t_f represent characteristic impedance, source resistance, load capacitance, line resistance, length of line, time delay and time of flight (ToF) of line respectively.

Further this equation reduce to

$$\frac{2Z_o}{Z_o + R_{tr}} \left[1 - e^{-\left(\frac{1}{C_L Z_o}\right)(t_{d,lc} - t_f)}\right] u_o\left(t_{d,lc} - t_f\right) = \frac{1}{2} \tag{3.2}$$

Equation (3.2) can be simplified as

$$t_{d,lc} = t_f + C_L Z_o \ln\left(\frac{4Z_o}{3Z_o - R_{tr}}\right) \tag{3.3}$$

By Using Linear Curve Fitting (3.3) can be approximated as

$$t_{d,lc} \cong t_f + C_L(0.45R_{tr} + 0.25Z_o) \tag{3.4}$$

Therefore, the time delay expression in equation (3.4) can be rewritten for a lossy RLC line as:

$$t_{d,rlc} \cong t_f + C_L(yrL + 0.45R_{tr} + 0.25Z_o) \tag{3.5}$$

To estimate the value of y, Consider Sakurai Model for Resistance –Capacitance Delay model as reported in research paper [107]:

$$t_{d,rc} = 0.377rcL^2 + 0.693(R_{tr}cL + rLC_L + R_{tr}C_L) \tag{3.6}$$

For highly resistive line, the distributed RLC line provides the same time delay as the RC line model, as given in equation (3.5) and (3.6). Assuming

$$rL \gg Z_o, C_L \gg cL \text{ and } rL \gg R_{tr} \tag{3.7}$$

With these conditions equation (3.5) will reduce to

$$t_{d,rlc} \cong C_L yrL \tag{3.8}$$

Further, equation (3.6) will reduce to

$$t_{d,rc} = 0.693rLC_L \tag{3.9}$$

By comparing equations (3.8) and (3.9), the value of y can be determined & given as:

$$y = 0.693.$$

Substituting this value in equation (3.5) and simplifying gives the approximate model for time delay of distributed RLC line with load capacitance as

$$t_{d,rlc} \cong t_f + 0.693C_L(rL + 0.65R_{tr} + 0.36Z_o) \tag{3.10}$$

From the above discussion we find that the actual time delay for a line is equal to the RC delay if resistance dominates, or is equal to the RLC delay if inductance dominates. Hence every interconnect has a distributed inductance associated with it. The terms RC and RLC are only suggestive of whether the line is dominantly resistive or inductive. Hence, time delay model that will reduce to the RC delay if resistance dominates or to the RLC delay if inductance dominates. The time delay of an interconnect is the greater of the RC and RLC model delay i.e. and given by the following relation:

$$t_d = \max(t_{d,rlc}, t_{d,rc})$$

For a simple RC charging circuit as shown in **Fig. 3.1(a)** the output voltage (V_o) and 50% rise time are given by equations (3.11) and (3.12) respectively.

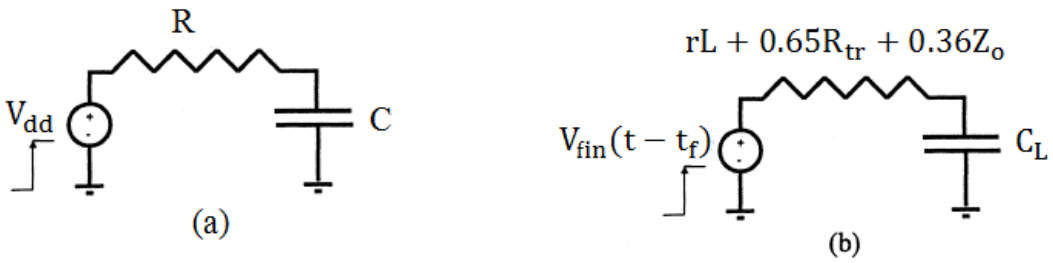


Fig. 3.1 (a) RC Charging circuit **(b)** Equivalent effective impedance of RLC line.

$$V_o(t) = V_{dd}\left(1 - e^{-\left(\frac{t}{RC}\right)}\right) \tag{3.11}$$

and

$$t_{d,50\%} = 0.693RC \tag{3.12}$$

Comparing equations (3.10) and (3.12), the transients induced in the quiescent distributed RLC line can be approximated as an RC charging of the load capacitance. The equivalent lumped element circuit model of the quiescent RLC line can be represented by **Fig. 3.1 (b)** by incorporating impedance in the current path is

$$R = rL + 0.65R_{tr} + 0.36Z_o \tag{3.13}$$

But neglecting source resistance, equation (3.13) becomes

$$R = rL + 0.36Z_o \tag{3.14}$$

For 10mm, length of interconnect the following parameters were estimated using PTM [108] $R = 22\Omega/mm, L = 1.937nH/mm, C = 243.7fF/mm,$ with $V_{in} = 1.8V, T = 10ns, t_r = t_f = 10ps, C_s = C_L = 0$ (ideal case), $R_s = 8\Omega, R_L = 10k\Omega,$ otherwise C_s & C_L have finite value for physical structure range of femto farad (fF). Simulative comparison between actual RLC model and equivalent $R_{eff}C_T$ is presented below in **Fig. 3.2**. The relative error between the actual & equivalent model is within the range of 3% as observed through simulation. The justification of equivalency between two models is presented below on comparing actual RLC model with $R_{eff}C_T$. Simulation and analytical value shows the results are in close agreement with the actual RLC and RC models. In this chapter on the basis of this analogy a mathematical modelling of VLSI interconnect with voltage and current mode signalling is presented.

Inductance control mechanism and operating frequency limitation for different dimensions and length of interconnects are reported further. The importance of damping factor is also considered as a figure of merit for modelling RLC equivalent RC models.

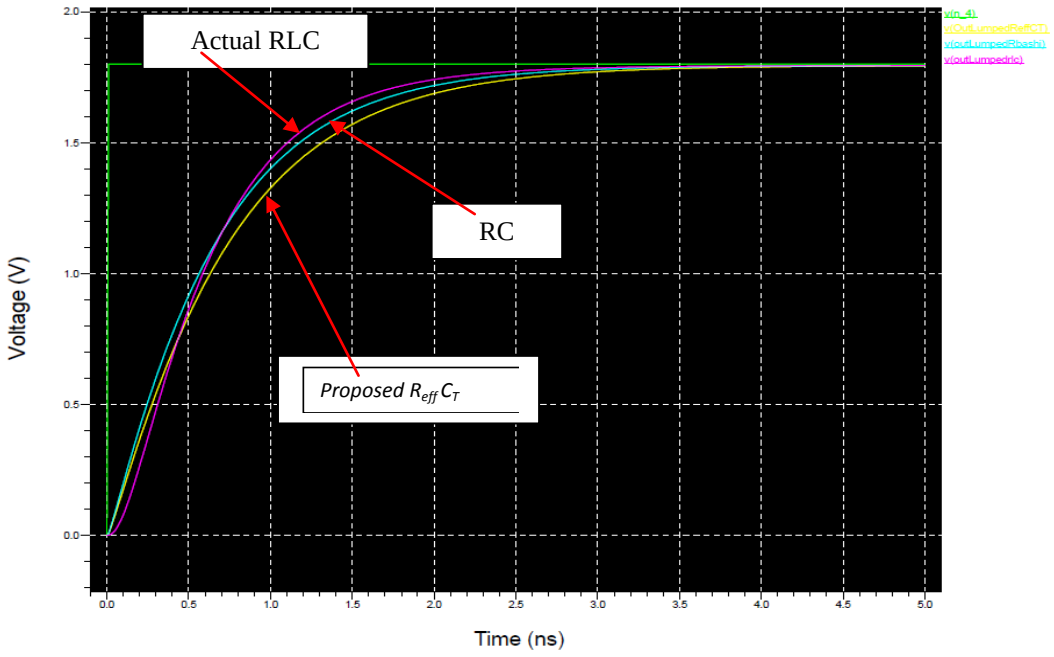


Fig. 3.2 Simulative analogy lumped models of actual RLC and $R_{eff}C_T$ and Simplified RC.

3.3 Model I Close Form Delay Formulation of VLSI Interconnect

In this section the interconnect delay model is developed for current mode signaling. The long interconnect line is modeled as a distributed RLC interconnect lines. In this work, inverter drives the long interconnect lines (or the memory storage components such as registers and SRAM cells) as shown in **Fig. 3.3(a)** and **Fig. 3.3(b)** respectively. The register or accumulator unit in a microprocessor as in **Fig. 3.3(b)** when accessed, will draw a read current through the data line, thus pulling down the potential of the bit line (interconnect line). Similarly, the inverter of **Fig. 3.3(a)** can be represented by a signal current source, which can be shunted by a resistance (the inverter output resistance). Thus both the situations depicted in **Fig. 3.3 (a)** can be modeled as shown in **Fig. 3.4.**

Fig.3.3 Long interconnect lines represented by distributed RLC transmission lines, and driven by **(a)** An inverter and **(b)** An architecture of a processor.

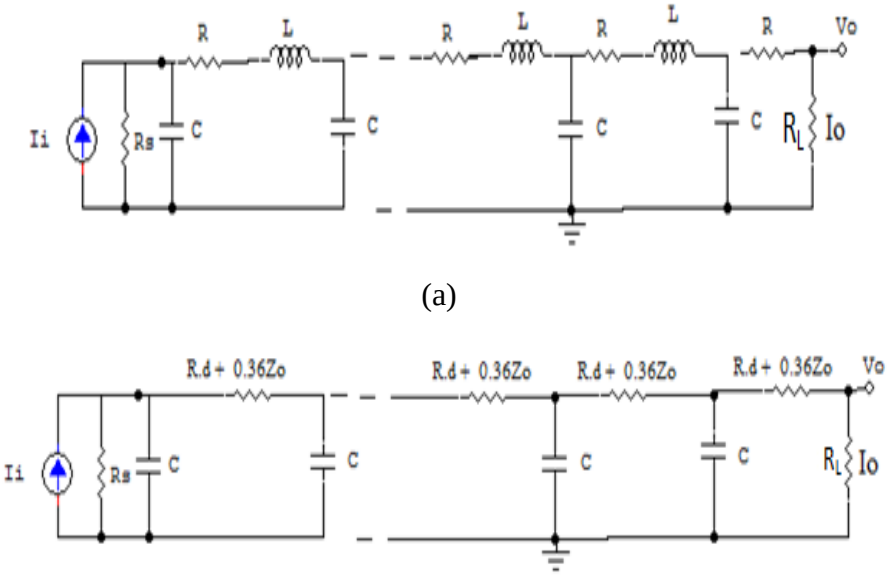
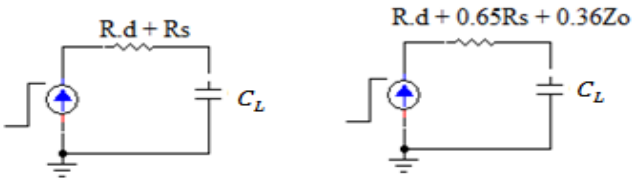


Fig. 3.4(a) Equivalent circuit model for **Fig.3.3**, output resistor R_L is added for generality. **(b)** Line inductance modeled into effective resistance $R_{eff} = R.d + 0.36Z_o$[22]

In **Fig. 3.4** I_i is the access current or it may be output current of driver circuit of register unit or memory cell. R_S is either the source resistance of the inverter or the bit-line load in parallel with the drain resistance of the access transistor. This is the output device of the memory cell. The infinite RLC ladder structure represents the interconnect line. The total resistance of the line is given by R_T and the total capacitance by C_T.The inductive effect of the line is approximated into effective resistance (R_{eff}). For the sake of generality the output of line is terminated by resistor R_L.

As the self-inductance of the line increases, it affects both the line delay and load delay. In order to physically understand the phenomena, assuming a step is applied to the line, on the rising edge, the line inductance resists the increase in current, which further increase the line delay. In order to quantify the inductance effect, a voltage mode delay model is expressed in terms of characteristic impedance Z_0, as is derived in research paper [22]. **Fig. 3.5** shows the equivalent circuit model for the voltage mode interconnects, where $Z_0 = \sqrt{L/C}$, L & C are the unit length inductance & capacitance and d is the total length of the interconnect line. In case of RC line, the equivalent resistance equals "$R.d + R_S$", however, When inductive effect is dominant the equivalent resistance becomes"$R.d + 0.65R_S + 0.36Z_0$", i.e. R_{eff} where the coefficient "0.65" and "0.36" reflect the shielding effect of inductance [22]. R_{eff} acts as a total line resistance and this new RLC model approximated as $R_{eff}C_T$ model.



(a) (b)

Fig. 3.5 Equivalent voltage mode interconnect model for an **(a)** RC Line Model **(b)** RLCmodel for an interconnect line of length'd'.

The RLC distributed model in **Fig.3.4 (a)** will be equivalent to the network shown in **Fig. 3.4(b)** and the definition of delay for the above network is defined as illustrated in **Fig. 3.6**

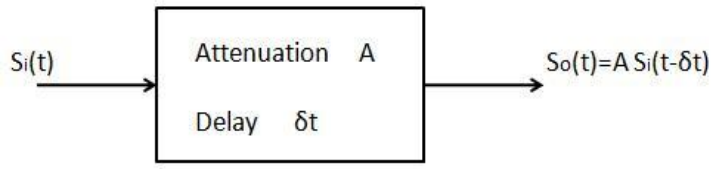


Fig. 3.6 Block diagram representation of a linear network, having attenuation A and delay δt.

For the formulation of delay a general linear network, having attenuation A and delay δt, which is driven by input signal $S_i(t)$, being either voltage or current mode is considered. The output signal is $S_o(t) = A.S_i(t - \delta t)$and has delay δtwith respect to the input signal. For the linear-ramp type of input signal $S_i(t) = p\,t$ and $S_o(t) = A.p(t - \delta t)$, with p the constant slope. The delay δtisrelated to the Elmore Delay as reported in research paper [31-32]. The Elmore delay is defined in terms of the step response of a linear network.

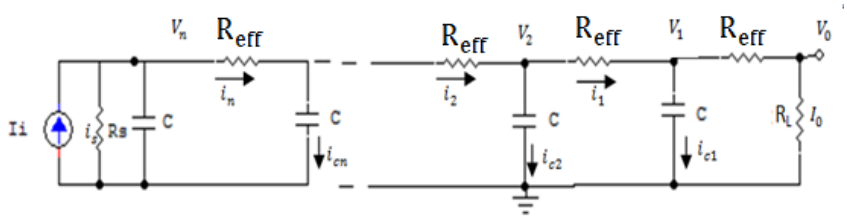


Fig. 3.7 Equivalent model of RLC interconnect line

Analytical expression for delay of the $R_{eff}C_T$ interconnect line is derived using equivalent model shown in **Fig.3.7.** It is assumed that the output current is a linear-ramp type signal:

$$i_o = p_o\,(t - \delta t), \qquad -\infty < t < \infty \tag{3.15}$$

Where p_o is the constant slope δt the delay and t is time.

A linear-ramp output signal is always associated with a linear-ramp input signal. Since$i_o$is a linear ramp &$v_1$also will be a linear ramp.

$$v_1 = i_o(R_{eff} + R_L) \tag{3.16}$$

Now the current through capacitor C between the nodes v_1 and ground will be constant:

$$i_{c1} = C\frac{dv_1}{dt} = C(R_{eff} + R_L)\frac{di_o}{dt} = p_o C(R_{eff} + R_L) \tag{3.17}$$

It follows that the current $i_1$is also a linear-ramp signal, since it is the sum of the linear-ramp current $I_o$and the constant current i_{c1} **.** Repeating this argument for all the other sections of the $R_{eff}C$ line, it is finally concluded that the input current $i_i$is a linear-ramp signal.When the input current is a linear-ramp signal, it follows that all voltages are linear ramps and other currents are either constant or linear ramps. Output current i_o is the function of input current i_i can be written as

$$i_o = f(i_i)$$

as shown in Fig. 3.7and Node voltage v_2 can be written as using (3.16) & (3.17)

$$v_2 = 2i_0R_{eff} + i_oR_L + \rho_oCR_{eff}(R_{eff} + R_L)$$

i_{c2}can be written as:

$$i_{c2} = C\frac{dv_2}{dt} = \rho_oC(2R_{eff} + R_L)$$

And from Fig. 3.7, i_2 can be calculated as

$$i_2 = i_o + 3\rho_oCR_{eff} + 2\rho_OCR_L.$$

Hence, the nodal voltages v_3 and v_4 and the currents i_3 and i_4 can be computed. Subsequently, v_3 and v_4 and $i_3$and i_4 are given as:

$$v_3 = 3i_oR_{eff} + i_oR_L + \rho_oCR_{eff}(4R_{eff} + 3R_L) \quad (3.18)$$

$$i_3 = i_o + 6\rho_oCR_{eff} + 3\rho_oCR_L \quad (3.19)$$

$$v_4 = 4i_oR_{eff} + i_oR_L + \rho_oCR_{eff}(10CR_{eff} + 6R_L) \quad (3.20)$$

$$i_4 = i_o + 10\rho_oCR_{eff} + 4\rho_oCR_L. \quad (3.21)$$

Now by examine the coefficients of equations (3.20) and (3.21), the general expressions for the n^{th} section can be given as:

$$v_n = ni_oR_{eff} + i_oR_L + \rho_oCR_{eff}^2\sum_{k=0}^{n-1}k(n-k) + \rho_oR_{eff}R_L\sum_{k=0}^{n-1}k \quad (3.22)$$

$$i_n = i_o + p_oCR_{eff}\sum_{k=0}^{n}k + np_oCR_L \quad (3.23)$$

For infinite number of sections in an RLC line and considering limits when $n \to \infty$, $n \to (n-1)$to $(n+1)$, and $nR_{eff} = R_T + 0.36Z_0 = R_{Teff}, nC = C_T$, where R_{Teff} and C_T are the total line effective resistance and capacitance respectively. Equations (3.22) and (3.23) can then be rewritten as:

$$v_n = i_oR_{Teff} + i_oR_L + \rho_o\frac{C_TR_{Teff}}{2}.\frac{R_{Teff}}{3} + \rho_o\frac{C_TR_{Teff}}{2}.R_L \quad (3.24)$$

$$i_n = i_o + \rho_o\frac{C_TR_{Teff}}{2} + \rho_oC_TR_{Teff}. \quad (3.25)$$

From **Fig. 3.7** the input current i_i can be written as:

$$i_i = i_n + \frac{v_n}{R_S} \quad (3.26)$$

By solving equation (3.25) using equation (3.24) and (3.26), leads to:

$$i_o = {}^{\mathrm{i_i}}\Big/\left(1+\frac{\mathrm{R_{Teff}}+\mathrm{R_L}}{\mathrm{R_s}}\right) - \frac{\rho^{\frac{\mathrm{R_{Teff}}\,\mathrm{C_T}}{2}}\left(1+\frac{2\mathrm{R_L}}{\mathrm{R_{Teff}}}+\frac{\mathrm{R_{Teff}}+3\mathrm{R_L}}{3\mathrm{R_s}}\right)}{\left(1+\frac{\mathrm{R_{Teff}}+\mathrm{R_L}}{\mathrm{R_s}}\right)}.$$

(3.27)

For a linear- ramp input signal $i_i = \mathrm{p_i t}$, with $\mathrm{p_i}$ the input current slope.It can be seen that equation (3.27) has a linear ramp part and a constant part. Hence, by using equation (3.15) and (3.27), ρ_o can be calculated as

$$\rho_o = \frac{\mathrm{p_i}}{\left(1+\frac{\mathrm{R_T}+\mathrm{R_L}}{\mathrm{R_S}}\right)}$$

(3.28)

By substituting equation (3.28) in equation (3.27) gives

$$i_o = \frac{\mathrm{R_s}}{\mathrm{R_s}+\mathrm{R_{Teff}}+\mathrm{R_L}}.\mathrm{p_i}.\left\{\mathrm{t}-\frac{\mathrm{R_{Teff}}\,\mathrm{C_T}}{2}.\frac{\left(\mathrm{R_s}+\frac{\mathrm{R_{Teff}}}{3}+\mathrm{R_L}\left(1+\frac{2\mathrm{R_s}}{\mathrm{R_{Teff}}}\right)\right)}{(\mathrm{R_s}+\mathrm{R_{Teff}}+\mathrm{R_L})}\right\}$$

(3.29)

Equation (3.29) has the general form given by:

$$i_o(t) = \mathrm{A_i}.\,\mathrm{i_i}(\mathrm{t}-\delta\mathrm{t}) \tag{3.30}$$

Where A_i is the current attenuation andδtis the delay of the output current with respect to the case where $\mathrm{C_T} = 0$.

From equations (3.29) and (3.30), the delay of the output current δt is given as

$$\delta\mathrm{t} = \frac{\mathrm{R_{Teff}}\,\mathrm{C_T}}{2}.\frac{\left(\mathrm{R_s}+\frac{\mathrm{R_{Teff}}}{3}+\mathrm{R_L}\left(1+\frac{2\mathrm{R_s}}{\mathrm{R_{Teff}}}\right)\right)}{(\mathrm{R_s}+\mathrm{R_{Teff}}+\mathrm{R_L})}$$

(3.31)

The output voltage v_o can be given as:

$$\mathrm{v_o}(\mathrm{t}) = \mathrm{i_o}(\mathrm{t}).\mathrm{R_L} = \mathrm{A_i}.\mathrm{R_L}.\mathrm{i_i}(\mathrm{t}-\delta\mathrm{t}) \tag{3.32}$$

It is seen that the delays of the output current and output voltage are equal, therefore represent the general delay.

For a given source configuration there is a choice of the load circuit to be either a voltage-mode or a current-mode circuit. In the case of voltage-mode it follows from equation (3.29) to (3.32) where load resistance is infinite, ($\mathrm{R_L}$infinite)as reported in [21].

$$\mathrm{v_o}(\mathrm{t}) = \mathrm{R_s}.\mathrm{i_i}(\mathrm{t}-\delta\mathrm{t_v})$$

where,

$$\delta t_v = \frac{R_{Teff} C_T}{2} . \left(1 + \frac{2R_s}{R_{Teff}}\right)$$

(3.33)

$$\delta t_v = \frac{(R_T + 0.36Z_0)C_T}{2} . \left(1 + \frac{2R_s}{R_T + 0.36Z_0}\right)$$

For current mode interconnects load resistance is reported in research paper [21] that $(R_L = 0)$ then the output current is equivalent to:

$$i_o(t) = \frac{R_s}{R_s + R_{Teff}} . i_i(t - \delta t_i)$$

(3.34)

Substituting the value $R_{Teff} = R_T + 0.36Z_0$, gives

$$\delta t_i = \frac{R_{Teff} C_T}{2} . \left(\frac{R_s + \frac{R_{Teff}}{3}}{R_s + R_T eff}\right)$$

(3.35)

$$\delta t_i = \frac{(R_T + 0.36Z_0)C_T}{2} . \left(\frac{R_s + \frac{(R_T + 0.36Z_0)}{3}}{R_s + (R_T + 0.36Z_0)}\right)$$

(3.36)

It is seen from equation (3.36) that δt_i is a function of total line capacitance and resistance including inductance effect in terms of characteristic impedance.

The various results obtained for validation of the proposed model for current mode signalling. Long interconnect lines are presented& discussed in this section. The implications of the results are also measured. $R_{Teff} C_T$ (RLC equivalent) interconnect line is analyzed and simulated for different lengths of interconnect. The number of sections N for distributed interconnect line is taken to be 1000 as reported in research paper [28]. During simulation $R_S = 2.5k$ and values of R_L ranges from 10 Ωto 400 Ω forcurrent mode (CM) and 1k Ω to 1MΩ for voltage mode (VM) is taken. Input signal is a linear ramp signal, of 1.8V for the analysis. The values of R, L, C interconnect lines are obtained from Predictive Technology Model (PTM) for 180nm technology as reported in research paper [25]. The design specifications for global interconnect are specified in **Table 3.1.** Simulation results are obtained using SPICEEDA tool and MATLAB 2011.

Table3.1 Dimension & Design Specification for Interconnect

Interconnect	Width (μm)	Space (μm)	Thickness (μm)	Height (μm)	Resistivity (μohm-cm)(Cu)
Global	0.80	0.80	1.25	0.65	ρ = 2.2

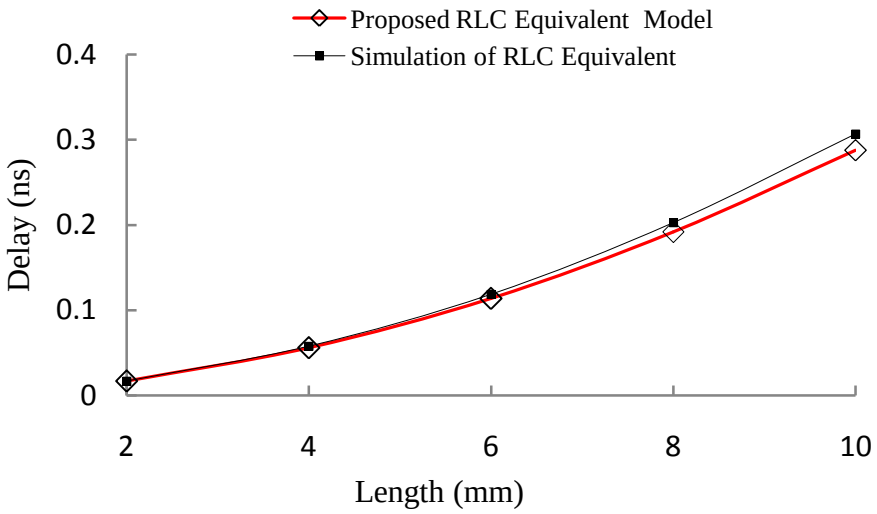


Fig. 3.8 Variation of delay with interconnect length

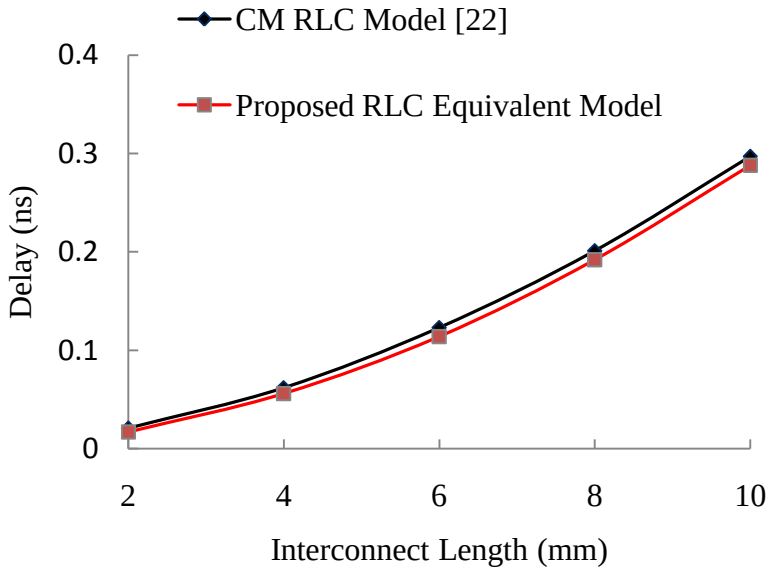


Fig. 3.9 Variations of Delay with Interconnect Length for Proposed RLC and Comparison with Existing Model.

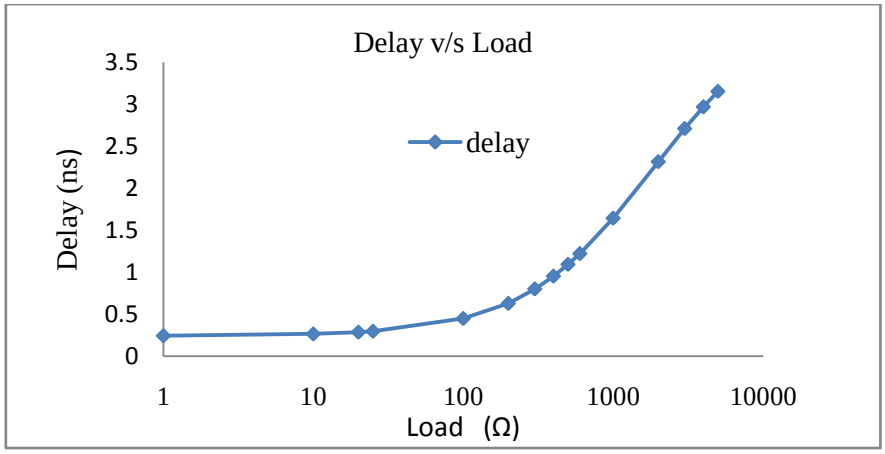


Fig. 3.10 Variations of Delay with Interconnect Length for Proposed RLC and comparison with Existing Model.

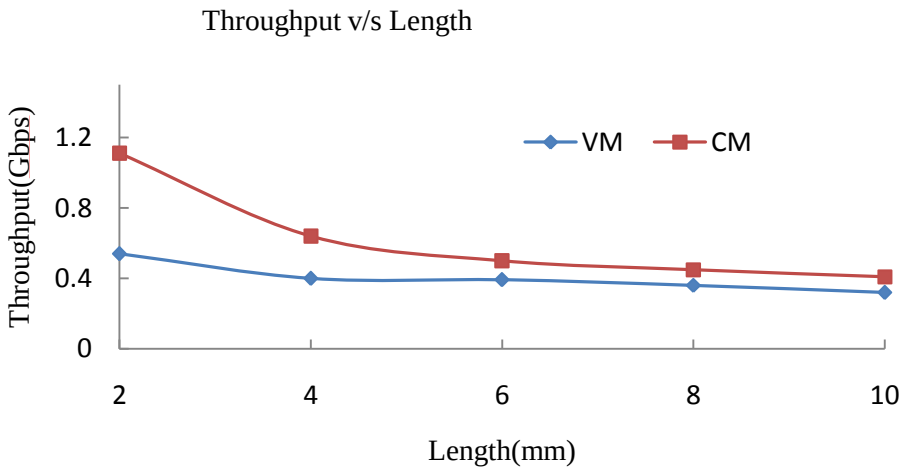


Fig. 3.11 Throughput variation with the length of interconnect

The simulation and analytical results deviates maximum by average error 6.59%, from **Fig 3.8.** For 4mm to10mm interconnect line length the delay response varies by nearly 1.01%. For smaller value of load impedance, it provides smaller delay as shown in Fig 3.10.CM signalling provide a higher value of throughput in the range of Gbps and it decreases with the length of interconnect. **Table 3.2** presents the simulation and analytical results of delay analysis of voltage mode and current mode interconnects. With increase in the length of interconnect the total resistance R_{Teff} of the line increases. As a result δt_i in equation (3.36) will also increase which verified by simulation results shown in **Table 3.2.** There is always probability of increase in error when data is transmitted over long length interconnects. Whereas same error tends to zero for smaller length of interconnect. Consequently, it is

justified that the proposed model is applicable for intermediate and global interconnects. **Fig.3.10** shows the variation of delay with interconnects length. It has been observed that delay increases with length of interconnect. This is in accordance with the analytical model given by equation (3.36). A very good agreement is seen between the analytical and SPICE simulation results. From **Fig. 3.8** it is observed that delay obtained is lesser in case of proposed RLC interconnect when it is compared to results reported in research paper [22]. This improvement in delay factor is because of moment approximation method is used in research paper [22] while the proposed model overcomes the approximation. Inductive effect is more prominent at longer length of interconnect. The rise of delay due to inductance is because inductance does not allow sudden change of current on line. As result delays due to RLCinterconnect line is higher as depicted in **Table 3.2.**

Further it is analyzed that current mode signaling is superior to voltage mode signaling with respect to the following parameters

i. An increase in signaling bandwidth
ii. Reduction in interconnection latency.

It is seen from column 7 and 8 of **Table 3.2** that current mode interconnects are faster compared to voltage mode interconnects.

Table.3.2 Simulation versus Analytical Delay Results

N (distributed interconnect line) =1000 [21-22]$R_s = 2.5\text{k}\Omega, R_L = 10\Omega$ to 400Ω (CM), $1\text{k}\Omega$ to $1\text{M}\Omega$ (VM), $V_{in} = 1.8$ for 180nm node.

Line length (mm)	$R_T(\Omega)$	C_T (pF)	L_T (nH)	$R_S(\text{K}\Omega)$	$R_{Teff}(\Omega)$ [R. d + $0.36Z_0$]	Delay (ns) δt_i[22]	Proposed Analytical Model Delay(ns)	Simulation Results Delay(ns)
2	44	0.487	3.23	2.5	73.318	0.021	0.017	0.017
4	88	0.975	7.015	2.5	118.53	0.062	0.056	0.058
6	132	1.462	11.00	2.5	163.226	0.123	0.114	0.119
8	176	1.950	15.14	2.5	207.72	0.201	0.192	0.203
10	220	2.437	19.37	2.5	252.09	0.297	0.288	0.307

Further the proposed model is compared and verified with ELMORE delay with different set of design parameters.

3.3.1 Results For Model I $R_{eff}C_T$ with Comparison to Elmore Delay Model (In Voltage Mode)

When $R_{eff}C_T$ Model I is compared with Elmore delay model column 3 with column 4 the relative average error between them is 1.01% where as maximum error is 1.7% and minimum is 0.49% for 2mm to 10mm length of interconnect. By using the proposed approach $R_{eff}C_T$ model generates the equivalent results to Elmore Model [22-33] on comparison. When further analytical and simulation results of the proposed model compared.

Table 3.3 Comparison of Proposed Equivalent Model with Various Existing Model N=1000, $(R_s = \mathbf{9\Omega} - 3k\Omega), R_L = 10\Omega - \mathbf{10k\Omega}$, (VM), $C_L = 20fF - 1pF$, $T = 10ns, t_r = t_f = 10ps(\mathbf{C_s = C_L = 0}$ in ideal case for VM)

Length (mm)	Analytical Delay **Moment Matching** [22]	Analytical Delay **Elmore Model** [33]	**This work Analytical Delay $R_{eff}C_T$**	**Simulation of $R_{eff}C_T$ Delay Model**	**Simulation of Actual RLC**	% of R. Error Col.3 /Col.4 with Elmore	% of Error Simulation versus analytical Col.4/col.5	% Dominance of inductance effect at smaller length
2	18ps	18ps	18ps	29ps	45ps	1.4	61	55
4	58ps	57ps	58ps	74ps	94ps	1.7	27	27
6	119ps	119ps	120ps	136ps	146ps	0.84	13	7.3
8	201ps	203ps	204ps	213ps	205ps	0.49	4.4	3.7
10	304ps	307ps	309ps	305ps	264ps	0.65	1.31	13

It is observed that the error for smaller length is greater than the longer lengths. It remains within the range of 3% for longer length whereas for smaller length the average error is 33%. It is not suitable for smaller length. Its suitability is better for longer length of interconnects. Similarly the dominance of inductance effect is large for smaller length of interconnect, whereas for global length the inductance effect remains to be very small for 6 to 10mm length of interconnect i.e. within the average dominance of 8%. But for smaller length inductance effect is highly dominant as shown in **Fig 3.12**(2mm) and for longer length shown in **Fig. 3.13** (10mm).

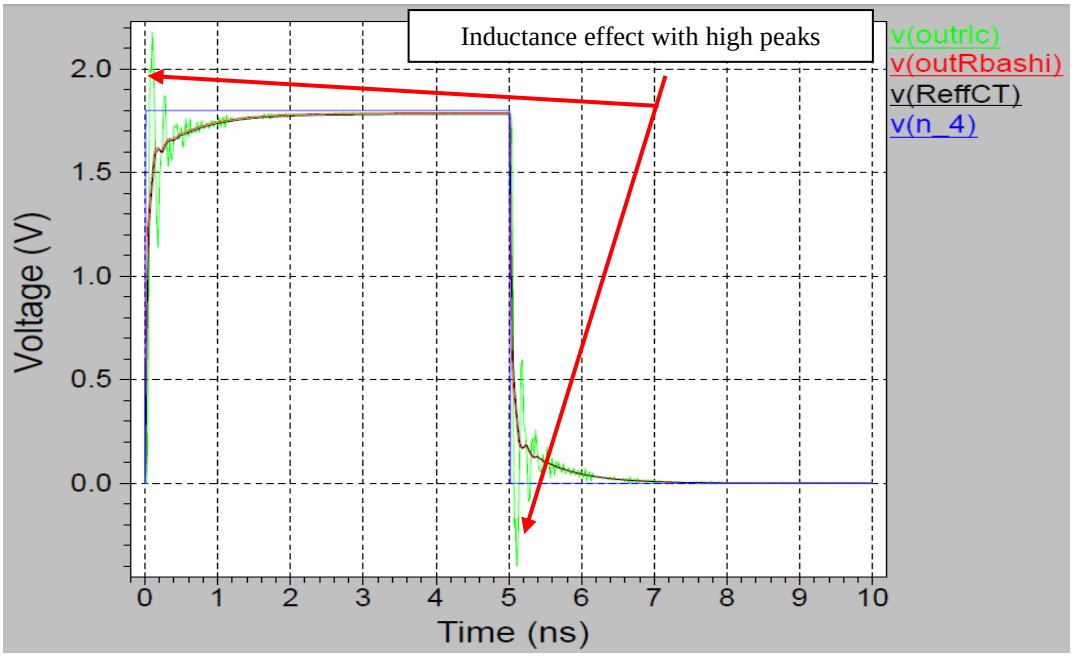


Fig. 3.12 Inductance effect dominance at 2mm length of distributed interconnect

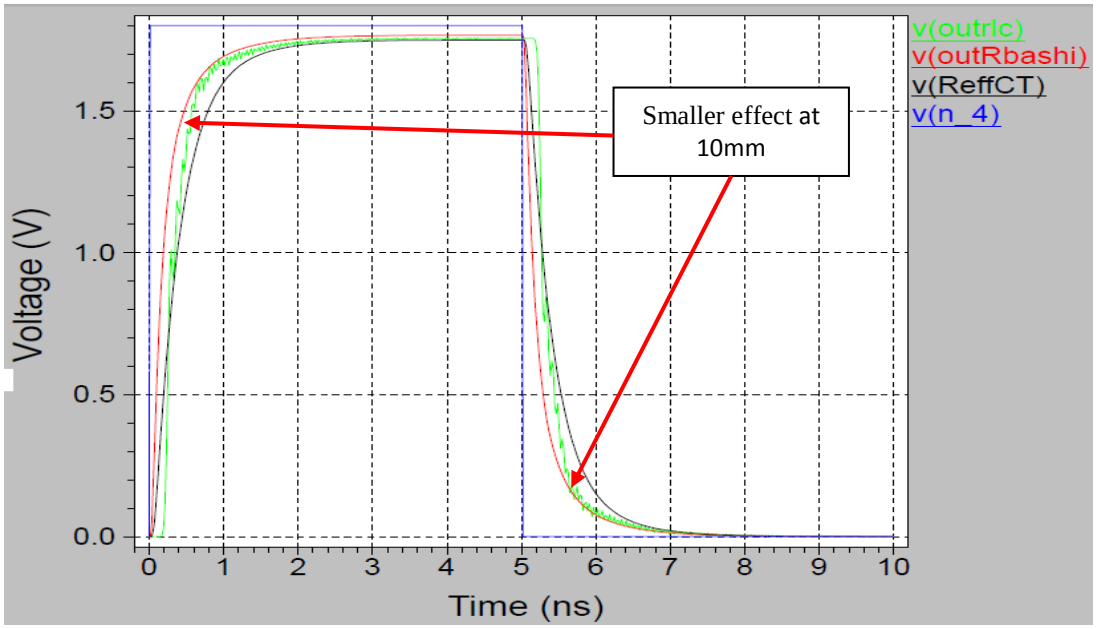


Fig. 3.13 Inductance effect at 10mm length of distributed interconnect.

This is due to that at longer length line becomes highly resistive ($R_{wire} + R_s > jwL$) as shown in **Fig. 3.13** whereas at smaller length $R_{wire} + R_s \leq jwL$, line become inductance dominant shown in **Fig. 3.12.** Further we discuss and implement the parameters, which minimize the inductance effect in wire. Spikes overshoots and undershoots comparisons in Actual RLC & proposed $R_{eff}C_T$ Model I is shown in **Fig. 3.14** In the next section objective will be, to make the model more accurate with the help of inclusion of

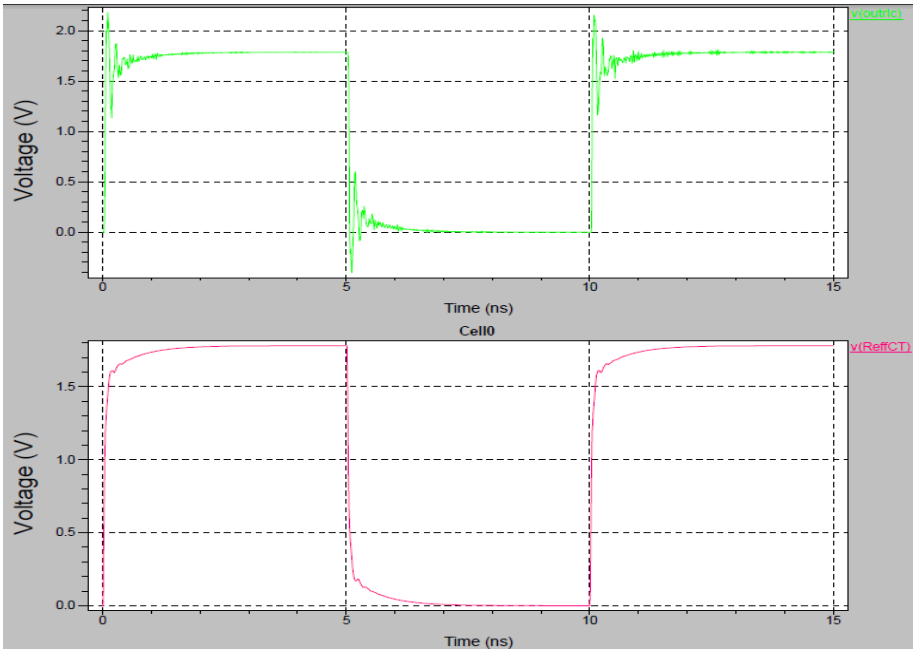


Fig. 3.14 Spikes overshoots and undershoots are reduced by proposed model R_{eff} C_T.

effect of parasitic load impedance. So that model will become more accurate structure. The equation in (3.31) will modify and this will becomes delay model for resistive and capacitive load. Variation of delay with load capacitance for minimization of error between actual RLC and

$$\delta t = \frac{R_{Teff}\, C_T}{2}.\frac{(R_s+\frac{R_{Teff}}{3}+R_L(1+\frac{2R_s}{R_{Teff}}))}{(R_s+R_{Teff}+R_L)} + R_{Teff}\, C_L \qquad (3.37)$$

R_{eff} C_T model presented below. This simulative sweep analysis (SSA) provides a clear picture about the error between the two models shown in **Fig. 3.15**.

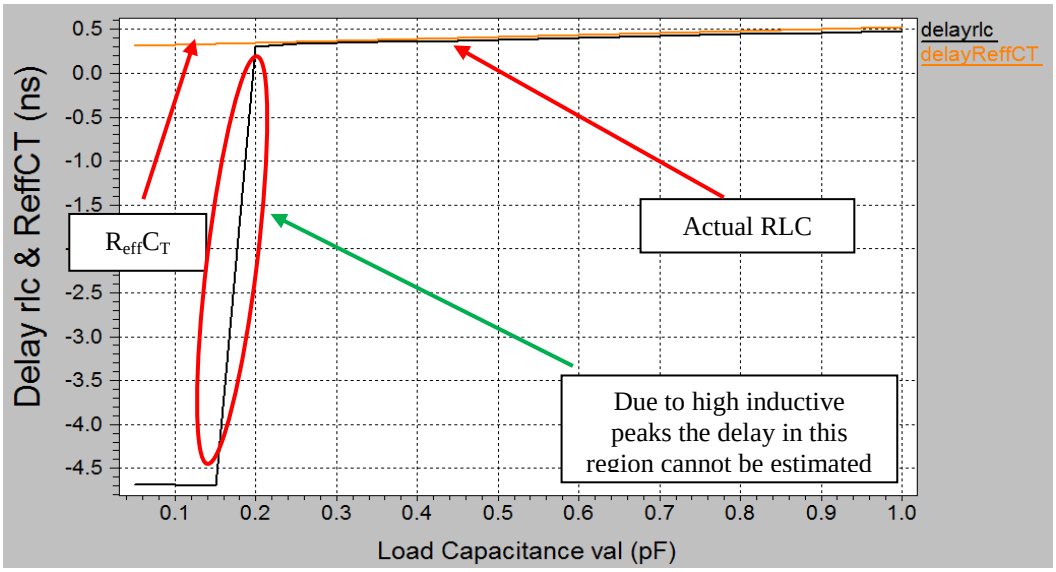


Fig. 3.15 Delay variation of proposed model with load capacitance.

The result of **Fig. 3.15** in zoom format is available below for identification of error between actual RLC & proposed $R_{eff}C_T$ Model I two models shown in **Fig. 3.16**.

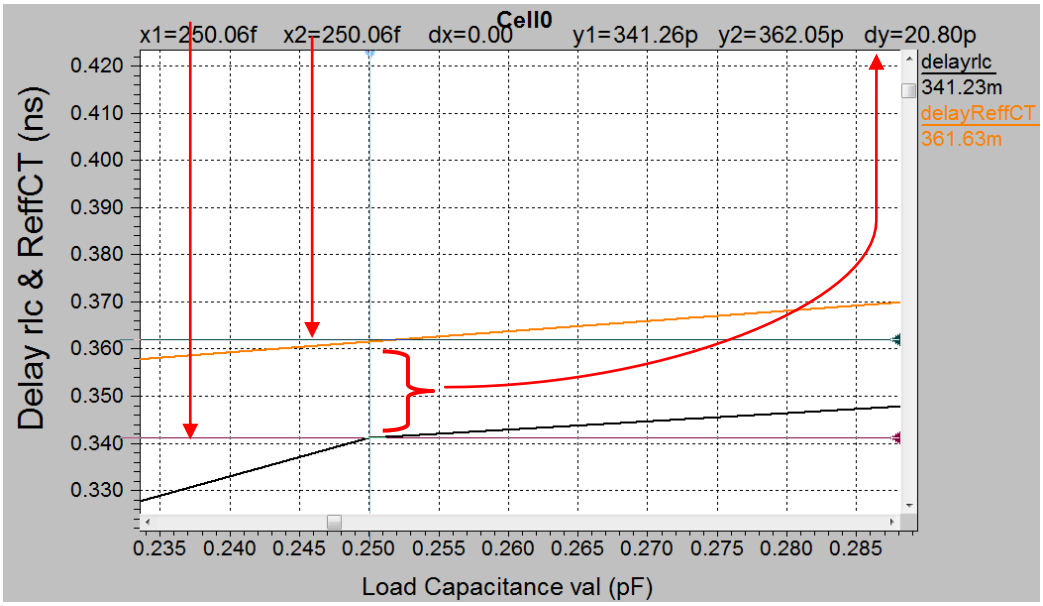


Fig. 3.16 Simulative differential error between the $R_{eff}C_T$ Model and Actual RLC at 250fF.

Table3.4 Model Validation with Capacitive Load and Minimization of Dominance of Inductance effect at $C_L = 250fF, R_s = 9\Omega, C_S = 0$

Length (mm)	Modified Analytical Model R_{eff} C_T (3.37)(ps)	Simulation of Modified R_{eff} C_T Model (ps)	Simulation of Actual RLC Model (ps)	% of Diff..Error between col.2 and col.3	% of R. Error between Col.4 & Col.3
2mm ($C_L = 250fF$)	36.32	50	61	37	22 ↑
2mm ($C_L = 680fF$)	68ps	87.96	87.96	27	NIL
10mm	372	361	341	2.9	5.5

Table 3.4 model again depicts better suitability for global length of interconnects say for 10mm length with differential error of 2.9% between simulation and analytical model whereas without load capacitance inclusion in model, this error was approximately 8%. Now this has reduced drastically. It means that model is becoming more accurate with physical structure. Further show 5.5% of relative error between actual RLC model and Simulated $R_{eff}C_T$. It means smaller inductive effect or dominance. But for smaller length of interconnect it has reduced up to 22% whereas without load capacitance assumption, it was approximately

55% as in table 3.3 for 2mm length of interconnect. Hence, all the above results are verified for voltage mode interconnects.

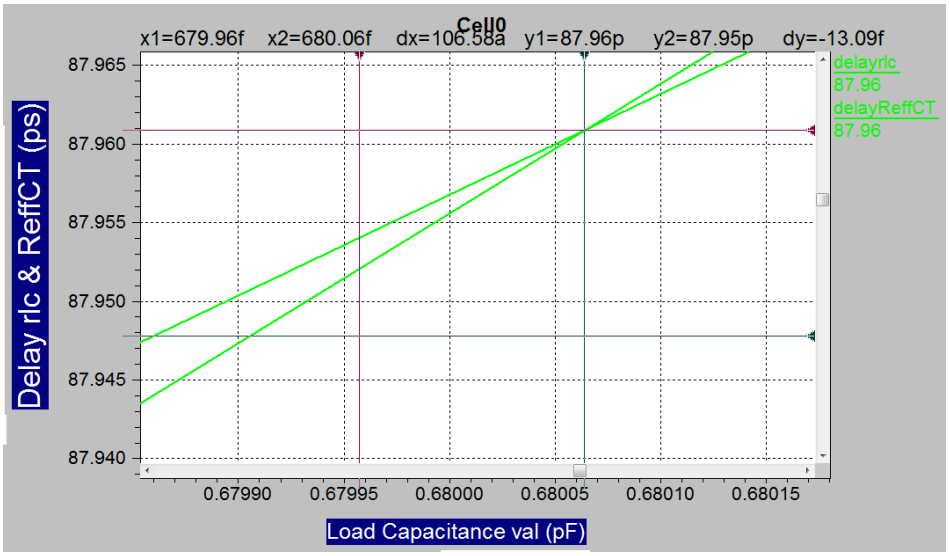


Fig. 3.17 For 2mm length of interconnect the point of intersection where both the $R_{eff}C_T$ and Actual RLC model match to each other.

For 2mm length of interconnect both $R_{eff}C_T$ Model I and Actual RLC Model match to each other for load capacitance value of 680fF and shown in **Fig. 3.17** and shows approximately minimum error between simulation models but analytical model is deviated by 27% form simulation model as shown in **Table 3.4.**Source Capacitance Dependency is negligible on distributed interconnect line delay as shown in **Fig. 3.18** for 2mm length of interconnect.

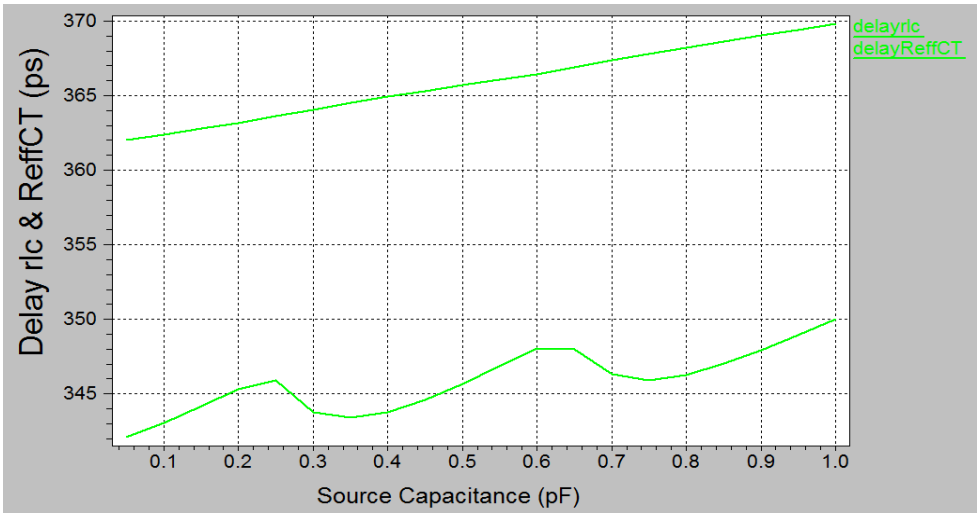


Fig. 3.18 Simulative verification of source capacitance effect on $R_{eff}C_T$Model I and actual RLC model.

The results presented in **Table 3.3** are equivalent to Elmore Delay at global length and comparisons with existing model reported in research paper [22] are presented.

3.3.2 Model Discussion and Verification for Current Mode System

Here, in this part the $R_{eff}C_T$ model has been verified and compared with existing model for current mode signaling.

Table 3.5 Comparison of Proposed Equivalent Model with Various Existing Model N=1000, $(R_s = 10\Omega - 3k\Omega), R_L = 50\Omega, C_L = 20fF - 1pF (R_L = 0$ in ideal case for Current Mode)

Length (mm)	$R_T(\Omega)$	C_T (F)	L_T (H)	$R_{eff}(\Omega)$	Analytical Delay Moment Matching by Zhou[22]	Analytical Delay Sakurai Model [107]	**This work Analytical Delay $R_{eff}C_T$**	**% Decrease of Delay Col.8 v/s 6**
2	44	0.487p	3.23n	73.318	6ps	13ps	5ps	16
4	88	0.975p	7.015n	118.53	19.3ps	42ps	19ps	1.55
6	132	1.462p	11.00n	163.266	39.8ps	88ps	39ps	2.01
8	176	1.950p	15.14n	207.72	68ps	150ps	67ps	1.47
10	220	2.437p	19.37n	252.09	104ps	227ps	102ps	1.92

When the proposed model are compared with the results of existing models in research paper [22] it is found that the CM signalling delay decrease for all length (2mm to 10mm) by an average value of 4.59% whereas for 4mm to 10mm length the results of proposed model in Current mode signaling decreased by average value of 1.73% to [22].

When compared the delay value of proposed model Current Mode system to Sakurai Delay [30], [107], it has been observed that delay due to current mode (CM) system is 2.22 times smaller for longer length of interconnect, CM signaling is highly suitable for Longer length of interconnects. In this section the comparison for throughput is discussed for both voltage and current signaling in **Table 3.6.**

Table 3.6 Comparison of Voltage & Current Mode for Delay & Throughput for Proposed Model

Length (mm)	VM Delay(ps)	CM Delay(ps)	% Decrease in Delay	Throughput VM(Gbps)	Throughput CM (Gbps)	% Increase in Throughput
2	18	5	72	55	200	263
4	58	19	67	17	52	205
6	120	39	67	8	25	212
8	204	67	67	4	14	250
10	309	102	67	3	9	200

CM delay has decreased upto 67% when compared to voltage mode signaling and this increment remains almost same for 2mm to 10mm length of line as shown in **Table 3.6**Hence, the throughput by using the current mode system has increased maximum by 263% for 2mm length of line whereas for 10mm line it is increased by 200% as shown in **Table 3.6.**

By using current Mode signaling the throughput has reached upto the value of 9Gbps for 10mm line whereas 2mm line it becomes 200Gbps. There is a huge increment in throughput. This is due to the fact that with the length throughput always decrease is as justified in **Table 3.6.**

3.4 Proposed Model II(R_0C_0): i.e. RLC Equivalent R_0C_0 Model for Current Mode (CM) & Voltage Mode(VM) Scheme

In this section the RLC interconnect line is forced by a CMOS inverter shown in **Fig. 3.19** for the duration of $0 < t < T_P$,whereas T_P is the time needed for the signal to propagate a distance equal to the length of interconnects line. T_P is generally defined as the time of flight of the interconnect line. The input signal is taken as a ramp with finite rise and fall time t_r (t_f). The formulation is started with the basic wave equation having γ as propagation constant. α and β are defined as attenuation constant and phase constant respectively. After separating real and imaginary part the attenuation constant is estimated by replacing $\mu\epsilon = \mathrm{LC}$ and $\sigma/\epsilon = \mathrm{R/L}$ in equation (3.43). Normalized asymptotic value for attenuation constant is given by equation (3.45).

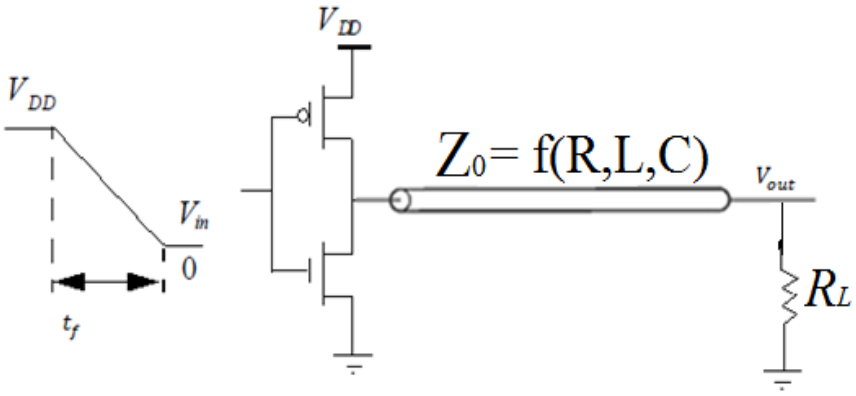


Fig. 3.19 CMOS drive a interconnect line with load resistance

The attenuation constant α of an RLC transmission line can be derived from the basic equations. We know that the

$$\gamma^2 = j\omega\mu\,(\sigma + j\omega\varepsilon) \tag{3.38}$$

where γ is propagation constant.

$$\text{We know that } \gamma = \alpha + j\beta \tag{3.39}$$

Squaring the equation (3.39) ,we get

$$\gamma^2 = \alpha^2 - \beta^2 + 2j\alpha\beta \tag{3.40}$$

Real part of equations (3.38) and (3.40) are compared

$$\text{Re}(\gamma^2) = \alpha^2 - \beta^2 = -\omega^2\mu\varepsilon \tag{3.41}$$

By taking the Mode of equation (3.38)

$$\gamma^2 = jw\mu\sigma - \omega^2\mu\varepsilon$$

$$|\gamma^2|^2 = (\omega\mu\epsilon)^2 + \omega^4(\mu\epsilon)^2$$

$$\gamma^2 = \omega\mu\sqrt{\sigma^2 + (\omega\epsilon)^2}$$

$$\alpha^2 + \beta^2 = \omega\mu\sqrt{\sigma^2 + (\omega\epsilon)^2} \tag{3.42}$$

Adding equations (3.41) and (3.42), we get value of α

$$\alpha = \omega\sqrt{\left(\frac{\mu\epsilon}{2}\right)\left[\sqrt{\left(1 + \left(\frac{\sigma}{\omega\epsilon}\right)^2\right)} - 1\right.} \tag{3.43}$$

Substitute$\mu\epsilon = LC$ and $\sigma/\epsilon = R/L$ in equation (3.43) , we get

$$\alpha = \omega\sqrt{LC}\sqrt{\frac{1}{2}\left(\sqrt{\left(1 + \left(\frac{R}{\omega L}\right)^2\right)} - 1\right.} \tag{3.44}$$

where R , L and C are the per unit length of line , respectively and ω is the radial frequency. The attenuation constant is shown to saturate with increasing frequency to an asymptotic value given by

$$\alpha_{asym} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{3.45}$$

The radial frequency after that it becomes constant

$$\omega_{asym} = R/L$$

The Characteristic impedance Z_0 of an RLC interconnect line is complex with negative and imaginary parts. Therefore, the characteristic impedance looks like a resistance in series with a capacitance. Hence, the characteristic impedance can be expressed as

$$Z_0 = R_0 - j\frac{1}{\omega C_0} \tag{3.46}$$

$$R_0 = \sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1 + \left(\frac{R}{\omega L}\right)^2\right)} + 1\right)} \tag{3.47}$$

$$C_0 = \frac{1}{\omega\sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1 + \left(\frac{R}{\omega L}\right)^2\right)} - 1\right)}} \tag{3.48}$$

$$Z_0 = R_0 - j\frac{1}{\omega C_0} \tag{3.49}$$

Both R_0 and C_0 concentrated to the asymptotic magnitude given as

$$R_{0asym} = \sqrt{\frac{L}{C}} \tag{3.50}$$

$$C_{0asym} = \frac{2\sqrt{LC}}{R} \tag{3.51}$$

We know that

$$Z_0 = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-} = \frac{R + j\omega L}{\gamma} = \frac{\gamma}{G + j\omega C} = \frac{\alpha + j\beta}{G + j\omega C} \tag{3.52}$$

Let assume $G = 0$,

$$Z_0 = \frac{\alpha + j\beta}{j\omega C} = \frac{\alpha}{j\omega C} + \frac{\beta}{\omega C} = \frac{\beta}{\omega C} - j\frac{\alpha}{\omega C}$$

$$Z_0 = \frac{\beta}{\omega C} - j\frac{\alpha}{\omega C} \tag{3.53}$$

Also we know that

$$Z_0 = R_0 - j\frac{1}{wC_0} \tag{3.54}$$

By comparing real and imaginary parts we have interconnect line in terms of R_0, C_0

$$R_0 = \sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1+\left(\frac{R}{\omega L}\right)^2\right)}+1\right)} \tag{3.55}$$

$$C_0 = \frac{1}{\omega\sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1+\left(\frac{R}{\omega L}\right)^2\right)}-1\right)}} \tag{3.56}$$

Hence, we will distribute these R_0, C_0 along the length of line and replace R_{Teff} by R_0 and C_T by C_0 in equation (3.31) of Proposed Model I ($R_{eff}C_T$), Then the New formulation for delay model of **RLC Equivalent R_0C_0 Model II** will come, which derived further for Voltage mode and Current mode signalling

$$\delta t = \frac{R_0C_0}{2}.\frac{\left(R_s + \frac{R_0}{3} + R_L\left(1+\frac{2R_s}{R_0}\right)\right)}{(R_s + R_0 + R_L)} \tag{3.57}$$

For VM signalling:-

$$\delta t_v = \frac{R_0C_0}{2}.\left(1+\frac{2R_s}{R_0}\right) \tag{3.58}$$

$$\delta t_v = \frac{\left(\sqrt{\frac{L}{C}}2\frac{\sqrt{LC}}{R}\right)}{2}.\left(1+\frac{2R_s}{\left(\sqrt{\frac{L}{C}}\right)}\right) = \frac{L}{R}\left(1+\frac{2R_s}{\left(\sqrt{\frac{L}{C}}\right)}\right) \tag{3.59}$$

For CM signalling:-

$$\delta t_i = \frac{R_0C_0}{2}.\left(\frac{R_s+\frac{R_0}{3}}{R_s+R_0}\right) \tag{3.60}$$

$$\delta t_i = \frac{L}{R}.\left(\frac{R_s+\frac{\left(\sqrt{\frac{L}{C}}\right)}{3}}{R_s+\left(\sqrt{\frac{L}{C}}\right)}\right) \tag{3.61}$$

From the proposed **Model II R_0C_0** the equations (3.59) and (3.61) provides the interconnect line delay for both voltage and current mode signaling respectively. Both the line delays are dependent on R, L, C and source resistance of driver circuit i.e. R_s . The various results are estimated on the basis of proposed model in equations (3.59)& (3.61).

3.4.1 Results Computed for Voltage Mode Signalling

The proposed Model II R_0C_0 compared with the existing model for VM signaling gives the superior performance than the other existing models at longer length. For longer lengths the results of proposed model are compared with the mathematical delay models presented in research papers of Rbashi [21] in which RC line are expressed with the help of state equations using the approach of modified nodal matrix (MNA) and for obtaining effective resistance and capacitance by applying first order AWE approximation.

Zhou research paper presents a closed-form delay formula for on-chip RLC interconnects for current mode signaling. The delay formula reported herein is derived based on the modified nodal analysis formulation and an equivalent lumped model representation of inductance effects. Compared to computationally intensive methods, this method results in a simple yet accurate expression by 'absorbing' the inductance into the RC model using Maclaurin series reported in research paper [22].

R.Kar used the technique of moment matching with effective resistance and capacitance model given by Rbashi in research paper [109]. Murthy presented a closed form model for the computation of finite ramp responses of RLC interconnects in VLSI interconnects. The models was based on extended Eudes model and Scaling and Squaring algorithm which allow numerical estimation of delay in lossy interconnect as reported in research paper [110-111].

The proposed model R_0C_0 delay has decreased by the 25.61% when compared Column 7 (Eudes Model) [110-111] for 10mm line. Shows superior performance at global length when compared to other existing models presented in **Table 3.7.**

Table 3.7 Comparison of R_0 C_0 Model (cal.$R_s = 6\Omega, R_L = 10k\Omega, N = 1000, t_r = 10ps$, with Existing Model$(R_s = 6\Omega - 3k\Omega), R_L = 10\Omega - 10k\Omega, C_L = 20fF - 1pF$ $(C_s = C_L = 0$ in ideal case for VM)

Length (mm)	$R_0(\Omega)$	C_0(pF)	Analytical Delay (Moment Matching+ inductance effect) [22] Zhou **[2005]**	Analytical Delay MNA (Moment Matching+ RBashi) [109] R.kar **[2010]**	Analytical Delay (MNA of RBashi) [21] **[2003]**	Analytical Delay using Eudes model (NS Muthy) [110-111] **[2013,2014]**	**This work Analytical** Delay (Z_0 with Asymptotic Distributed Model) R0C0 Model	**This Work Simulation** of R_0C_0 Delay Model	**% Error**
2	81.43982	1.80	18ps	8ps	10ps	64ps	75ps	76ps	1.3
4	84.82259	1.87	58ps	24ps	23ps	80ps	81ps	82ps	1.2
6	86.77612	1.92	119ps	54ps	52ps	88ps	85ps	87ps	2.3
8	88.11415	1.95	201ps	98ps	92ps	98ps	88ps	90ps	2.2
10	89.15322	1.97	304ps	134ps	133ps	121ps	90ps	96ps	2.2

Further analytical results of proposed Model IIare compared with the SPICE simulations the average error for all length is 1.84%, whereas maximumerror is of 2.3%.In the proposed model the asymptotic value of characteristic impedance are used for estimation of effective resistance and capacitance by exploiting the relationships of α and β is attenuation constant and phase constant respectively. The mathematical formulation developed by the proposed approach results in a superior and better performance and detailed in **Table 3.7**.

3.4.2 Results estimated for Current mode signalling

For Current Mode Signaling the delay of proposed model has decreased upto 53%, 35%, and 20% for 10mm, 8mm, 6mm line whereas for 2mm length & 4mm length line it has increased by 75%, when compared to existing models as detailed in **Table 3.8.**

So the suitability of proposed model is valid for longer length of interconnects (i.e. Top level global interconnects ranges from 15mm- 20mm).

Table 3.8 Comparison of R_0 C_0 Model (cal.$R_s = 6\Omega, R_L = 50\Omega, N = 1000, t_r = 10ps$, with existing model($R_s = 6\Omega - 3k\Omega$), $R_L = 10\Omega - 10k\Omega, C_L = 20fF - 1pF$, ($R_L = 0$ in ideal case for Current Mode),

Length (mm)	R_{eff} (Ω)	C_{eff} (pF)	R_0 (Ω)	C_0 (pF)	Analytical Delay (Moment Matching+ inductance effect) [22] Zhou **[2005]**	Analytical Delay MNA (Moment Matching+R Bashi) [109] R.kar **[2010]**	Analytical Delay (MNA of RBashi) [21] **[2003]**	**Analytical Delay using Eudes model** (NS Muthy) [110-111] **[2013,2014]**	**This work Analytical Delay** (Z_0 with Asymptotic Distributed Model) **R_0C_0 Model II**	% Decrease Of Delay Col.7 v/s Col.10
2	22.26	0.366	81.43	1.80	6ps	5ps	4ps	64ps	24ps	80 ↑
4	36.49	0.725	84.82	1.87	19.3ps	14ps	13ps	80ps	26ps	75 ↑
6	48.86	1.082	86.77	1.92	39.8ps	35ps	28ps	88ps	28ps	20
8	60.46	1.432	88.11	1.95	68ps	45ps	43ps	98ps	29ps	35
10	71.66	1.722	89.15	1.97	104ps	64ps	61ps	121ps	30ps	53

3.4.3 Comparison of VM and CM Delay & Throughput for R_0C_0 Model II

Table 3.9 Throughput and Delay Comparison for Voltage and Current Mode

Length (mm)	**VM Delay(ps)**	**CM Delay(ps)**	**% Decrease of Delay**	**Throughput VM (Gbps)**	**Throughput for CM (Gbps)**	**% Increase in Throughput**
2	75	24	68	13.33	41.66	212
4	81	26	67	12.34	38.46	211
6	85	28	67	11.76	35.71	203
8	88	29	67	11.36	34.48	202
10	90	30	67	11.11	33.33	200

By comparison of CM to voltage mode signaling for the proposed model R_0C_0 it is found that the percentage of decrease of delay remains to be 67% as in the earlier Model I $R_{eff}C_T$.

Throughput for the R_0C_0 in model again to be 200% increase for 10 mm line with the value of throughput 33Gbps for CM (10mm) and it remains maximum upto 42% for 2mm line, whereas the R_{eff} C_T Model I with CM model gives 9Gbps for 10mm line.

With this new (R_0C_0) Model II throughput has increased significantly in comparison to previous approaches.

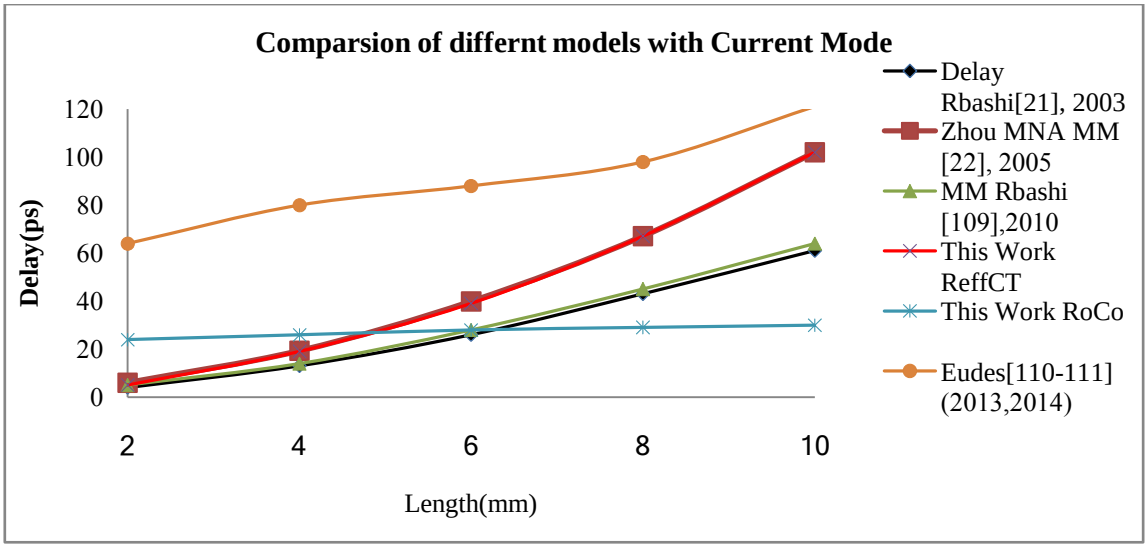


Fig. 3.20 Comparison of different models with current mode.

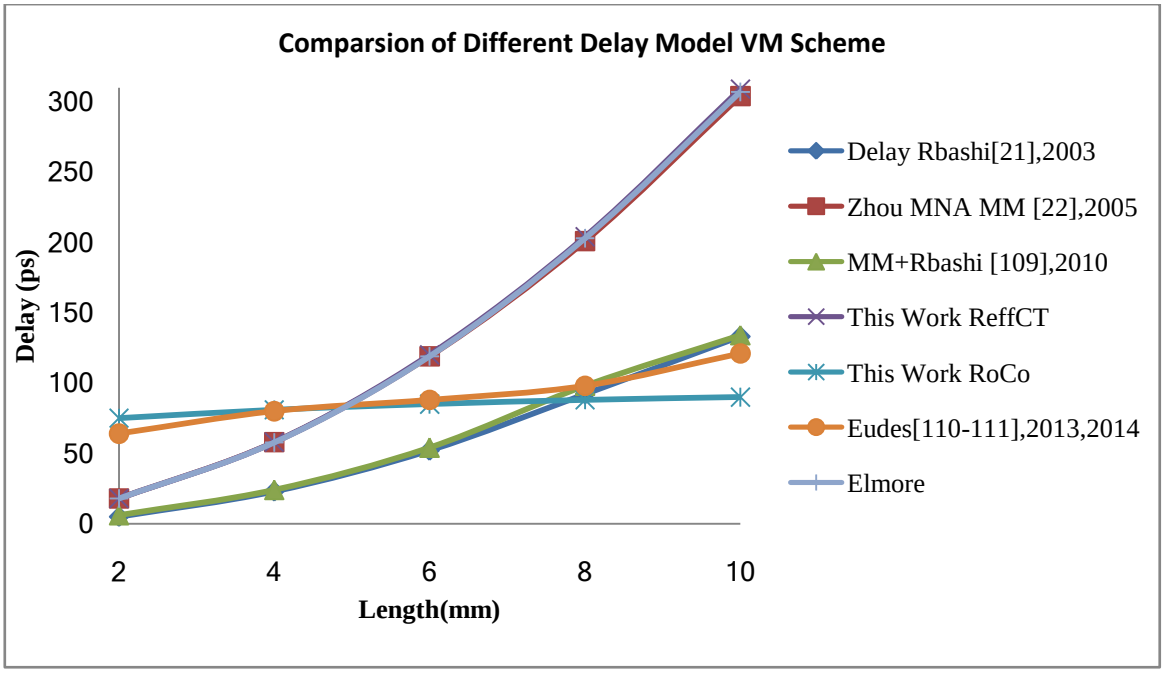


Fig. 3.21 Comparison of different delay models for voltage mode case.

In **Fig. 3.20**and **Fig. 3.21**the proposed model R_0C_0 shows significant performance on comparison to model existing model [21-22] [109-111] for lengths greater than 6mm for voltage mode schemes. So the proposed modeling is significantly applicable for global length of interconnects. In Current Mode Scheme the delay provided is in the range of 30ps clear from **Fig. 3.20** and available with Table 3.8. Throughput increase by 33.33 times than VM signaling as shown in **Table 3.9**.

3.5 Model III Mathematical Model Formulation Using Transmission Line Approach:

In this section a bit line delay is modelled when a read operation performed on CMOS SRAM. Current mode signalling technique is exploited for fast access/transfer of information to data line of any microprocessor/microcontroller. Current mode signalling a system consists of a driver circuitry interconnects line and followed by receiver circuitry having a decoding unit. The problem targeted in this work depicted in **Fig. 3.22**

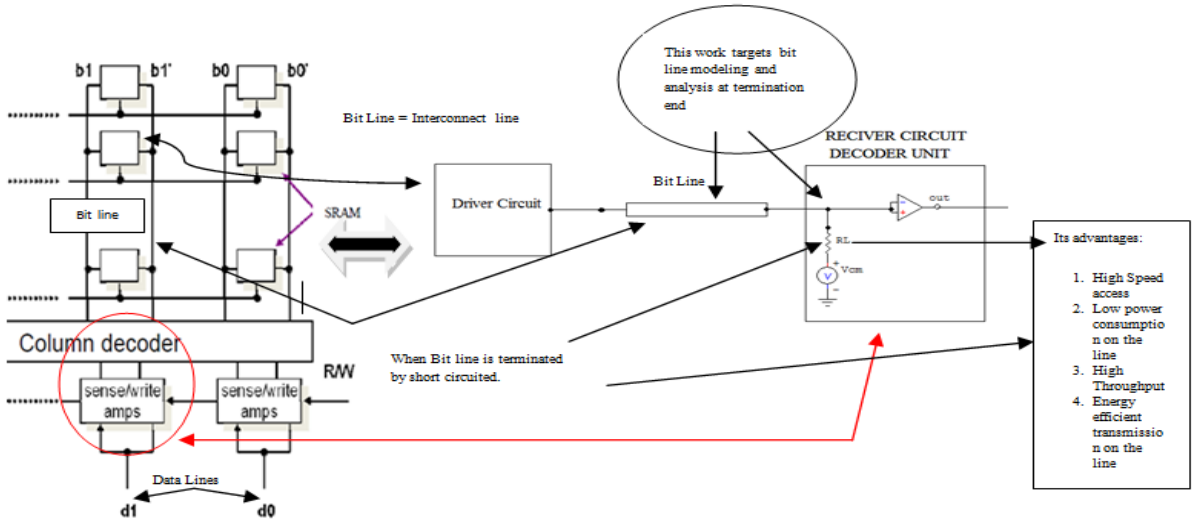


Fig.3.22 Proposed equivalent circuit for SRAM transmitting signal on bit line

For the above proposed distributed *RLC* model for a current mode interconnects is shown in **Fig. 3.23.** Line proposed parameters are designated *R*, *L*, and *C* as unit length resistance, inductance and capacitance respectively, $\Delta \boldsymbol{x}$ is the length of each lumped section and R_S is the source resistance. It is very much clear from literature that current mode signaling differs from voltage mode in that interconnect terminates at a finite resistance in addition to capacitive load. In this work delay model is proposed for resistive load only. As shown in **Fig. 3.23,** the principle of current mode signaling is that by loading the line with finite impedance, the dominant pole of the system shifts and results in a smaller time constant with lesser delay. Long transmission line is modeled as a linear time invariant distributed network. To represent a constant current and voltage on the line the differential equations representation is used, where voltage $V(x,t)$ and $V((x+\Delta x),t)$ and current $I(x,t)$and $I((x+\Delta x),t)$,

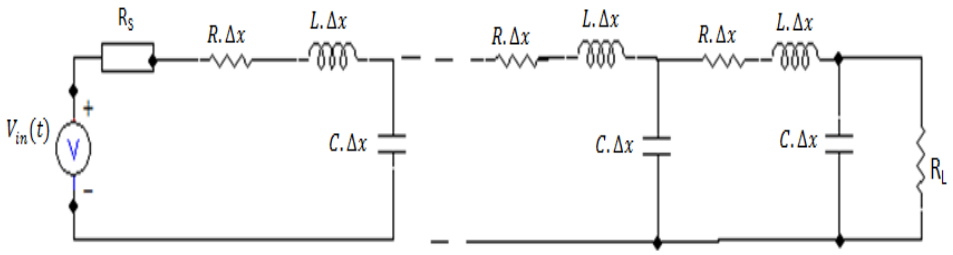


Fig. 3.23 Distributed RLC Interconnect Model with resistive load.

are represented at the source and load ends *at* $x = 0$ and $x = d$ (length of line) respectively. **Fig. 3.24** shows the equivalent distributed *rc* interconnect model. Here $\boldsymbol{r}$ represent unit length equivalent resistance and $\boldsymbol{c}$represent unit length capacitance of the interconnect.

For constant current

$$\frac{V(x,t) - V(x+\Delta x,t)}{r.\Delta x} = I(x,t) \tag{3.62}$$

For $\Delta x \to 0$

$$I(x,t) = -\frac{1}{r}\frac{\partial V(x,t)}{\partial x} \tag{3.63}$$

For constant voltage

$$I(x,t) - I(x+\Delta x,t) = c\Delta x \ \frac{\partial V(x,t)}{\partial t} \tag{3.64}$$

For $\Delta x \to 0$

$$\frac{\partial I(x,t)}{\partial x} = -c\frac{\partial V(x,t)}{\partial t} \tag{3.65}$$

Substituting equation(3.63) into equation (3.64), reduces to

$$\frac{\partial^2 V(x,t)}{\partial x^2} = rc \ \frac{\partial V(x,t)}{\partial t} \tag{3.66}$$

Thus

$\frac{\partial^2 V(x,t)}{\partial x^2} - rc \ \frac{\partial V(x,t)}{\partial t} = 0$ (3.67)

For s- domain representation of equation(3.67) becomes

$$\frac{\partial^2 V(x,s)}{\partial x^2} - rcs\, V(x,s) \quad = 0 \tag{3.68}$$

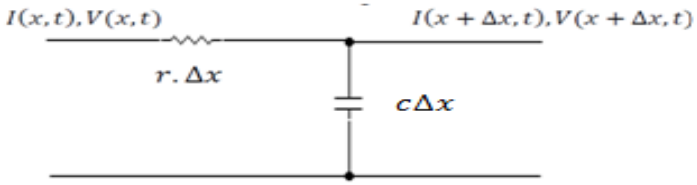


Fig. 3.24 Distributed *rc* interconnect line model.

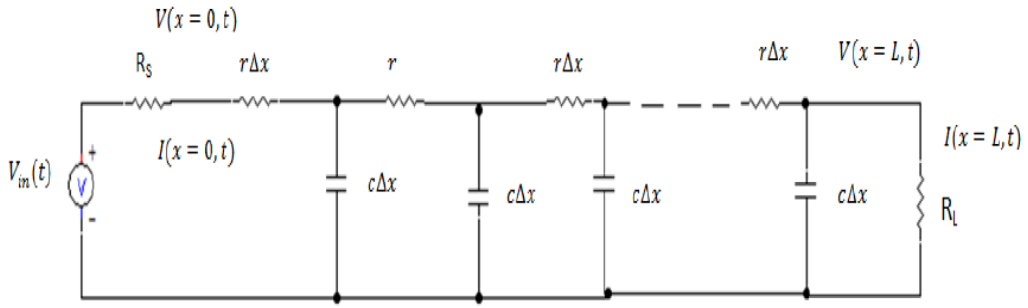


Fig. 3.25 Interconnect line modelled as a distributed line.

Fig. 3.25 gives the *rc* distributed model of an interconnect line. $V_{in}(t)$is the time varying input signal, and R_S is a source resistance with R_L resistive load. $r.\Delta x$and$c.\Delta x$ represent small increments in the value of unit length resistance and capacitance down the interconnect line. The solution of partial differential equation (3.68) in terms of voltage and current on the line is given by

$$V(x,s) = A_{11} sinh(\sqrt{scr}\, x) + B_{11} cosh\,(\sqrt{scr}\, x) \tag{3.69}$$

$$I(x,s) = -\sqrt{\frac{sc}{r}}\ [A_{11} cosh\,(\sqrt{scr}\, x) + B_{11} sinh(\sqrt{scr}\, x)] \tag{3.70}$$

By applying the boundary conditions on equations (3.69) and (3.70), A_{11}, B_{11} with R_L as resistive load termination are obtained. And the boundary conditions are as:

$$V_{in}(s) = V(x = 0, s) + I(x = 0, s) R_S$$

$$V(x = d, s) = I(x = d, s) R_L$$

$$A_{11} = -\frac{V_{in}(s)[cosh\left(\sqrt{scr}\,d\right) + \sqrt{\frac{sc}{r}}R_L\ sinh\left(\sqrt{scr}\,d\right)]}{\left(\frac{sCR_LR_S}{r}+1\right)sinh\left(\sqrt{scr}\,d\right) + \sqrt{\frac{sc}{r}}(R_L+R_S)cosh\left(\sqrt{scr}\,d\right)}$$

$$B_{11} = \frac{V_{in}(s)[sinh\left(\sqrt{scr}\,d\right) + \sqrt{\frac{sc}{r}}R_L\ cosh\left(\sqrt{scr}\,d\right)]}{\left(\frac{sCR_LR_S}{r}+1\right)sinh\left(\sqrt{scr}\,d\right) + \sqrt{\frac{sc}{r}}(R_L+R_S)cosh\left(\sqrt{scr}\,d\right)}$$

Using, the values of A_{11} and B_{11} at the load end equation (3.69) and (3.70) reduce to equation (3.81).

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{\sqrt{\frac{sc}{r}}R_L}{\left(\frac{sCR_LR_S}{r}+1\right)sinh\left(\sqrt{scr}\,d\right) + \sqrt{\frac{sc}{r}}(R_L+R_S)cosh\left(\sqrt{scr}\,d\right)} \tag{3.81}$$

Let $\sqrt{scr}d = u$

Equation (3.81) becomes

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{\frac{u}{dr}R_L}{\left(1+\frac{u^2}{r^2d^2}R_LR_S\right)sinh(u) + \frac{u}{dr}(R_L+R_S)cosh(u)}$$

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{1}{\left(\frac{rd}{uR_L}+\frac{u}{rd}R_S\right)\left(\frac{e^u-e^{-u}}{2}\right) + \left(1+\frac{R_S}{R_L}\right)\left(\frac{e^u+e^{-u}}{2}\right)} \tag{3.82}$$

By rewriting equation (3.81) as:

$$f(u) = \left(\frac{a}{u}+bu\right)\left(\frac{e^u-e^{-u}}{2}\right) + c\left(\frac{e^u+e^{-u}}{2}\right) \tag{3.83}$$

where,

$$a = \frac{rd}{R_L} = \frac{R_1}{R_L},\quad b = \frac{R_S}{rd} = \frac{R_S}{R_1},\quad c = (1+\frac{R_S}{R_L})$$

On simplifying equation (3.83), it gives:

$$f(u) = 1/2[e^{u}\left(\frac{a}{u} + bu + c\right) + (c - bu - \frac{a}{u})e^{-u}$$

(3.84)

By solving equation (3.84), $f(u)$ finally reduces to

$$f(u) = (a + c) + \left(b + \frac{c}{2!} + \frac{a}{3!}\right)u^2 + \left(\frac{b}{3!} + \frac{c}{4!} + \frac{a}{5!}\right)u^4 + \left(\frac{b}{5!} + \frac{c}{6!} + \frac{a}{7!}\right)u^6 + \cdots \ldots \ldots \ldots$$

(3.85)

Substituting the value of

$$u = \sqrt{scr}\, d$$

$cd = C_1$, Total capacitance of interconnect line of length'd'.

$rd = R_1$, Total effective resistance of interconnect line of length'd', and equation (3.85) becomes:

$$f(u) = (a + c) + \left(b + \frac{c}{2!} + \frac{a}{3!}\right)C_1R_1s + \left(\frac{b}{3!} + \frac{c}{4!} + \frac{a}{5!}\right)(C_1R_1)^2s^2$$
$$+ \left(\frac{b}{5!} + \frac{c}{6!} + \frac{a}{7!}\right)(C_1R_1)^3s^3 + \cdots \ldots \ldots \ldots$$

(3.86)

The distributed network is further approximated to a first order transfer function as shown below where a_1 is the dominat pole that determines the delay of the line.

$$\frac{V(x = d, s)}{V_{in}(s)} = \frac{1}{(a + c) + \left(b + \frac{c}{2!} + \frac{a}{3!}\right)C_1R_1s}$$

(3.87)

First order transfer function is equivalent to

$$\frac{V(x = d, s)}{V_{in}(s)} = \frac{K_1}{s + a_1} = \frac{V_{dd}}{s}\left(\frac{K_1}{s + a_1}\right)$$

(3.88)

By converting equation (3.88) into time domain and becomes:

$$V(x = d, t) = \frac{V_{dd}}{a + c}[1 - e^{-a_1t}]u(t)$$

(3.89)

Delay time is computed as:

$$\tau_d = \frac{1}{a_1} = \frac{\left(b + \frac{c}{2!} + \frac{a}{3!}\right)}{a + c}C_1R_1$$

(3.90)

Substituting the values of value of *a*, *b*, and *c*, in equation (3.90) reduces to:

$$\tau_d = \frac{[\frac{R_S}{R_1} + \frac{1}{2}\left(1 + \frac{R_S}{R_L}\right) + \frac{1}{6}\frac{R_1}{R_L}]C_1R_1}{[\frac{R_1}{R_L} + \left(1 + \frac{R_S}{R_L}\right)]}$$

(3.91)

On the basis of above mathematical model, the various results are estimated for delay parameters which are similar to previous Model IR_{eff} C_T.

By using this proposed model dominant pole is computed from the first order system function. It is analyzed for different current mode circuit parameters to determine the nature of current mode circuits. It is also observed that with the increase in the length of interconnect the simulation results deviate from the proposed model by 3.96%. For load resistance equal to total equivalent resistance of *RLC* lines the system delay is still smaller than voltage mode signalling. The delay at R_L=0 is 2.77 times lesser than the current mode delay at $R_L = R_T$. Hence, it is concluded that the use of current mode techniques can lead to significant speed enhancement in long VLSI interconnects.

This proposed current mode technique can significantly impact chip access times and architecture trade-offs for future fast CMOS SRAM design. Current mode signal receivers can be used to significantly reduce the line delays in CMOS VLSI chips. Further figure of merit have been evaluated determine the relative accuracy of a R_{Teff} C_T model of on-chip interconnects, which will be discussed in next section. The time delay derived expression along with accuracy analysis can serve as a convenient tool for delay estimation with minimal computation during design.

3.5.1 Steady State and Bandwidth Formulation of Long RC Interconnect Line

The proposed Model III has been exploited for 3dB bandwidth formulation & steady state response generation. The novel delay model derived in equation (3.91) reports the column bit line delay has been used, in whichR_1 represents total line resistance, R_L is load resistance, $R_S$is the driver output resistance and given by:

$$\tau = {}^{1}/_{a_1} = \left(\frac{R_S}{R_1} + \frac{\left(1 + \frac{R_S}{R_L}\right)}{2!} + \frac{\frac{R_1}{R_L}}{3!}\right)C_1R_1/(\frac{R_1}{R_L} + \left(1 + \frac{R_S}{R_L}\right))$$

(3.92)

The above representation of column bit line delay is without any assumption for voltage and current mode signaling. As the line delay in nanometer regime will be different. At highly scaled technologies $\tau_{int} > \tau_{gate}$ this corresponds to $R_1 > R_S$&τ_{int} is the delay of interconnect and τ_{gate} is the delay of gate. So the line delay can be approximated as under:

For voltage mode signaling ($R_L = \infty$): For current mode signaling ($R_L = 0$):

$$\tau_{VM} = R_S C_T + 0.5\tau_{CM} = 0.5R_S C_T + 0.166R_1 C_T \tag{3.93}$$

3-dB bandwidth for the above system can be calculated as:

$\omega\tau = 1,\ \omega = 1/\tau$ (rad/s)

Then

$$f_{3db} = 1/2\pi\tau$$

This is the 3-db bandwidth of interconnect line without any approximation of DSM. Further the same can be approximated for VM and CM systems respectively.

$$f_{3db} = 1/2\pi\left(\frac{R_S}{R_1} + \frac{\left(1+\frac{R_S}{R_L}\right)}{2!} + \frac{\frac{R_1}{R_L}}{3!}\right) C_1 R_1 / (\frac{R_1}{R_L} + \left(1 + \frac{R_S}{R_L}\right)) \tag{3.94}$$

$$f_{3db,VM} = 1/2\pi(R_S C_T + 0.5R_1 C_T) \quad , \quad f_{3db,CM} = 1/2\pi(0.5R_S C_T + 0.166R_1 C_T) \tag{3.95}$$

Step Response Calculation:

A step input r(t) = Ru(t),where R is real constant, and u(t) is unit step function. During calculation R is 1.8V which is equivalent to V_{DD}. Hence, system response is converted into time domain

$$V(x = d, t) = \frac{V_{DD}}{(\frac{R_1}{R_L} + \left(1 + \frac{R_S}{R_L}\right)} [1 - e^{-a_1 t}]u(t) \tag{3.96}$$

whereas, $a_1 = 1/\tau$.

The step response, delay and 3-db bandwidth are computed for current mode signaling using SPICE and MATLAB simulator for various value of load. The comparison between SPICE and analytical is presented in Table 3.10 without the condition of Deep Submicron Regime (DSM) calculated the system time constant, steady state value and the dc coefficient. The interconnect design parameters for 180nm technology is calculated using PTM. The step response for first order system is calculated and presented in **Fig.3.26** for value of $R_L$in the range of 1k Ω to 1MΩ (ideally $R_L = \infty$). the case of voltage mode signaling with the variation of source resistance R_S. From the step response it is observed that the increase in source resistance value overcome the problem of overshoot and undershoots. Whereas in the case of

current mode signaling The value of R_L is taken in the range of 1 Ωto 100 Ω(ideally R_L=0). Keeping same analogy in mind the different results are estimated from the analytical model as in equation (3.94) by using MATLAB and the results of the mathematical model is validated by the SPICE simulations. During this model validation, firstly we optimized the value of source resistance R_S for 2mm line of length. For the analysis, the first iteration value of R_S=81.44Ω has been taken, which is nearly equal to the value of characteristic impedance of line. By setting the value of source resistance and load resistance to 81.44Ω the reflection at the source end are minimized and the estimated results are presented in **Table 3.10**.

But during SPICE analysis overshoots are observed which are not desirable as shown in **Fig. 3.26**. Due to overshoots system response goes to sluggish. The rise time of the system is calculated for 10% to 90% and is equivalent to mathematical calculation. Further the time constant of the network is estimated as the step response to rise to 63.2% of its final value. Settling time (T_s) is within 2% of the final value. The step response for current mode system for 2mm length of interconnects line with R_L=81.44Ω & R_S= 81.44Ω is estimated and plotted using MATLAB shown in **Fig. 3.27 (a)** and the same are verified by using SPICE simulations reported in **Fig. 3.27(b).**System time constant 50% delay (τ) for 2mm line is also in close agreement with calculation as reported in Table 3.10. Steady state value is very close to each other and same is verified using SPICE and MATLAB simulations presented in **Fig. 3.27(a) & Fig. 3.27 (b)**for 2mm length of interconnect.

This steady state value is the dc coefficient on interconnect line which is very small in magnitude for R_L=81.44 Ω. It is the available swing on the interconnect line which is responsible for very small amount of power consumption on line. For different length of interconnect line the dc coefficient is calculated and presented in Table 3.10. Further frequency response analysis and the bandwidth of interconnect line is estimated. And it is found to be very large for current mode system. This bandwidth of the first order system decrease with the time constant (τ) as it increases or in other way with the length of interconnect it decreases. The frequency response is shown in **Fig. 3.28 (a) &Fig. 3.28 (b)** i.e. verified by SPICE and MATLAB simulations. The above discussion is also verified for R_L=81.44 Ω& R_S= 81.44Ω and SPICE and MATLAB calculated results are reported in Table 3.10. Further for R_L=1k Ω & R_S= 81.44Ω the above analysis has been done but it is considered as a case of voltage mode signalling and estimated results for this case are reported in **Table 3.10.** So the value of time constant and the magnitude of dc coefficient

have increased on the line. Signal swing is increased, which is responsible for large amount of power dissipation on the interconnect line. Similarly bandwidth is also decreased for 2mm length of line for ideal case of VM & CM signaling from 6.8 GHz to 0.844GHz detailed in **Table 3.11** with the condition of DSM.

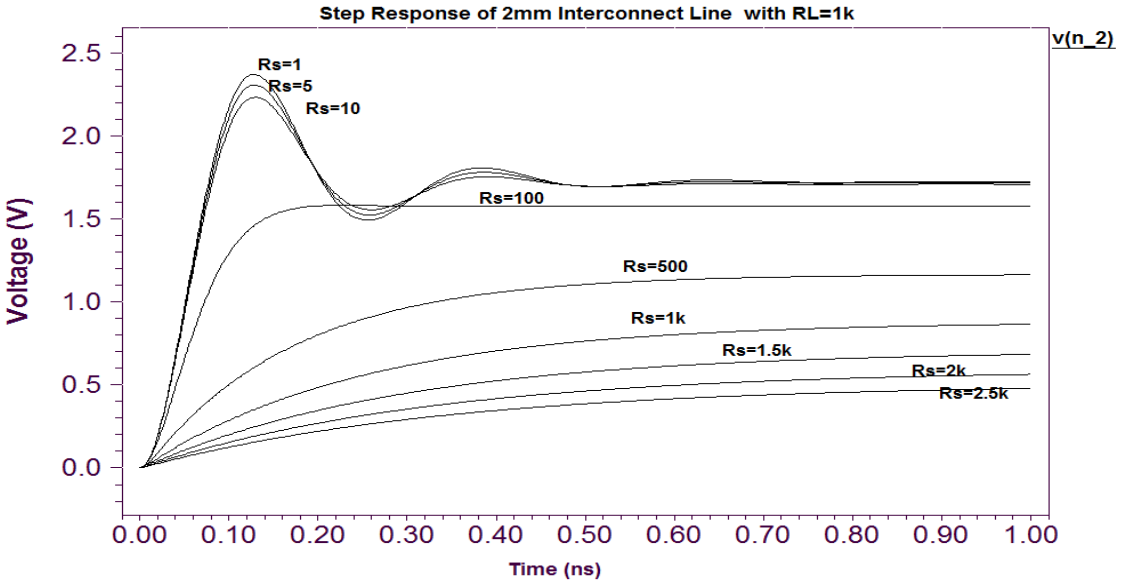


Fig. 3.26 Step response of 2mm length of interconnect line using SPICE

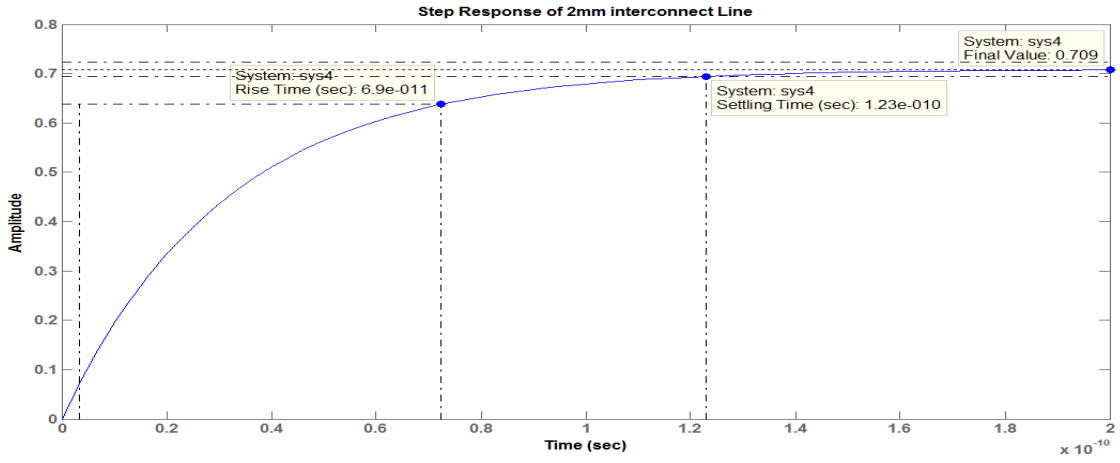


Fig. 3.27(a) Step response using MATLAB with settling time (R_L=81.44Ω & R_S= 81.44Ω)

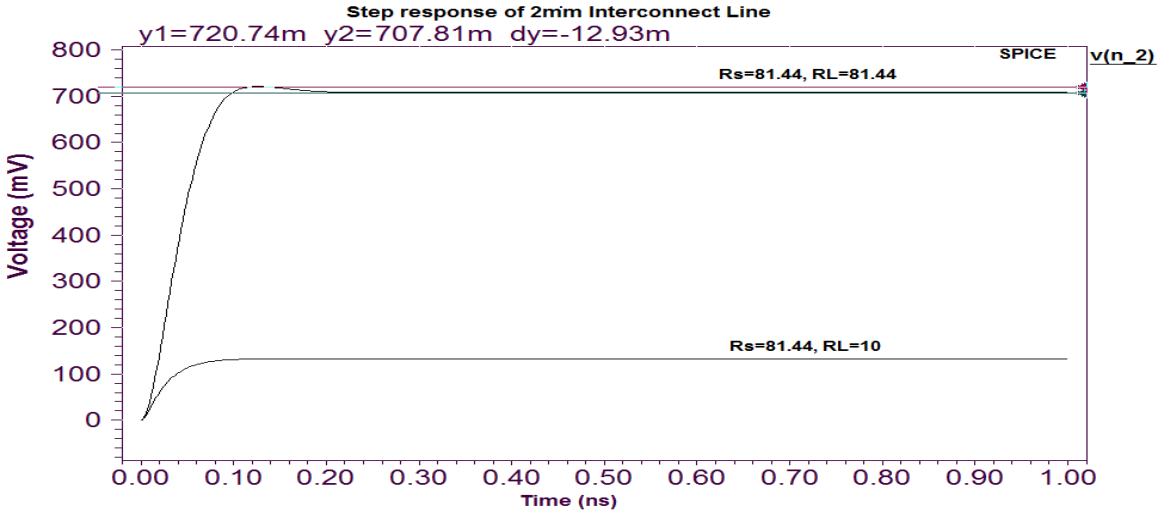


Fig. 3.27 (b) Steady state value verification of model using SPICE

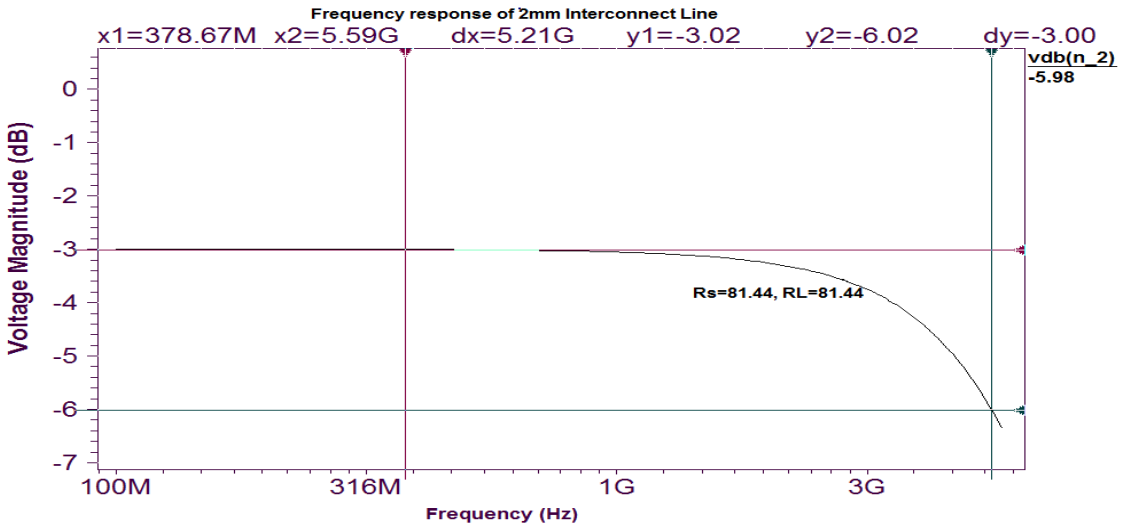


Fig. 3.28 (a)3-db bandwidth estimation using SPICE (R_L=81.44Ω & R_S= 81.44Ω)

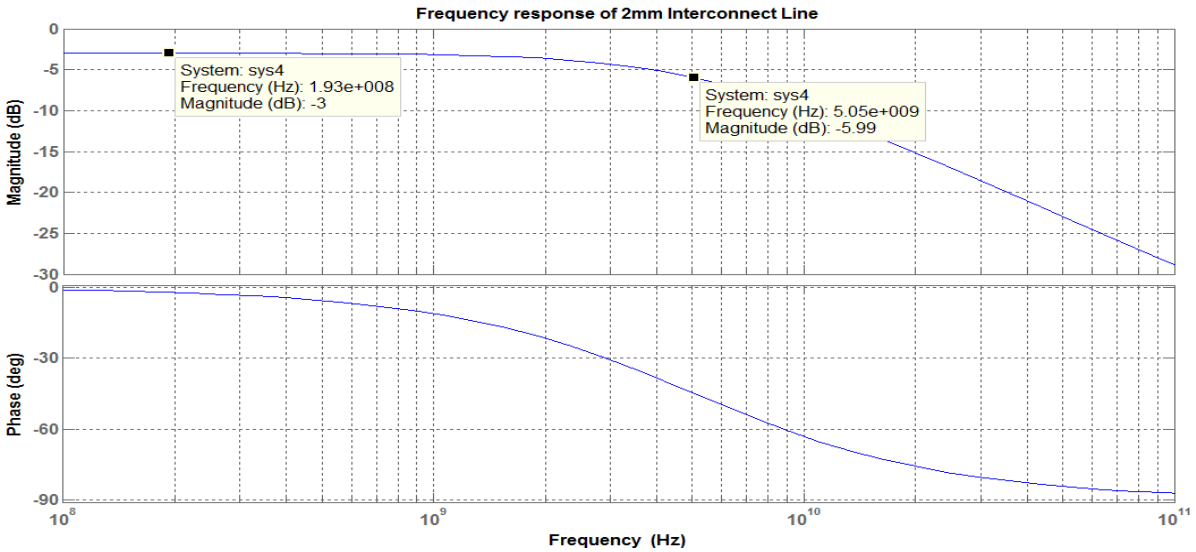


Fig. 3.28 (b) 3-db Bandwidth estimation for 2mm length of interconnect line using MATLAB And verification of SPICE results

In this section a first order transfer function is investigated for current mode versus voltage signalling. The step response and bandwidth is estimated for various length of VLSI interconnects. The rise time is calculated and verified for output signal form 10% to 90% of settling time within the tolerance of 2%. The dc coefficient on interconnect line is a useful parameter for exact calculation of power consumption on the line. Further, the bandwidth is estimated for different length of interconnect. It is decreasing with the length. Current mode signalling is found to be superior in bandwidth when compared to voltage mode systems. Analytical calculations are in close agreement to SPICE simulations. This proposed closed form representation is convenient for step input analysis and for bandwidth estimation for any length of interconnect line.

Table 3.10. Calculation of time constant bandwidth and steady state value. (Current Mode and Voltage Mode)						
CM	**R_L=81.44Ω, R_S=81.44Ω, V_{dd}=1.8V**			Dc Coefficient	**Existing Model [21]**	Steady State Val.
Length (mm)	**This Work (τ) (ns)**	This Work (GHz)	SPICE (GHz)	K_{dc}	RC(ns) (τ)	V_{dd}*K_{dc}
2	0.031	5.132	5.59	0.393	0.0257	0.708
4	0.070	2.267	2.690	0.324	0.0606	0.584
6	0.116	1.361	1.726	0.276	0.104	0.497
8	0.171	0.930	1.263	0.240	0.155	0.432
10	0.232	0.684	0.996	0.212	0.213	0.382
VM	**R_L=1kΩ, R_S=81.44Ω, V_{dd}=1.8V**				**Existing Model [21]**	
Length (mm)	**This Work (τ) (ns)**	This Work (GHz)	SPICE (GHz)	K_{dc}	RC(ns) (τ)	V_{dd}*K_{dc}
2	0.04742	3.35716	3.916	0.888541	0.0477	1.599374
4	0.11263	1.41342	1.403	0.85511	0.114	1.539198
6	0.19423	0.8196	0.737	0.824103	0.198	1.483385
8	0.29145	0.54622	0.439	0.795267	0.298	1.431481
10	0.40313	0.39490	0.306	0.76838	0.413	1.383084
	R_L=1kΩ, R_S=2.5kΩ, V_{dd}=1.8V				**Existing Model [21]**	
Length (mm)	**This Work (τ) (ns)**	This Work (GHz)	SPICE (GHz)	K_{dc}	RC(ns) (τ)	V_{dd}*K_{dc}
2	0.35416	0.44950	0.443	0.2821	0.369	0.50778
4	0.72154	0.22063	0.223	0.2787	0.75	0.50166
6	1.10048	0.14466	0.146	0.2753	1.14	0.49554
8	1.49228	0.10668	0.112	0.2720	1.55	0.4896
10	1.8952	0.084	0.085	0.2688	1.97	0.48384

Table 3.11. Calculation of delay and bandwidth for CM ($R_L = 0$) & VM ($R_L = \infty$)				
Length (mm) (L)	CM delay (ns)	VM delay (ns)	Bandwidth (GHz) for CM	Bandwidth (GHz) for VM
2	0.023402	0.050375	6.802837	3.160298
4	0.054002	0.122304	2.948039	1.301675
6	0.091697	0.215557	1.736153	0.738552
8	0.136604	0.330408	1.165412	0.481829
10	0.188591	0.466539	0.844155	0.341236

Finally bandwidth with current-sensing is wider than voltage-sensing. It is because the shift in pole position and reduction of the system time constants that result from sensing signals with low impedance nodes. Table 3.11 shows current-mode bandwidth is higher than voltage-mode. It is due to voltage sensing induces high impedance (R_L) on the side of receiver, increasing the system time constants due to the impedance termination of the line. Current sensing refers to sense a signal with a low impedance termination at the receive-end which results in a shift in pole position by increasing the bandwidth of the line. It also offers impedance matching in receiver side.

3.6. Geometrical & Critical Frequency Estimation for Inductance

In this section the explanation about the controlling as well as minimization of inductance is discussed& presented

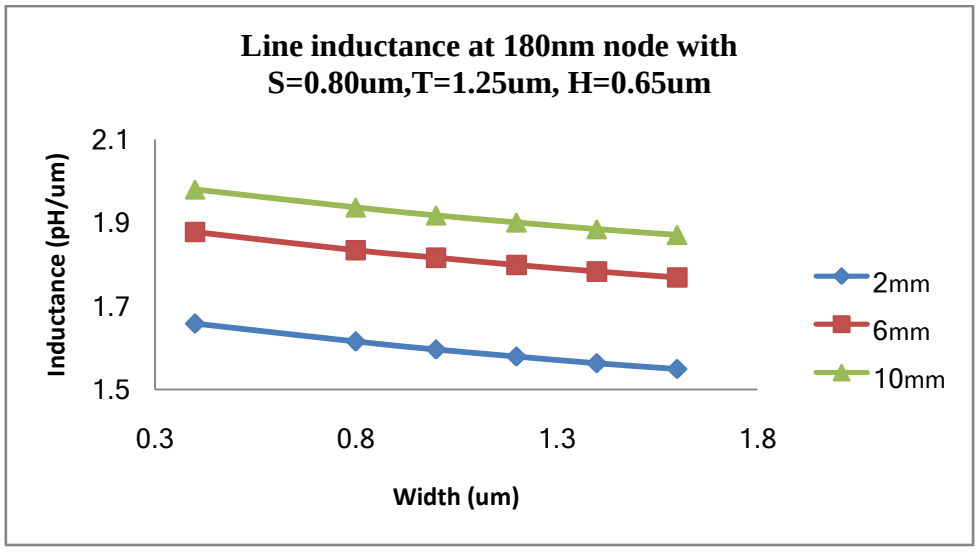


Fig. 3.29 Line inductance variation with the width

From **Fig. 3.29** it is concluded that the inductance of a interconnect line decrease with the increase in the width of wire.

$$\emptyset = Li = L\left(\frac{V}{R}\right) \tag{3.97}$$

$$L = \emptyset(\frac{R}{V}) \tag{3.98}$$

Due to the increase of width of wire, the resistance of wire will decreases and with decrease in resistance the inductance will also decrease as given in equation (3.97) & (3.98), and also reported in **Fig. 3.29.** With the increase in length of interconnect the resistance increase in direct proportion of length, so as the resistance will increase inductance will increase for one particular width of line. The same is reflected by **Fig. 3.29.**

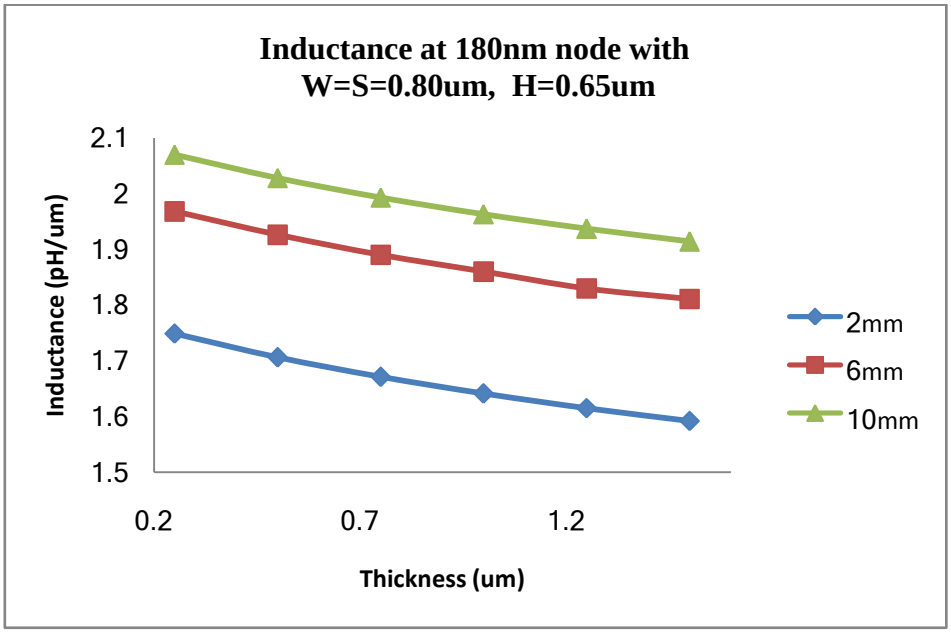


Fig. 3.30 Inductance variation with the thickness of interconnect line

The explanation for the case of inductance decrement with the increase in thickness as shown in **Fig. 3.30** as the thickness will increase resistance will decrease, and as the decrement in resistance will minimize the value of inductance as reported in equation (3.98).

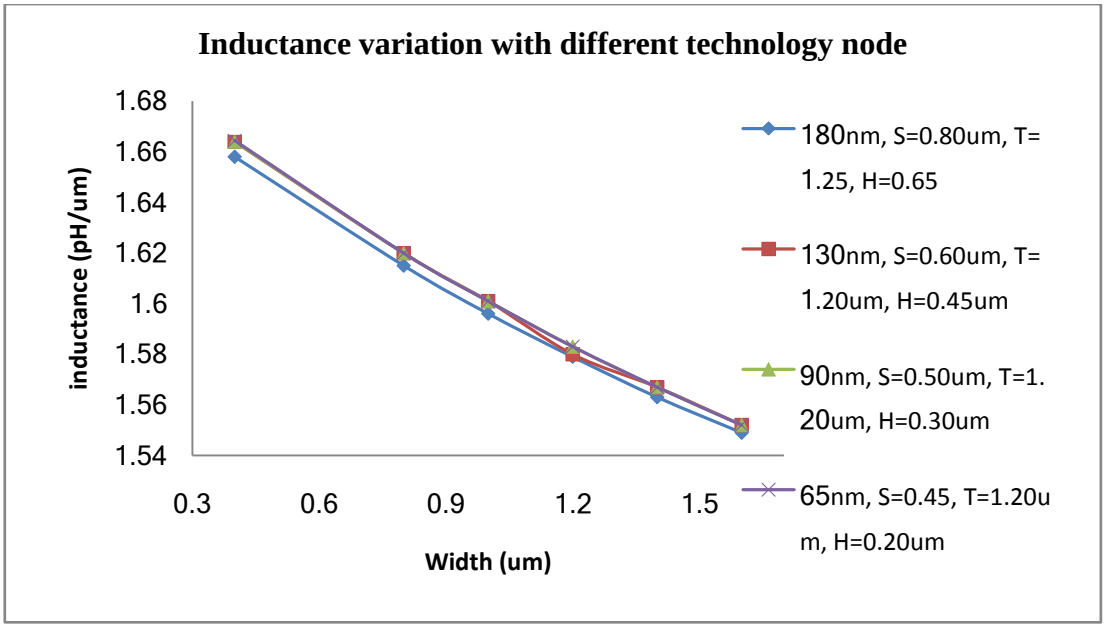


Fig. 3.31 Inductance variation for different technology node with width

From **Fig. 3.31** it is clear that with technology scaling the value of inductance will increase for one particular width of wire as the resistance of wire also increase with scaling. Because with technology scaling, the thickness of wire remains constant but width reduces due to increases in resistance of wire.

3.6.1Critical Frequency Selection for Avoiding the Inductance Effect

In this section the effects of inductance with frequency are presented and discussed.

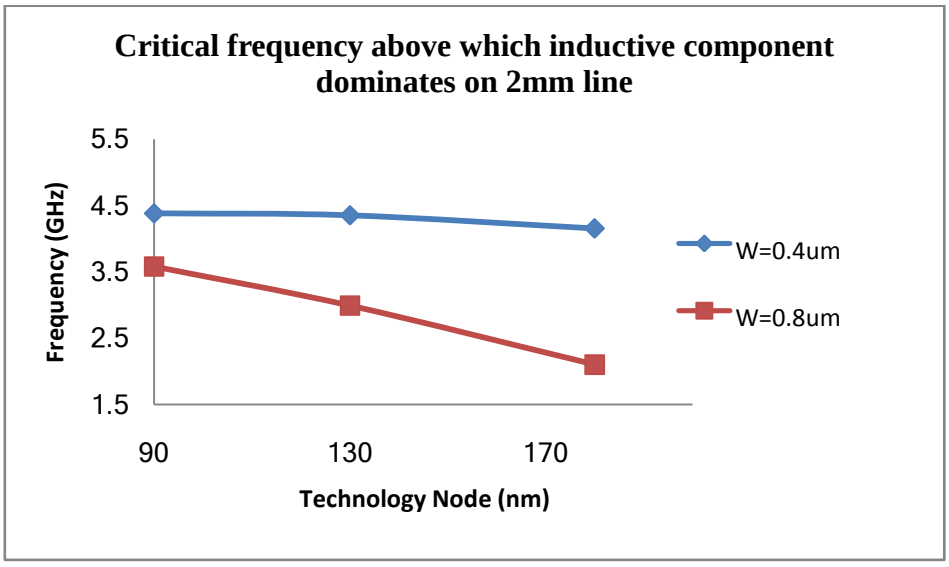


Fig. 3.32 Variation of frequency with technology nodes for 2mm length of interconnect line

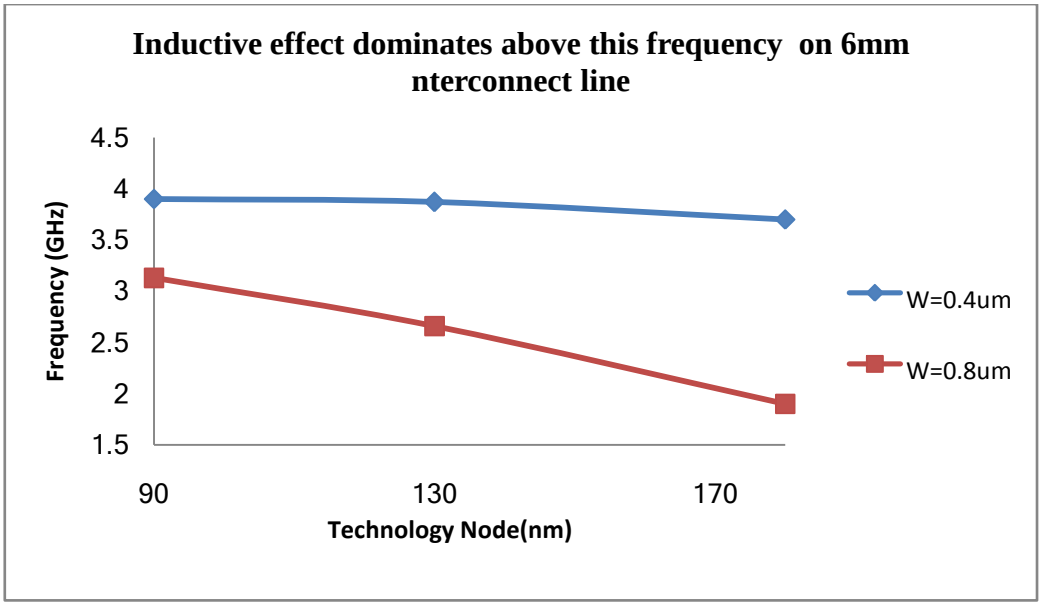


Fig. 3.33 For 6mm length of interconnect line

From **Fig. 3.32, Fig. 3.33** and **Fig.3.34** for different length 2mm, 6mm and for 10mm length with technology scaling variation is shown for the frequency above which inductance effect will start to dominate, as the frequency input signal is larger than the calculated one.

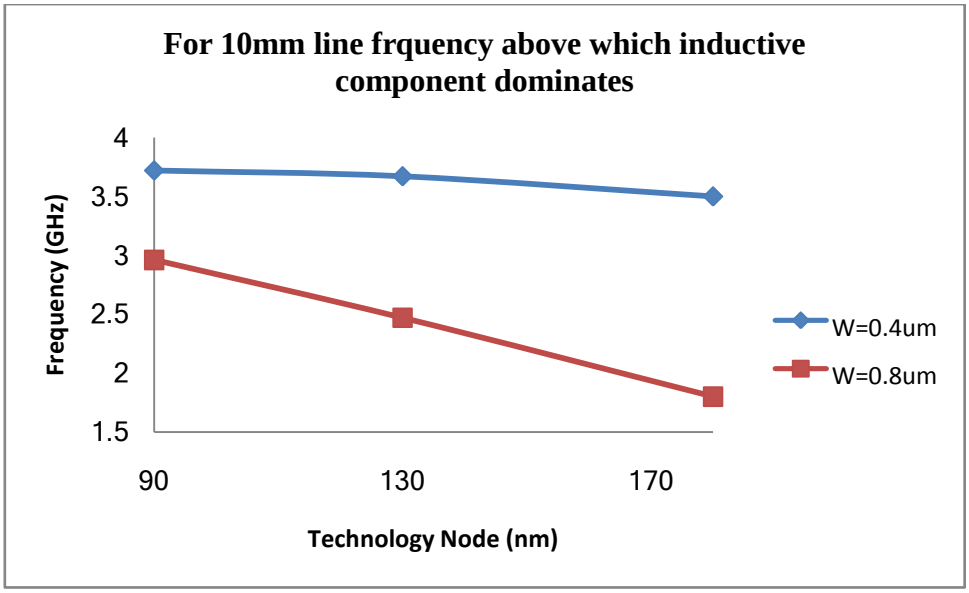


Fig. 3.34 For 10mm length of interconnect line

Even this frequency range can be decreased as per the requirement of the design, if the designer wants to decrease the operating frequency, it can be decrease just by controlling the width of wire as shown in **Fig. 3.32, Fig. 3.33, Fig. 3.34**.

Table 3.12 Calculation of Input Frequency Signal for 180nm node for Different Length

180nm node	2mm		6mm		10mm	
W=0.4µm	88 Ω	1.658pH/um *2000µm=3370pH=l	264 Ω	1.878pH/um *6000µm=11268 pH	440 Ω	1.980pH/um *10000µm= 19800pH
	6.28*3370pH*f=88 $f = \frac{88}{21163e-12}$ $= 0.00415e12 = 4.15GHz$		6.28*11268pH*f=264 $f = \frac{264}{70763e-12}$ $= 0.0037e12 = 3.7GHz$		6.28*19800pH*f=440 $f = \frac{440}{124344e-12}$ $= 0.0035e12$ $= 3.5GHz$	
Resistance of wire (W=0.8µm)	44 Ω	1.615pH/um × 2000µm = 3230pH = l	132 Ω	1.834pH/um *6000µm=l	220 Ω	1.9371pH/um *10000 µm=l
Inductive part of the wire impedance become equal to resistive component at a frequency (f)	$\omega l = 2\pi fl = R$ $2 \times 3.14 \times f \times 3230pH = 44$ $f = \frac{44}{20284 \times 10^{-12}}$ $= 0.00216e12 = 2.1GHz$		6.28 × 11004pH × f = 132 $f = \frac{132}{69105 \times 10^{-12}}$ $= 0.00191e12 = 1.9GHz$		6.28 × 19371pH × f = 220 $f = \frac{220}{121649e-12}$ $= 0.00180e12$ $= 1.8GHz$	

Table 3.13 Depict Calculation of Frequency at 130nm Technology Node

130nm node	2mm		6mm		10mm	
W=0.4µm	91 Ω	1.664pH/um *2000µm=3328pH=l	275 Ω	1.884pH/um *6000µm=11304 pH	458 Ω	1.986pH/um*100 00µm=19860pH
	6.28*3328pH*f=91 $f = \frac{91}{20899e-12}$ $= 0.00435e12 = 4.35GHz$		6.28*11304pH*f=275 $f = \frac{275}{70989e-12}$ $= 0.00387e12$ $= 3.87GHz$		6.28*19860pH*f=458 $f = \frac{458}{124720e-12}$ $= 0.00367e12$ $= 3.67GHz$	
Resistance of wire (W=0.8µm)	61 Ω	1.62pH/um × 2000µm = 3240pH = l	183 Ω	1.860pH/um *6000µm=l	305 Ω	1.963pH/um *10000 µm=l
Inductive part of the wire impedance become equal to resistive component at a frequency (f)	$\omega l = 2\pi fl = R$ $2 \times 3.14 \times f \times 3240pH = 44$ $f = \frac{61}{20347 \times 10^{-12}}$ $= 0.00299e12 = 2.99GHz$		6.28 × 11160pH × f = 183 $f = \frac{183}{70084 \times 10^{-12}}$ $= 0.00261e12$ $= 2.6GHz$		6.28 × 19630pH × f = 305 $f = \frac{305}{123276e-12}$ $= 0.00247e12$ $= 2.47GHz$	

Table 3.14 Calculation of Frequency at 90nm Technology Node

90nm node	2mm (2000um)		6mm (6000um)		10mm (10000um)	
W=0.4µm	91 Ω	1.664pH/um *2000µm=3328pH=l	275 Ω	1.884pH/um *6000µm=11304 pH	458 Ω	1.986pH/um*100 00µm=19860pH
	6.28*3328pH*f=91 $f = \frac{91}{20899e-12}$ $= 0.00435e12 = 4.35GHz$		6.28*11304pH*f=275 $f = \frac{275}{70989e-12}$ $= 0.00387e12$ $= 3.87GHz$		6.28*19860pH*f=458 $f = \frac{458}{124720e-12}$ $= 0.00367e12 = 3.67GHz$	
Resistance of wire (W=0.8µm)	73 Ω	1.62pH/um× 2000µm = 3240pH = l	220 Ω	1.860pH/um *6000µm=l	366 Ω	1.963pH/um *10000 µm=l
Inductive part of the wire impedance become equal to resistive component at a frequency (f)	$\omega l = 2\pi fl = R$ $2 \times 3.14 \times f \times 3240pH = 73$ $f = \frac{73}{20347 \times 10^{-12}}$ $= 0.00358e12 = 3.58GHz$		6.28× 11160pH × f = 220 $f = \frac{220}{70084 \times 10^{-12}}$ $= 0.00313e12$ $= 3.13GHz$		6.28× 19630pH × f = 305 $f = \frac{366}{123276e-12}$ $= 0.00296e12 = 2.96GHz$	

With technology scaling the operating frequency increase, the same behaviour is self-explanatory from above **Fig. 3.32, Fig. 3.33, Fig. 3.34** and **Table 3.12, Table 3.13, Table 3.14** depicts the calculation for different length of interconnect at 180nm, 130nm & 90nm respectively. Hence, with increase in length and technology is scaled down the frequency of signal also decrease, this behaviour also illustrated in **Fig. 3.32, Fig. 3.33, Fig. 3.34**. The calculation process for different technology node is presented with different widths.

The consequences of inductance dominance includes ringing, overshoot effects, reflection of signals due to impedance mismatch, inductive coupling between line, and switching noise due to (Ldi/dt) voltage drops.

Further inductance can be reduced by increasing width and thickness of line. Hence, it can be reduced by the low value of permittivity and permeability of the surrounding dielectric. With the inclusion of all above factors the consequences of inductance dominance can be avoided.

3.6.2 Importance of Damping Factor for VLSI Interconnects

Damping factor, input signal rise time and significant length of without inductance effect has been addressed in [112]. When these factors are incorporated with RLC model it can be approximated as RC interconnect model. For this frequency response of lumped RLC circuit

is estimated from basic equation of circuit theory. Generalized transfer function of RLC lump network is presented below

$$H(s) = \frac{\frac{1}{LC}}{\left[s^2 + \left(\frac{RC}{LC}\right)s + \left(\frac{1}{LC}\right)\right]} \tag{3.99}$$

Comparing the above eqn. with 2nd order transfer function

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + 1} \tag{3.100}$$

It generates: $\omega_n^2 = 1/LC$ and $2\xi\omega_n = RC/LC$ and hence the damping factor becomes

$$\xi = \frac{R_t}{2}\sqrt{\frac{C_t}{L_t}} = R.\frac{d}{2}\sqrt{\frac{C}{L}} = d.\alpha_{sat} \tag{3.101}$$

And the poles of the circuit are

$$P_{1,2} = \omega_0[-\xi \pm \sqrt{(\xi^2 - 1)}] \tag{3.102}$$

Hence, the above formulation implies that, if ξ is greater than one, the poles are real and the effect of inductance on the circuit is small. The greater the value of ξ, the more accurate the RC model becomes and it validates that line is highly resistive. On the other way ξ becomes less than unity, the poles becomes complex and oscillations occur. Damping factor (DF) represents the attenuation of wave suffers as it travels a distance corresponds to length of interconnect. As attenuation increases, the effects of the reflections decrease and the RC model becomes more accurate. The pictorial view of RC and RLC lines is presented with ξ(damping) variation in **Fig.3.35.** The input transition time is considered as an alternative for defining the accuracy of RC global interconnect lines over RLC [112].

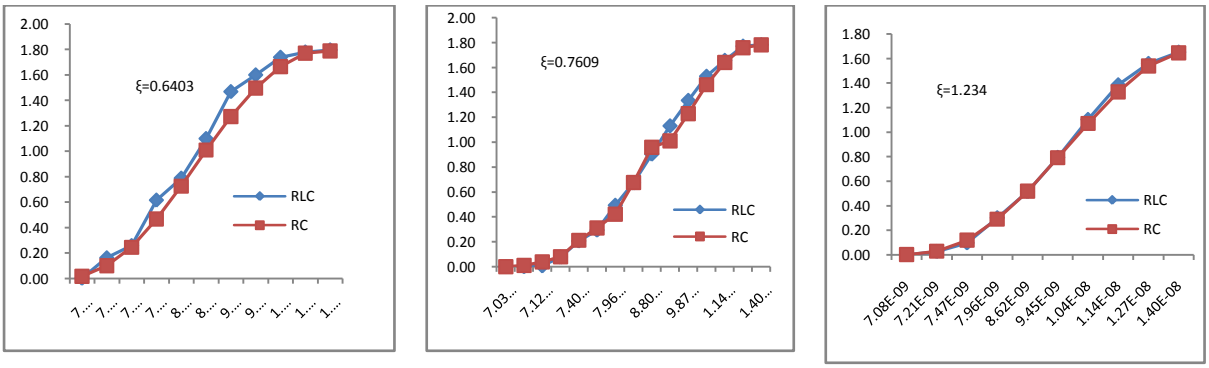


Fig. 3.35 Output response comparison of RLC interconnect model to RC model in term of DF (Damping Factor).

Further the range of interconnect with significant inductance effect is given by

$$\frac{t_r}{2\sqrt{LC}} < d < \frac{2}{R}\sqrt{\frac{L}{C}} \tag{3.103}$$

This range depends upon the parasitic impedance of the interconnect per unit length as well as on the rise time of signal at the input of the CMOS circuit driving the interconnect. The above implications are tested and verified for line $R = 22\Omega/\text{mm}, C = 0.2437\text{pF/mm}, L = 1.937\text{nH/mm}$. With this data, length of interconnect reduces to 2.301*mm*< *d* <8.10*mm.* This region defines the range of *l* for which an RC model is no longer accurate and the interconnect impedance model must include inductance. The response of RC circuit compared to the response of an RLC transmission line is shown in **Fig.3.36**. The above figure demonstrates that inductance has a significant effect on the response of a signal propagating across an interconnect line for the range of length defined above. After observation it is found that the RC circuit model becomes more accurate for when "d" is smaller than 2.301mm and larger than 8.10mm.

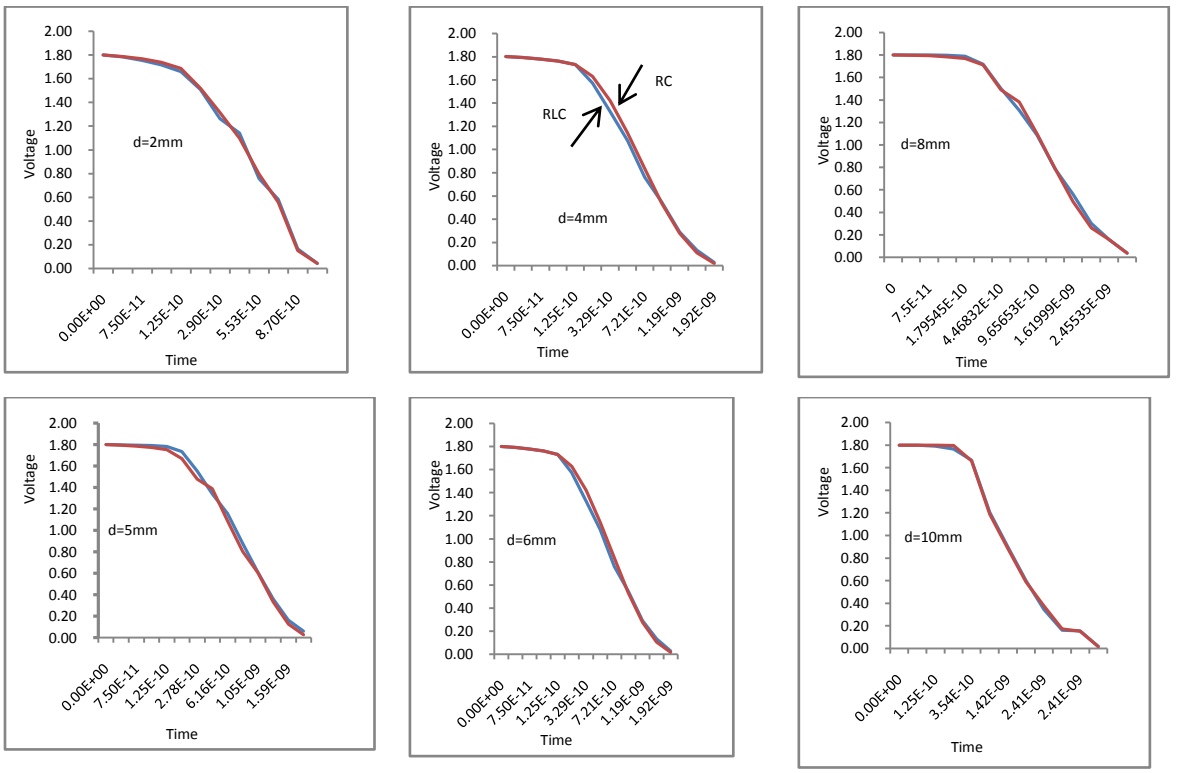


Fig. 3.36 Length dependent accuracy of RC model

3.7 Step Response Analysis of Proposed Models with Existing models

In this section the comparison between the entire proposed and existing model are presented. This comparison has been by the help of step response analysis of all the models. The performance of the entire models has been measured on the basis of $t_{50\%}$ delay for all. Then during analysis it is found that the proposed model R_0C_0 shows the superior & better performance when compared with all other models. But Actual RLC model shows significant inductance in terms of overshoots and undershoots or it can be ringing effect, is pictured in **Fig.3.37** below. After observation it is found that RLC Actual and $R_{eff}C_T$ are closer to each other as shown in **Fig.3.37** by taking simulation parameters as (R_L=10k, R_s=10ohms, C_S=C_L=0 for VM), t_r=1ps, V=1.8V).

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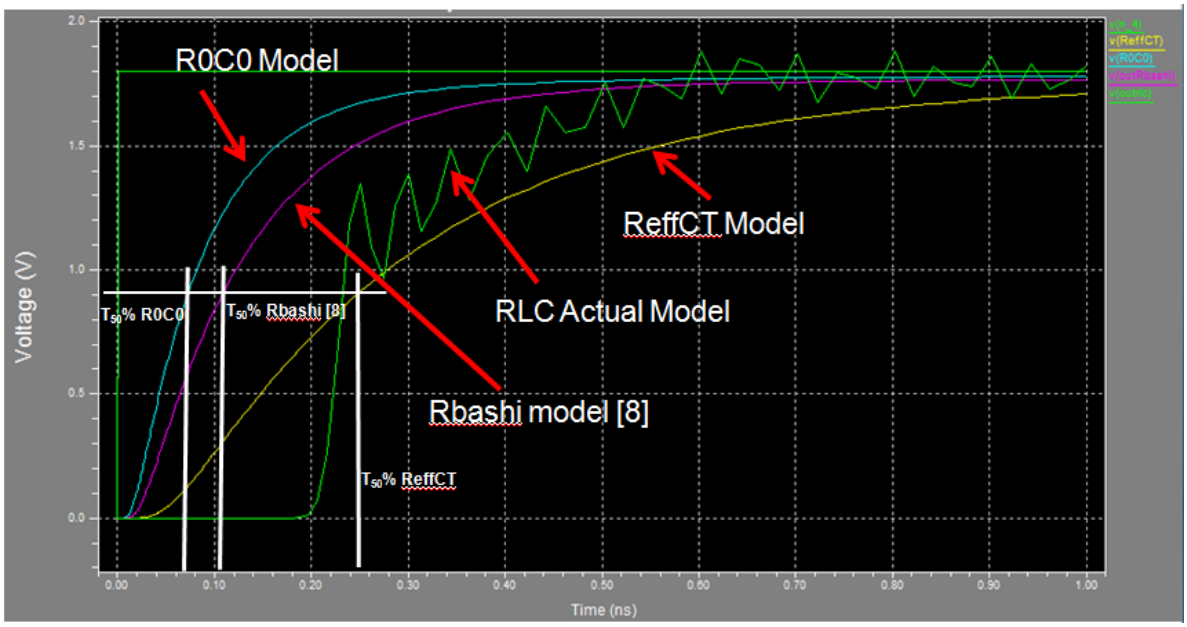


Fig. 3.37 Step response comparison of all the models

In **Fig. 3.38** the step response variation with R_L with different set of source resistance and load capacitance value of C_L=10fF has been taken. After the observation of results it is found that with increase of source resistance the problem of ringing effect is going to decreased. With this interconnect line is becoming resistance dominant with higher value of source resistance.

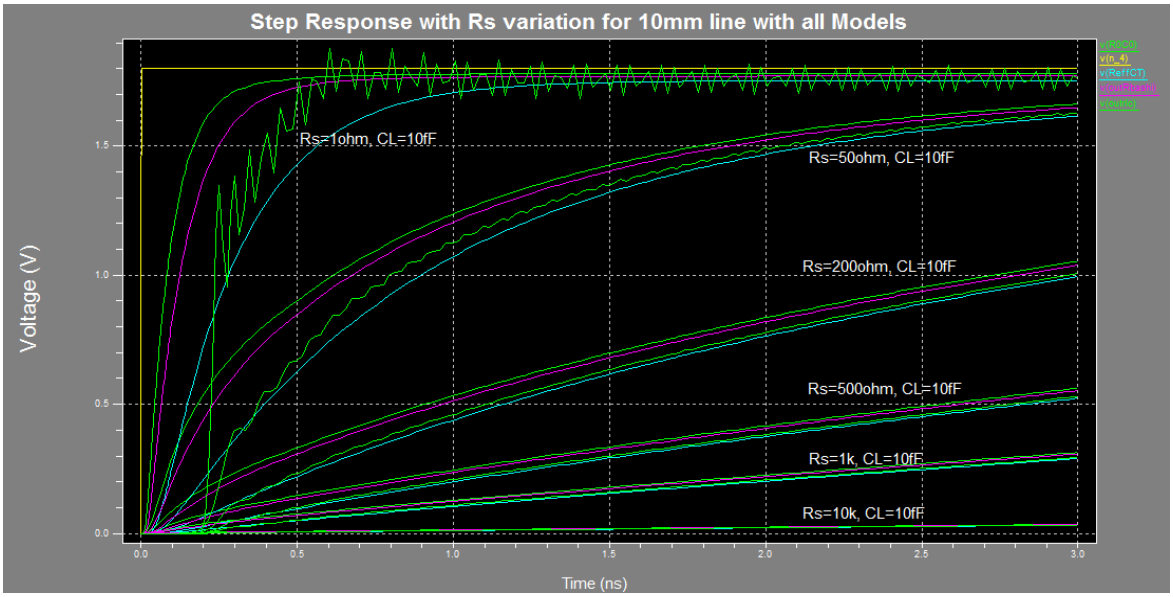


Fig. 3.38 Step response with source resistance variation (with R_S variation R_L=10kΩ).

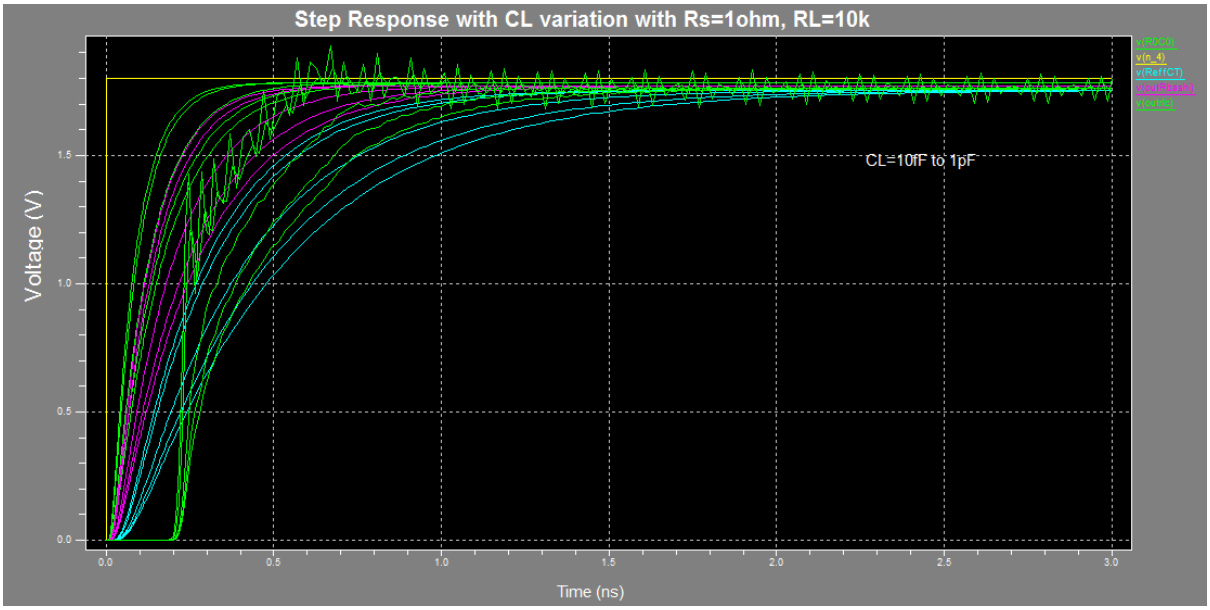


Fig. 3.39 Step Response with Load capacitance variation (R_s=1Ω, R_L=10kΩ for 10mm line).

Fig. 3.39 provide the information about the load capacitance variation with R_L=10kΩ, the case of voltage mode signaling. And the output voltage swing reaches to the value of Full swing voltage of 1.8V and same has been validated through SPICE simulation in Fig. 3.39.

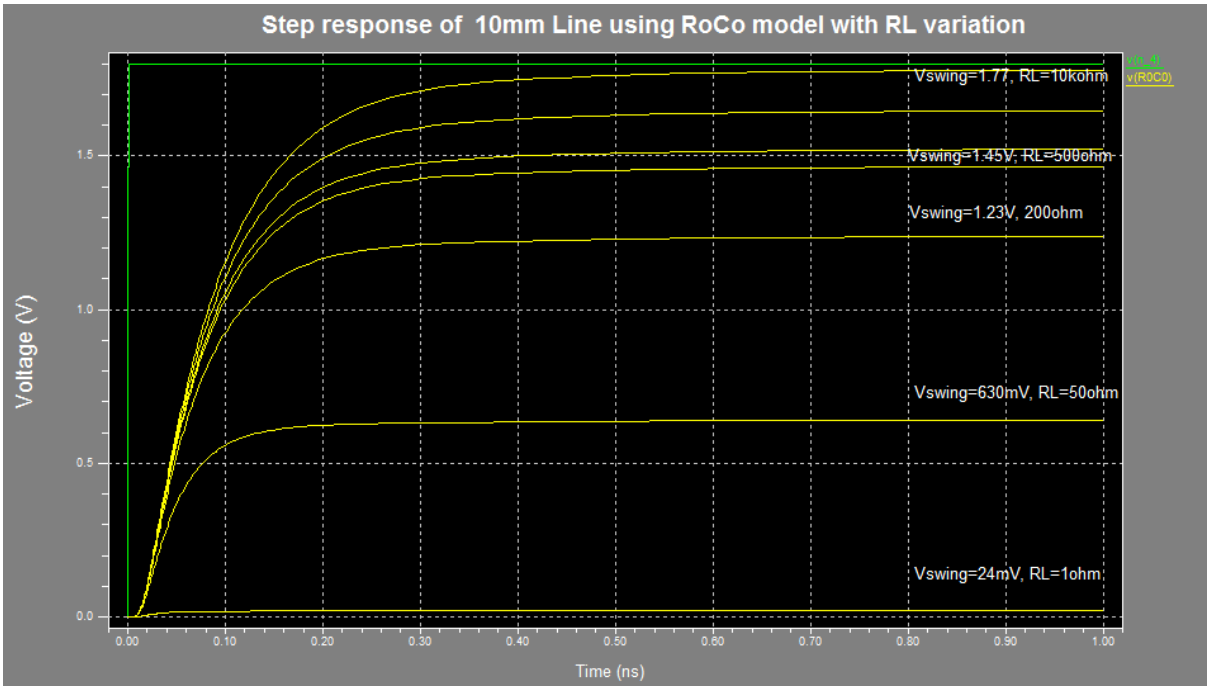


Fig. 3.40 Step response with load resistance variation.

(With R_L Variation with C_L=10fF, Rs=10Ω)

CM systems are the low swing systems are clearly defined from the above **Fig. 3.40** as the CM systems are mainly designed for low swing application. Because this low swing is helpful in number of ways to the complete design. It will reduce switching activity and swing of voltage signal on the line. Once swing is minimized on the line, it directly reduce the dynamics power component on the interconnect line.Further the impact of repeater insertion with VM and CM signaling is analyzed.

3.8 Repeater Insertion with Current and Voltage Mode Signalling

This technique of buffer insertion used in global interconnect buses for minimization of the propagation delay and to improve the quadratic dependency of delay on interconnect line length [32].Most of the microprocessors requires repeating signals at the global level to some extent. Intel Itanium microprocessor [59-60] fabricated in 0.18um 6 Metal Layer with a total of 24.5 million transistors, requires approximately 85% of its global nets to be repeated. From these 13000 total nets at the top level, approximately 11000 require insertions of repeaters.Average number of repeater drop points per net is approximately 1.5 [61].Hence, optimal repeater insertion can be achieved in actual designs but the complexity that arises with it physical implementation (i.e. Placement, area, power and noise).Optimum Number of buffers to be inserted so that the problem of area overhead and increment of power

dissipation can be minimized. Hence, we will calculate optimum number of buffers and buffer size for VM & CM signaling further their comparison will be done.

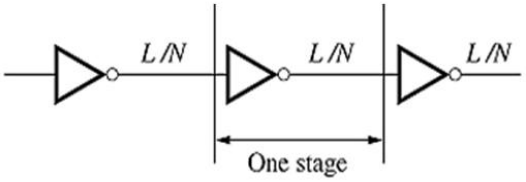
3.8.1 Calculation of Optimum Number of Buffers and Buffer Size for Distributed Model

Wire Resistance per Unit length =R_{int} (Ω/μm)

Wire Capacitance per Unit length = C_{int} (fF/μm)

Total Length of Wire = L(μm)

For reduction of delay, the N numbers of buffer are inserted (Including first buffer) to L length of wire as shown in Fig.3.41 (a)



(a) Wire of length *L* with *N* buffers inserted

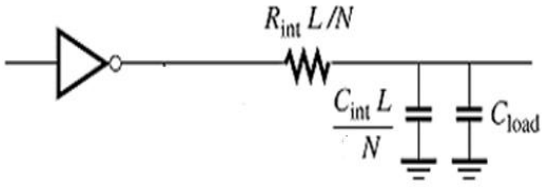
Fig. 3.41 (a)

Now assume the input and output capacitance for minimum size buffer:

$$C_{out} = C_{eff} W(1+\beta) = C_j(1+\beta) \quad (3.104)$$

$$C_{in} = C_g W(1+\beta) = C_G(1+\beta) \quad (3.105)$$

Here, β = the ratio of PMOS to NMOS device size. And the one stage represented below in Fig. 3.41 (b).



(b) One segment of buffer and interconnected

Fig. 3.41 (b)

Value of $C_j = C_{eff} W$, where W is the size of the NMOS device for 1X inverter.

$$C_G = C_g W \quad (3.106)$$

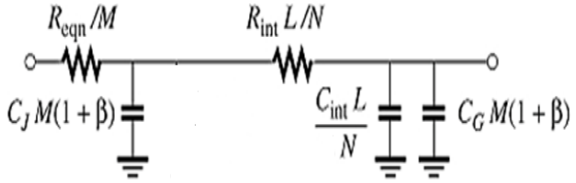
Let M represent the optimal buffer size for the buffer insertion, then For a buffer which is M times larger than a 1X buffer

$$R_{eff} = R_{eqn}/M \quad (3.107)$$

$$C_{out} = C_{eff} W(1+\beta)M = C_j(1+\beta)M \quad (3.108)$$

$$C_{in} = C_g W(1+\beta)M = C_G(1+\beta)M \tag{3.109}$$

Now from Fig. 3.41 (c) The RC Model used for each stage during delay calculation, therefore



(c) *RC* model for one segment

Fig. 3.41 (c)

The delay for each segment

$$t_{segment} = \frac{R_{eqn}}{M} C_j (1+\beta)M + \left(\frac{R_{eqn}}{M} + \frac{R_{int}L}{N}\right) \times \left(\frac{C_{int}L}{N} + C_G(1+\beta)M\right) \tag{3.110}$$

$$t_{total} = N \times t_{segment} = N\left[\frac{R_{eqn}}{M} C_j (1+\beta)M + \left(\frac{R_{eqn}}{M} + \frac{R_{int}L}{N}\right) \times \left(\frac{C_{int}L}{N} + C_G(1+\beta)M\right)\right] \tag{3.111}$$

For optimal value of N & M, we apply the derivative w.r.t. to each variable

$$\Rightarrow N = \sqrt{\frac{R_{int}C_{int}L^2}{R_{eqn}(C_j+C_G)(1+\beta)}} \quad \text{This is the optimal Number of buffers} \tag{3.112}$$

Further derivative w.r.t. to M calculated, $\frac{dt}{dM} = 0$

$$\Rightarrow M = \sqrt{\frac{R_{eqn}C_{int}}{C_G(1+\beta)R_{int}}} \tag{3.113}$$

$\Rightarrow$ This is the optimal value of Buffer size

The various results are estimated on the basis of optimal number of buffers and using buffer size. All the estimated results are presented in **Fig. 3.42** to **Fig. 3.47** using the following parameters R_S=6Ω & R_L=10kΩ for VM and R_S=6Ω & R_L=50Ω for CM. The comparison with the previous work in this domain is also included. After doing this comparison, it is observed that the performance of proposed R_0C_0 Model II is superior in speed. Even after buffer insertion, its performance improves by the 96%. Initially the results are estimated for repeater insertion using the research paper [21]. The results for R.Bashi Model [21] reported in **Fig. 3.42.** Further the results are estimated for the proposed **Model I** & **Model II** and comparison with the existing models reported in research paper [21-22], [106], [109].

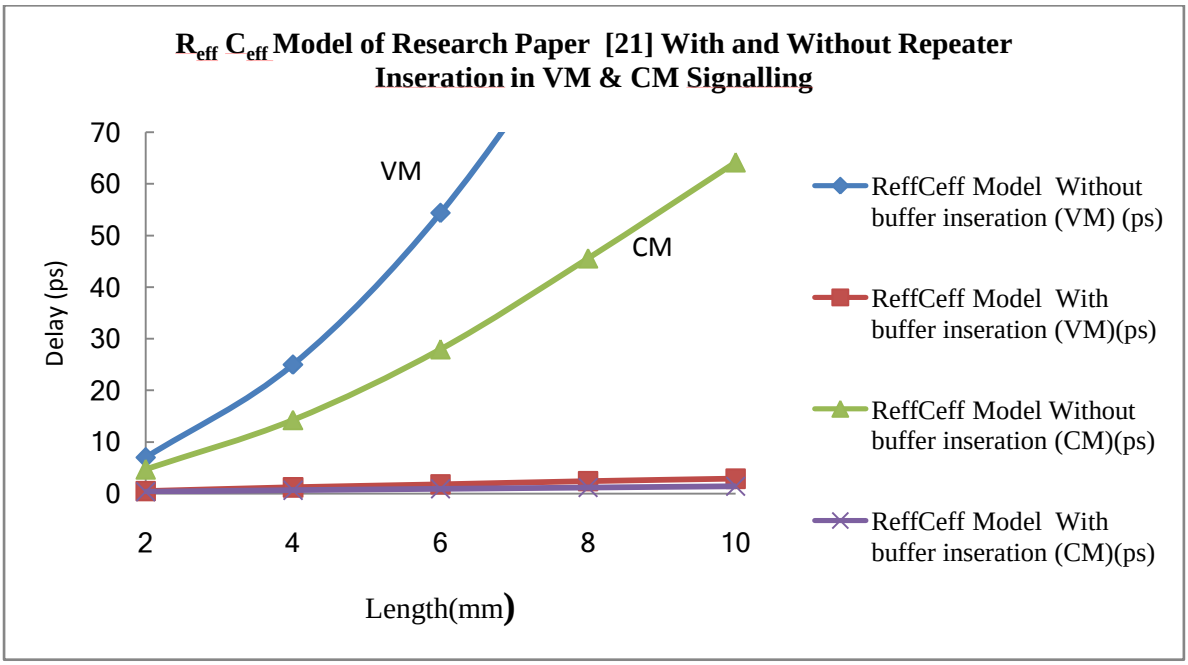


Fig. 3.42 Comparison for repeater insertion in VM and CM signaling.

With voltage mode technique without repeater insertion the delay provided by proposed Model II at 2mm and 10mm is 75ps& 90ps respectively and results are plotted in **Fig. 3.43** After implementation of repeater insertion technique the delay becomes 2.17ps for 2mm length & 2.45ps for 10mm length of interconnect. The number of repeaters utilized for achieving this performance is 120 for 2mm and 135 for 10mm length of interconnects respectively. When the same case applied with current mode signaling, it is observed that current mode technique without repeater insertion provides 24ps of delay for 2mm and 30ps of delay for 10mm length of interconnect respectively. As the technique of repeater insertion is applied with current mode signaling the delay reduces to 0.8ps for 2mm and 1.03ps for 10mm length of interconnects. In order to achieve this performance the number of repeaters utilized is 52 for 2mm length of interconnects and 59 Number of repeaters for 10mm length of interconnects.

Using the current mode technique with buffer insertion performance of system enhanced by 96%. This can be a tremendous improvement at low cost. Because if the same performance is required by voltage mode signaling, the number of repeaters required by voltage mode signaling will increase by a factor of 2.28 time as in voltage mode. The performance achievement with current mode signaling is tremendous, even after buffer insertion with low

cost. More than double of area can be saved by using the current mode signaling technique with repeater insertion with top level global signal like clock buses, ground & power rails etc. Proposed $R_{eff}C_T$ Model I with and without repeater insertion results are presented in **Fig. 3.44.** Tremendous speed improvement is observed with repeaters in CM.

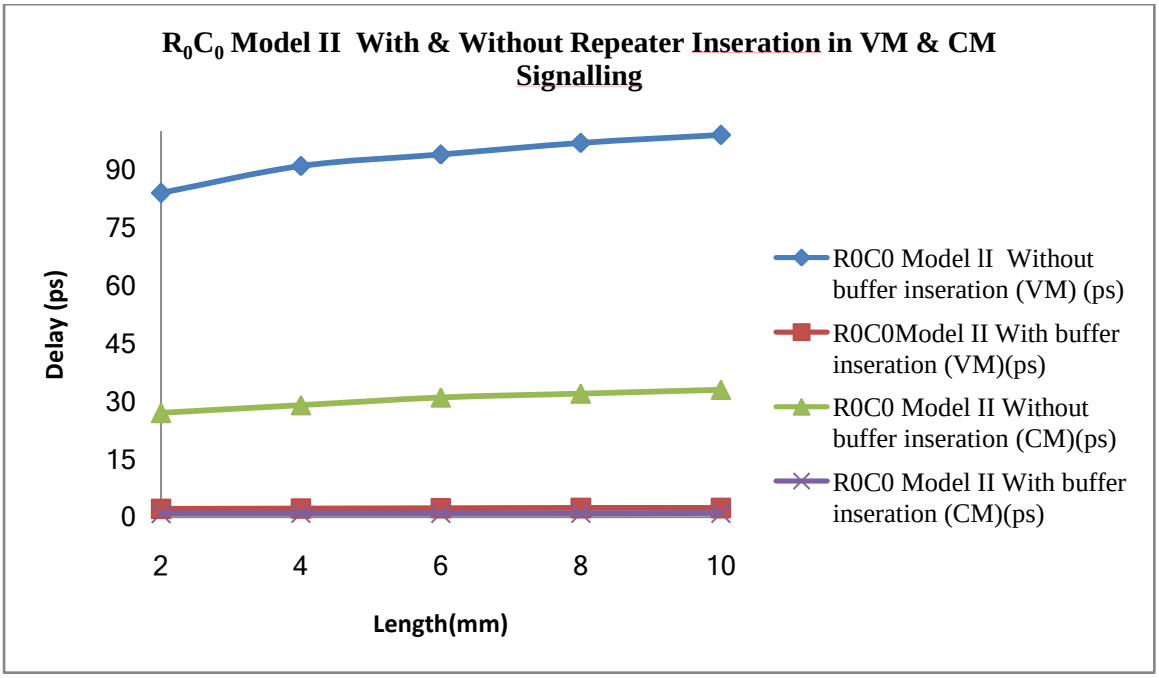


Fig. 3.43 Proposed Model II with &without repeater insertion in VM and CM signaling.

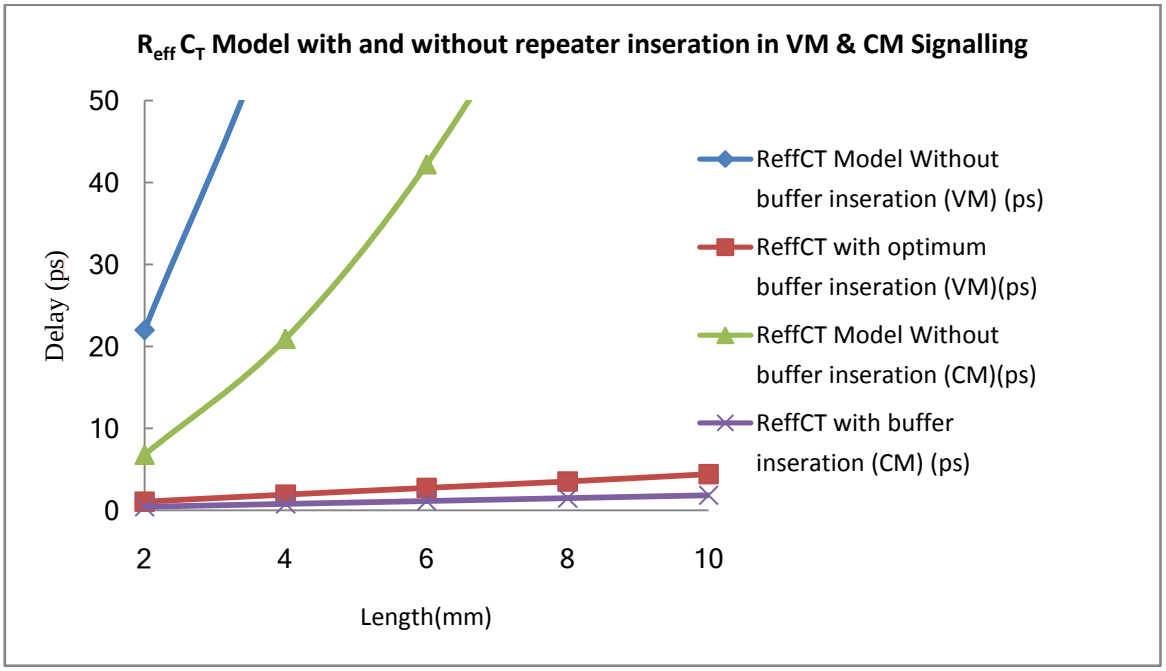


Fig. 3.44 $R_{eff}C_T$ Model I with and without repeater insertion.

Speed improvement using Current Mode Signaling is really equivalent to speed of light transmission with repeater insertion.

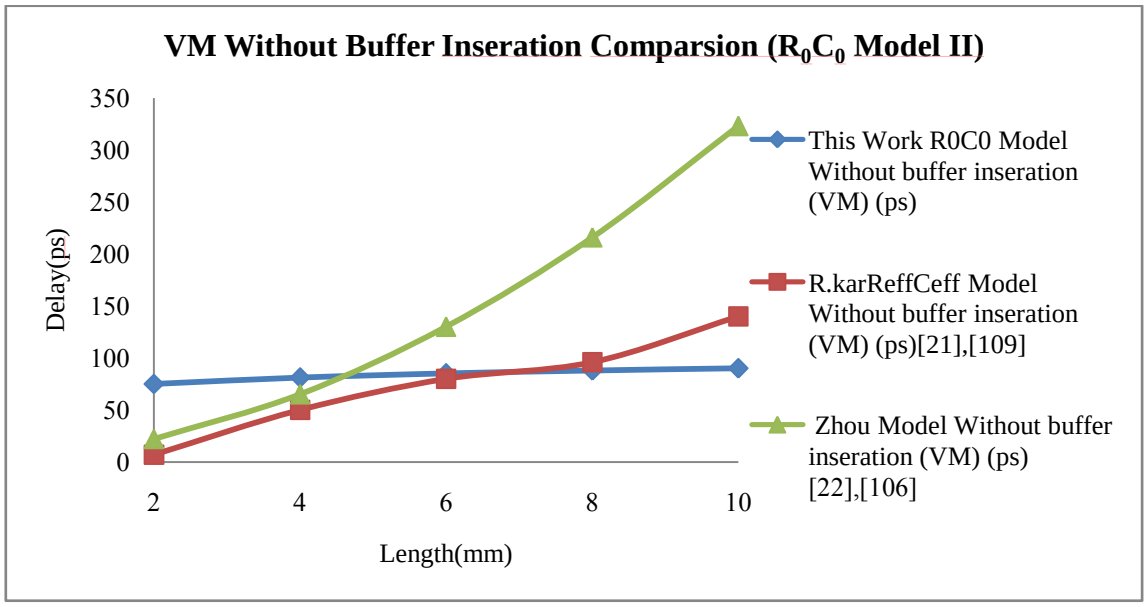


Fig. 3.45 VM comparison without buffer insertion.

In **Fig. 3.45** and **Fig. 3.46** the comparison for the proposed ModeI II R_0C_0delay is presented without and with buffer insertion respectively. After observation of the results, it is found that for longer length of interconnect the proposed Model II is highly suitable, when compared with other existing Models reported in research papers [21-22], 106], [109].

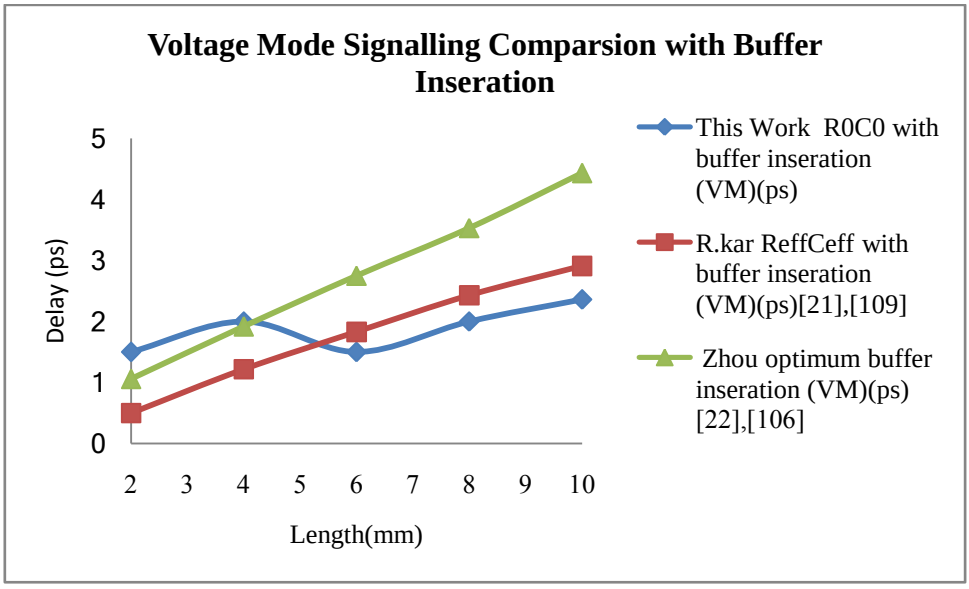


Fig. 3.46 Voltage mode signaling comparison with buffer insertion.

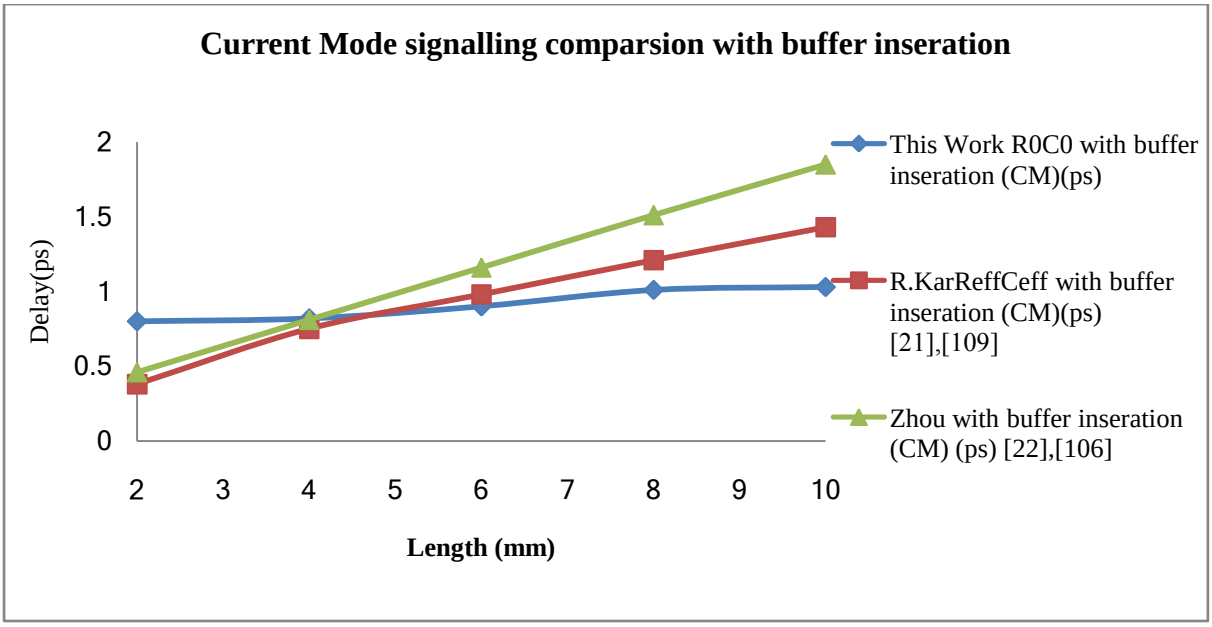


Fig. 3.47 Current mode signaling comparison with buffer insertion.

The proposed Model results with Current model Signalling are reported in **Fig. 3.47.** In which proposed model proves the superiority behavior when compared with other existing models. The proposed model is suitable for longer length of interconnect, after making the observation of results.

Table 3.15 Number of Repeater Utilized in Achieving This Performance

Length (mm)	VM delay with Repeater insertion (ps)	CM delay with Repeater insertion (ps)	No.of Repeater used in VM (N)	No of Repeater used in CM (N)	Performance factor in term of delay	Cost factor reduced in terms of No of Repeaters
2	2.17	0.8	120	52	2.71	2.30
4	2.25	0.82	125	55	2.74	2.27
6	2.30	0.9	130	57	2.55	2.28
8	2.35	1.01	133	58	2.32	2.29
10	2.45	1.03	135	59	2.37	2.28

By using the CM with proposed Model IIR_0C_0 the delay factor reduced by an average value 2.67.The Number of repeaters reduced by average value of 2.28.If same performance is required by voltage mode (VM) as compared to current mode (CM) system, we have to increase the number of repeaters in voltage mode (VM) by the factor 2.28 (approx.) as reported in **Table 3.15**. The performance comparison in terms of number of repeaters is reported in **Table 3.15**.

3.9 Model Validation at Scaled Technology Using CNT

From the literature it is concluded that

- Copper has lower resistivity (about 30% lower than that of aluminium)
- Melting point for Cu is more than 450 degree Celsius higher
- Atomic weight is more than two times heavier than that of Al
- Cu has lower atomic diffusivity than Al
- Again lower atomic diffusivity at higher temp. as 100 degree Celsius
- Lower Value of effective charge on moving ion than Al
- Current Density of Aluminium wire is also limited

Now Technology is Shifting toward future interconnect material i.e. CNT. And Copper due to DSM scaling also have the problem of electro-migration etc.

- CNT material having high value of mobility 100000 cm^2/Vs (Si= $450cm^2/Vs$)
- Higher Current Density in the range of 10^9 A/cm^2 (Cu = 10^6 A/cm^2)
- Lesser Electro-migration problem due to sp^2 bonding structure in CNT
- and It has even four time smaller electro migration than pure copper [09]
- Resistivity of SWCNT ropes of the order of (10^{-04} ohm-cm) at27 degree Celsius [113], therefore these are known as most conductive carbon
- It is thermally stable up to 4000 K [113]
- Activation Energy is high for CNT material than Cu (2.2 eV)

Performance analysis with CNT & Copper material using Current Mode Technique at scaled technologies is discussed in this section. Parameters at Scaled technologies are calculated using dimensions presented in **Table 3.16** with the help of PTM.

The calculation of CNT based parameters value of R, L, C has been done with the help Carbon Nanotube Interconnect Analyzer (CNIA Tool) provided by Nano-Hub. Org [114-115]. Transmission line based Model using characteristic impedance [116] has been used for calculation of delay parameter of Al, Cu and CNT material in 45nm Technology node.

Table 3.16 Dimensions Used for Calculation of Electrical Parameters of CNT & Cu at CNIA & PTM

Parameters →Technology node		Width	Thickness	Spacing	Height	Dielectric const
45nm	Local	68nm	136nm	68nm	136nm	2.1
	Intermediate	95nm	240nm	95nm	136nm	2.1
	Global	310nm	820nm	310nm	136nm	2.1

Table 3.17 Comparison between Present and Existing Work at 45nm (Without DSM condition)

Interconnect Lengths (µm)	Interconnects Delay for 45nm technology Node						
	Present Work			Ref. [22]			Reduction Improvement in Present Work (CNT) than Ref. [22] (CNT) %
	Al Delay (ns)	Cu Delay (ns)	CNT Delay (ns)	Al Delay (ns)	Cu Delay (ns)	CNT Delay (ns)	
10	0.000045	0.000037	0.00007	0.000056	0.000048	0.000104	32.69
50	0.000706	0.000516	0.00038	0.000745	0.000566	0.000553	31.28
100	0.002498	0.001791	0.000831	0.0025	0.001851	0.001173	29.16
500	0.026074	0.018665	0.004289	0.024829	0.018271	0.00616	30.37
750	0.054243	0.039149	0.009142	0.050383	0.037296	0.011771	22.33
1000	0.090636	0.065906	0.013714	0.082889	0.06166	0.017111	19.85
5000	0.286767	0.206207	0.052564	0.274987	0.203215	0.071167	26.14
7500	0.601816	0.432954	0.089358	0.56218	0.414952	0.116602	23.36
10000	1.008322	0.730307	0.133034	0.926656	0.687107	0.168439	21.02

Materialistic comparison with Al/Cu/CNT at 45nm technology node is presented in **Table 3.17.**The average error between Analytical and SPICE simulation for CNT type material for Global interconnect 0.450% & Local and Intermediate 2.1% 3.9% respectively**.** It is found that CNT provides 81.78% reduction in delay w.r.t. to Al and 86.80% w.r.t. to Cu as reported in **Table 3.18.** In DSM the superiority factor current between voltage remains 66.66%, once the load is shorted at termination end. CM dissipates 0.015pJ energy whereas VM consume

0.045pJ for single bit transmission across the interconnect using CNT material. Superiority factor matches with theoretical calculation i.e approximately three times. It means CM signalling is three time superior than VM signalling.

Table 3.18 Material Based Comparison at 45nm Technology Node

Interconnect Lengths (μm)		Material based comparison of proposed model at 45nm						
		Present Work						% Reduction using Proposed model CNT v/s AL
		Al Delay (ns)	Cu Delay (ns)	CNT Delay (ns)	Simulation CNT (ns)	% Error Col.4 v/s Col. 5	% Reduction using Proposed model CNT v/s Cu	
Local	10	0.000045	0.000037	0.00007	0.00007	0	89.189	55.555
	50	0.000706	0.000516	0.00038	0.000392	3.1	26.356	46.175
	100	0.002498	0.001791	0.000831	0.000859	3.3	53.601	66.733
Int.	500	0.026074	0.018665	0.004289	0.00442	3.0	77.021	83.550
	750	0.054243	0.039149	0.009142	0.009515	4.0	76.648	83.146
	1000	0.090636	0.065906	0.013714	0.01438	4.8	79.191	84.869
Global	5000	0.286767	0.206207	0.052564	0.053204	1.2	74.509	81.670
	7500	0.601816	0.432954	0.089358	0.090336	1.0	79.360	85.151
	10000	1.008322	0.730307	0.133034	0.1327	0.2	81.783	86.806

Table 3.19 Comparison Between Voltage and Current Mode Interconnect Delay Using CNT Material at 45nm in DSM when $\tau_{int} > \tau_{gate}$ then $R_{int} > R_S$ *or* $R_1 > R_S$

Length (μm)	Interconnect	CM delay (ps) $_{R_L=0}$	VM delay (ps) $_{R_L=\infty}$	% of Reduction Col.2 v/s Col.3
10		0.0238	0.071	66.48
50	Local	0.130	0.391	66.75
100		0.286	0.858	66.67
500		1.472	4.418	66.68
750	Intermediate	3.171	9.514	66.67
1000		4.798	14.394	66.67
5000		17.999	53.999	66.67
7500	Global	31.030	93.090	66.67
10000		46.245	138.737	66.67

With the CNT material the current mode delay is reduced by 67% than VM using transmission line approach.It is found that CNT provides 81.78% reduction in delay w.r.t. to

Al and 86.80% w.r.t. to Cu. And throughput comparison is also reported in **Fig. 3.48** with the variation of length of interconnect.

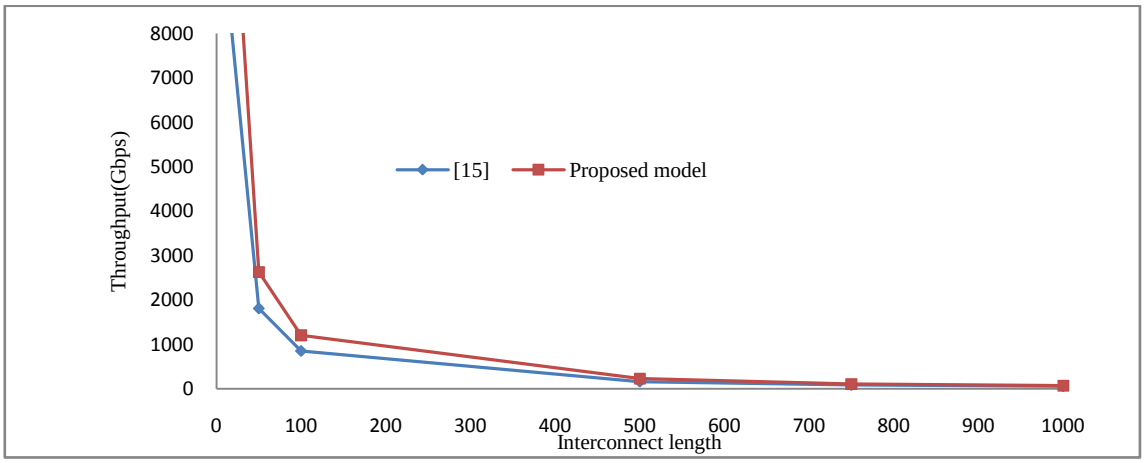


Fig. 3.48 Throughput with the length of interconnect for CNT materials.

3.10 Power Dissipation Model for Current Mode Circuits

There are three primary sources of power dissipation in current-mode circuits: static, dynamic and short-circuit power dissipation. Typically, the major component is the static power dissipation that arises from the constant current path from V_{DD} to ground via the resistive termination R_L. The dynamic power is dissipated when the capacitive components are charged through the PMOS device and discharged via the NMOS device. The third source of power dissipation arises from the finite input signal edge rates that result in short-circuit current. By, careful control of input edge rates can minimize the short-circuit current component to within 20% of the total dynamic power dissipation. The dynamic power dissipation of current-mode circuits can be modelled by the well-known [33] equation $P_{dyn}=V_{DD}^2 C_T f$, because it assumes that all the capacitive components of the distributed *RC* line are charged to V_{DD}. As illustrated in **Fig. 3.49**, the voltage at any point of a resistively terminated line will be less than V_{DD}, which results in a smaller dynamic power dissipation component.

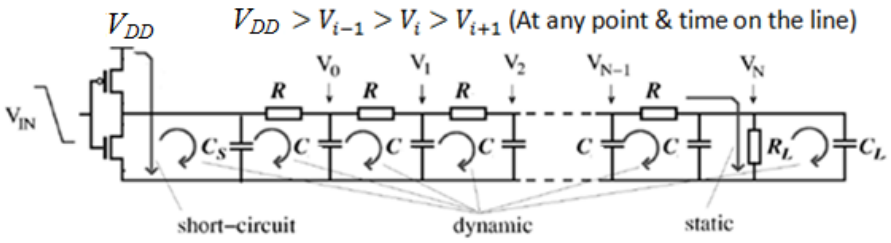


Fig 3.49 Power dissipation analysis of current-mode interconnects signalling.

As we are interested in reducing the voltage swing of output node of driver due to result of that the dynamic power dissipation which is dependent on output swing i.e. is V_{DD}. So if the swing of the output node is decrease to a larger extend or approximately equal to zero. Due to it the dynamic power dissipation across the interconnect line is reduce drastically comparative to voltage mode. Since, the dynamic power is very small because the large wire capacitance charge and discharge to only very small voltage swings.

$$P_{dyn} = V.\Delta V.C_{Tot}f \tag{3.114}$$

Where $C_{Tot} = C_S + C_T + C_L$ and f is input frequency signal. In ideal case of voltage mode signalling due to the full wing on the line, the capacitance associated with the line will charge for small value, or having minimum capacitance, which can be neglected.

V is the full swing applied voltage, ΔV is the change in voltage swing on the line, as the swing on the interconnect line is reduced, due to it the input signal edge rate to the receiver is very small, so the short-circuit power dissipation component will be fraction of the total of dynamic power dissipation [21], [109].

But there will be a static power dissipation which is the major component of power dissipation in current mode circuit. It is because of a low resistance path from driver to receiver. It is given by

$$P_{static} = I^2 R_{Total} \tag{3.115}$$

$$P_{static} = V.\frac{\Delta V}{R_S + R_T + R_L} \tag{3.116}$$

$\Delta V$is the change in voltage swing on the line, R_S is the source resistance, R_T is the total line resistance and R_L is the load resistance, V is the full swing applied voltage.

Hence, the total power dissipation in current mode signalling

$$P_T = P_{static} + P_{dyn}$$

$$P_T = V.\frac{\Delta V}{R_S + R_T + R_L} + V.\Delta V(C_S + C_T + C_L).f \tag{3.117}$$

The short circuit power component exists due to the flow of direct current between supply rails. This is approximated as the fraction of total dynamic power component, the value of x ranges from 0.1 to 0.2 [21], [60].The complete system of current mode interconnect system consist of driver, line of interconnect and receiver circuitry with decoding unit as shown below in **Fig.3.50**.

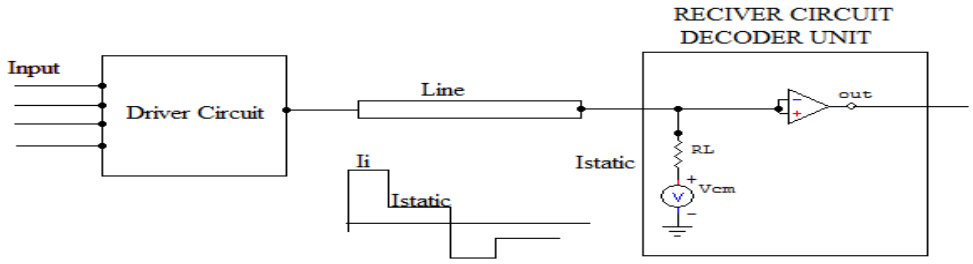


Fig. 3.50 Current mode interconnect system with driver and receiver

If we hold the voltage on the interconnect Fixed

$\Delta V \cong 0, While\ \Delta I \neq 0$

⇩

Need of Low input Impedance Receiver

⇩

C1. No Voltage Swing on the wire

⇩

C2. So Dynamic Power Dissipation is negligible

⇩

C3. Less Charging & Discharging of Interconnect Capacitance

⇩

Advantage: Wire Delay is Much lower

⇩

1. Short Circuit Power Dissipation is almost equal to Zero because of drastic change in signal swing (Input Signal Edge rate to the receiver is very small)

2. CM circuit have a flow of static current from transmitter to receiver because of low

resistance path, So static PD exists in CM

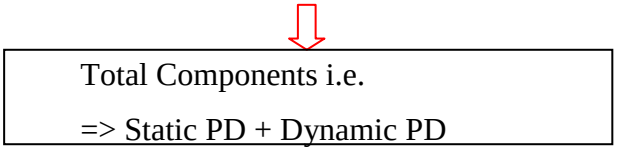


Fig. 3.51 Flow Graph for Power Analysis.

On the basis of flow graph analysis the dynamic and static power are estimated and found within the limits of above assumptions for current mode signaling. The calculation of above power dissipations using the approximated formulation as in equation (3.114) & (3.115) for the proposed modeling is presented below in the **Table 3.20.** Separately for voltage mode scheme and current mode scheme, with different design parameters.

Table 3.20 Comparison between Static and Dynamic Power Dissipation for Voltage and Current Mode Systems at 180nm Technology Node

Length (mm)	**Voltage Mode** $V_{DD} = 1.8V, R_S = 10\Omega, R_L = 1k\Omega$ $f = 1GHz, \Delta V = 1.8V$		**Current Mode** $V_{DD} = 1.8V, R_S = 10\Omega, R_L = 10\Omega, \Delta V = 210mV, f = 1GHz$	
	Static P.D(mW)	Dynamic P.D(mW)	Static P.D(mW)	Dynamic P.D(mW)
2	3.07	1.57	6	0.184
4	2.95	3.159	3.5	0.368
6	2.83	4.736	2.48	0.552
8	2.73	6.318	1.92	0.737
10	2.63	7.895	1.57	0.921
Average	**2.84**	**4.735**	**3.094**	**0.552**
On Comp.	Lower	Higher	**Dominant**	**Reduced**

From the above table it is clear that dynamic power dissipation component by using current mode signaling technique has reduced drastically as shown above i.e. average power is coming 0.552mW in CM whereas in voltage mode the same dynamic power component is dominating drastically and average value approaches 4.735mW in VM. Hence, it is really a good technique in terms of the saving the power or avoiding excess power dissipation in the clock network& global buses used in microcontrollers/microprocessors. Similarly static power dissipation component in current mode signaling is dominating due to the low

resistance path or low impedance termination at the load end as shown in the **Table 3.20.** For current mode signaling the average value of power dissipation is going to be 3.09mW whereas the average value of same power component in voltage mode signaling is 2.84mW. The above shows clearly, about the dominance of static power dissipation in current mode circuits. In the next section the various techniques are proposed for minimization of static power component in current mode circuits. Various results using SPICE and MATLAB simulation are presented below for verification of above facts.

For estimation of voltage swing on the interconnect line for different schemes with different value of load impedance are plotted using transient analysis with $C_L = 10fF, R_S = 10\Omega$ by the proposed Model II R_0C_0 are reported in **Fig. 3.51**. The case of full swing and low swing both are included in **Fig. 3.52.** After observation of results, it will not be difficult to designer to identify the low swing system, which helps in controlling the dynamic power component on the line.

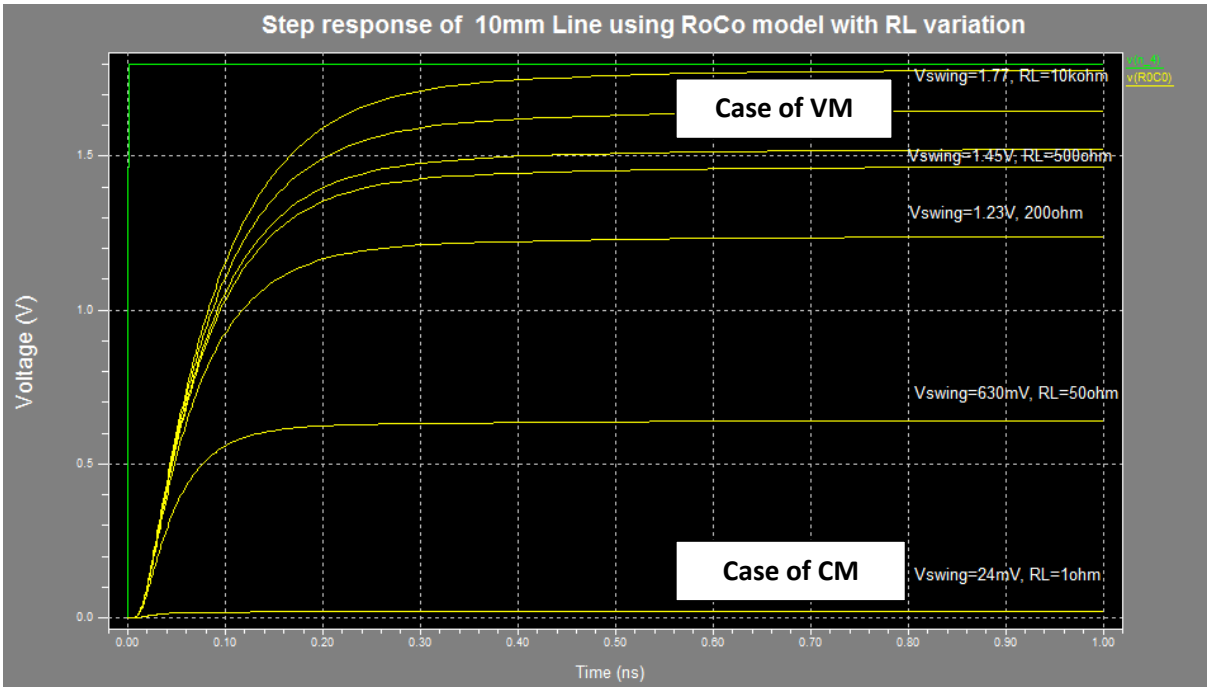


Fig. 3.52 Voltage swing analysis forVM and CM scheme

For different value of load impedance the corresponding voltage swing is first estimated for calculation of dynamic Power component on the interconnect line by taking the frequency of input signal of 1GHz, and the value of source resistance and load capacitance taken as 1Ω & $C_L = 10fF$ respectively.

Results calculated and reported in **Fig. 3.52** for both the cases of voltage mode and current scheme. Due to the nature of low impedance termination the circuits dissipates low of amount of power dissipation. But the high impedance termination is again to responsible for large amount of power dissipation in the network. The comparison of dynamic power in case of proposed Model II & Model III are reported in **Fig. 3.53** including comparison with existing Model reported in research paper [21]. The proposed Model III still shows better performance. The termination networks in both the schemes of VM and CM are reported in **Fig. 3.54**. Gate of MOS transistor is responsible for attaining high impedance in VM schemes. And drain gate connected configuration is fundamental in attaining low impedance in CM schemes

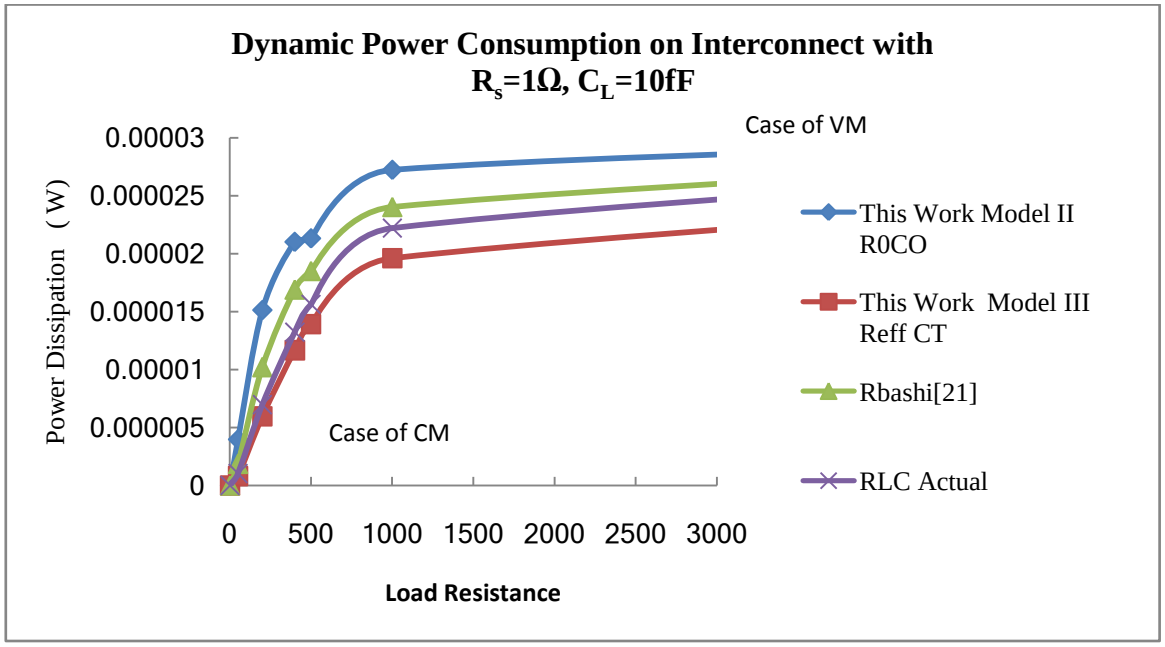
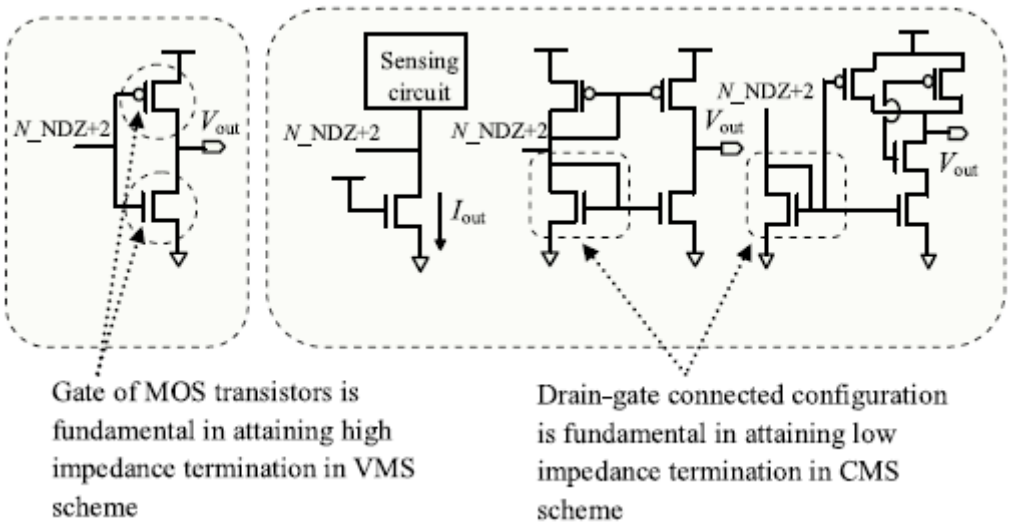


Fig.3.53 Dynamic power comparisons for various models



(a) (b)

Fig.3.54 Termination circuit can be equivalent as (a) VM scheme with high impedance (b) CM scheme with low Impedance

Further the applicability of low swing is explored and discussed in the chapter 5.

3.11 Static Leakage is Dominant in CM systems

As in previous section we observed that the current mode systems are static leakage dominant. So in this section following techniques are proposed for controlling the leakage component in Driver & receiver circuit in Current Mode Systems:-

Solution Proposed for Static Leakage Control in Current Mode System:-

- Forcing the optimum Bulk Signal
- Using Stacking technique
- Using Self Bias optimum bulk technique in driver receiver circuit
- Reducing the switching activity on interconnect line:-i.e. by using the encoding technique (Binary to Grey converted signal propagated on the line) will increase area and power dissipation of driver and receiver circuitry but it will reduce the major power dissipation on interconnect Line.
- To be applied on distributed line for reduction of switching activity factor

In this section the technique of optimum bulk, stacking driver circuit & optimum bulk with self bias transistors are explored as the driver circuitry of current mode systems and comparison are presented.

3.10.1 Modeling of Optimum Bulk Signal for NMOS/PMOS Device

(a) Determination of Optimum Reverse Bias

If the body of MOS transistor is more forward biased there will be excessive sub-threshold leakage adding to the total leakage. If the body is more reverse biased there will be excessive band to band tunneling current (BTBT), also increasing the total leakage. The location of this minimum leakage value is highly technology dependent. A circuit trades off sub-threshold leakage with band-to-band tunneling leakage at the active regions source/drain junctions to determine the optimal substrate bias for different technology generations and under process variations.

When a positive substrate voltage is applied to the p-MOS substrate, the power dissipation first decreases upto some value of $V_{bs}$and then it starts to rise as reported in **Fig. 3.55**. This value (which is 3.6 V in this case- Simulation is done using 180 nm technology at supply voltage, V_{dd}=1.8V) of V_{bs} gives the optimum RBB (Reverse body bias) value for p-MOS. But the supply voltage available is 1.8V. So, the optimum V_{bs} value is chosen as 1.8V (instead of 3.6V).

Similarly, when a negative voltage is applied to n-MOS substrate, as the value of V_{bs} becomes more negative, power dissipation decreases and becomes minimum at V_{bs}= -0.6V as reported in **Fig. 3.56**. A further decrease of V_{bs} leads to an increase in power dissipation. This gives optimum value of RBB for n-MOS.

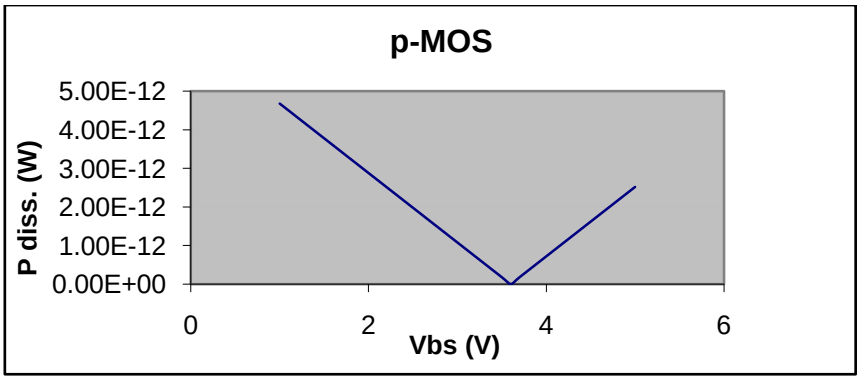


Fig. 3.55 Power dissipation as a function of substrate to source voltage applied (for p-MOS)

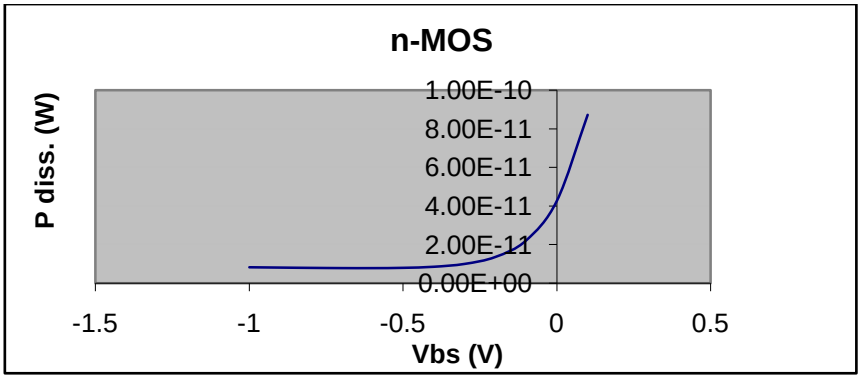


Fig. 3.56 Power dissipation as a function of substrate to source voltage applied (for n-MOS)

Mathematical analysis shows that for n-MOS device $V_B < 0.72$ V and for p-MOS device $V_B < 2.52$ V (in order to make value of V_T in equation (3.118) a real quantity)

$$V_T = V_{T0} + \gamma \left(\sqrt{(|2\Phi_F| + V_{SB})} - \sqrt{|2\Phi_F} \right) \quad (3.118)$$

For an n-MOS device, V_T will be a real number if$(|2\Phi_F| + V_{SB})$ is a positive number and becomes imaginary, when $(|2\Phi_F| + V_{SB})$ is negative. Hence,

$(|2\Phi_F| + V_{SB}) > 0$ for V_T to be a real number,

$\Rightarrow |2\Phi_F| > (- V_{SB})$

$\Rightarrow |2\Phi_F| > V_{BS}$

$\Rightarrow 0.72 \text{ V} > V_B - V_S$ (Since, $|2\Phi_F|$=0.72 V, From model file parameters)

$\Rightarrow V_B < 0.72$ V (since $V_S = 0$ V as the source of n-MOS device is connected to ground)

Similarly for a p-MOS device, V_T will be a real number if$(|2\Phi_F| + V_{SB})$ is a positive number and becomes imaginary, when $(|2\Phi_F| + V_{SB})$ is negative. Hence,

$(|2\Phi_F| + V_{SB}) > 0$ for V_T to be a real number,

$\Rightarrow |2\Phi_F| > (- V_{SB})$

$\Rightarrow |2\Phi_F| > V_{BS}$

$\Rightarrow 0.72\text{V} > V_B - V_S$

$\Rightarrow$ 0.72V > V_B – 1.8V (since V_S = 1.8V as the source of p-MOS device is connected to supply voltage, V_{DD})

$\Rightarrow V_B < 2.52$ V

For a CMOS inverter the variation of V_T when V_{BS} is varied is shown in Table 4. When RBB is applied, V_T value increases.

Mathematically, the threshold voltage of a CMOS inverter is given by

$$V_T = \frac{V_{t,n} + \sqrt{K_p/K_n}\,(V_{DD} + V_{t,p})}{1 + \sqrt{K_p/K_n}}$$

(3.119)

When no bias is applied to n-MOS as well as p-MOS, substituting $V_{t,n}$= 0.38V, K_p/K_n= 35.4/170.2 = 0.21, V_{DD} = 1.8V, $V_{t,p}$ = -0.42V (From Model file parameters), in equation(3.120), the value of V_T is found to be 0.694 V.

$$V_T = \frac{\mathrm{Vto,n} + \sqrt{Kp/Kn}\,(\mathrm{VDD} + \mathrm{Vto,p})}{1 + \sqrt{Kp/Kn}}$$

(3.120)

However, when RBB is applied to n-MOS (V_{bs}= -0.6V) and p-MOS (V_{bs}= 1.8V), using equation (3.118) the value of $\mathrm{Vt,n}$ is found to be equal to 0.545V by substituting V_{T0} =0.38V, $\gamma = 0.55\sqrt{V}$, $|2\Phi_F|$= 0.72V and V_{SB}=0.6V. Also, $V_{t,p} = V_{to,p}$ as V_{SB}=0V.

Now using equation (3.119) V_T comes out to be equal to 0.81V by substituting $V_{t,n}$=0.545V.

Table 3.21 Threshold Voltage for Inverter with and Without RBB Applied

V_{BS}	V_T (By Simulation)	V_T (Mathematically)
0V	0.74 V	0.694 V
Applied	0.82 V	0.81 V

The standard logic gates show a decrease in standby power dissipation when the optimized reverse body bias is applied to substrate.

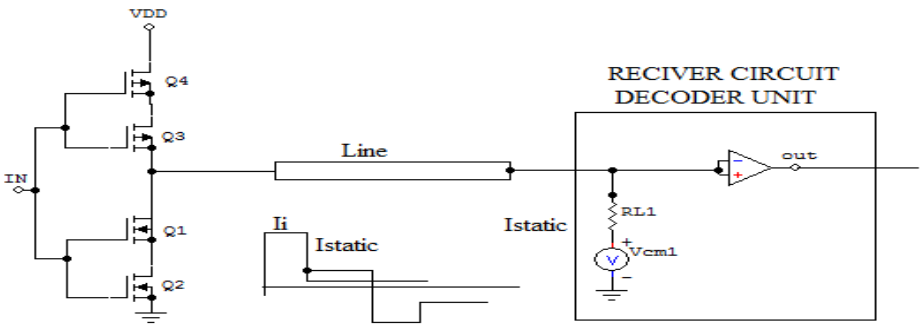
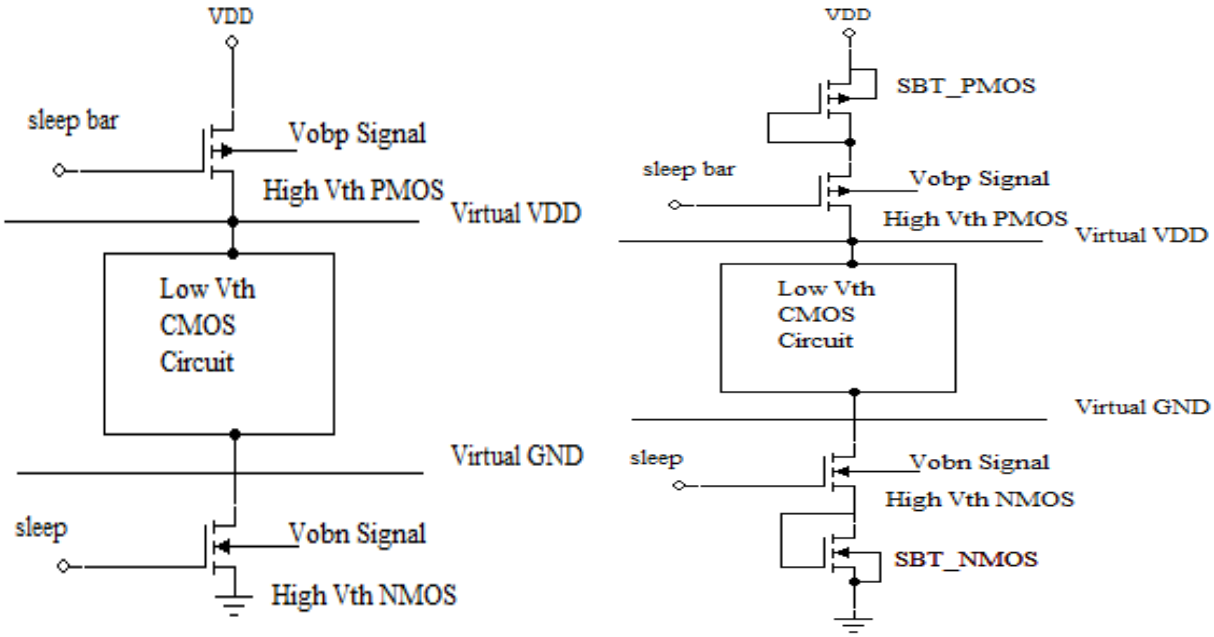


Fig. 3.57 Proposed stacking driver system for CM signalling

This optimised reverse body bias is utilized in driver and receiver part of current mode system with stacking topology reported in **Fig. 3.57** for reduction of standby leakage current from driver through interconnect line in resistive load termination. i.e. name as I_{static} .

Simplest CMOS inverter can be modified as shown in **Fig. 3.57** for stacking driver. In table 3.22 NAND Gate as driver circuit is used and results for static power dissipation are reported. With the application of optimum bulk signal the static component is reduced by 50.9% but parallel delay component is increased by a factor of 2.2 times. Using a SBT transistor a gate drain shorted NMOS/PMOS is connected as shown in **Fig. 3.58**. With the use of SBT transistor with optimum bulk signal the static power dissipation is reduced by 35.75% reported in **Table 3.22**.



Modified with optimum bulk (a)

(b) Modified with Self Bias transistor (SBT) optimum bulk

Fig. 3.58 Driver circuit for CM scheme using optimum bulk and self bias transistor (SBT).

Table 3.22 Static Power Dissipation for NAND Gate as Driver Circuit for CM in 180nm

NAND Gate power	Conv. CMOS NAND	**Optimum NAND**	Comparison (%)	With SBT	**This Work SBT NAND Optimum**	Comparison (%)
Static (00) (pW)	9.387	4.609	50.900	6.679	4.291	35.753
Delay (ns)	0.288	0.634	2.2 x More	1.20	4.12	3.4 x More

Table 3.23 Static Leakage Current & Thresholdvoltage of NANDas Driver Circuit in CM

Leakage current	Conv. NAND		**Optimum. NAND**		SBT NAND		**This Work SBT NAND optimum**	
	I_{ststic} (pA)	V_{TH} (mV)	I_{ststic} (A)	V_{TH} (mV)	I_{ststic} (pA)	V_{TH} (mV)	I_{ststic} (A)	V_{TH} (mV)
NMOS_1	5.037	436.18	81.05f	581.05	3.472	435.80	58.81f	581.27
NMOS_2	1.790	416.37	7.709e-25	580.54	474.55	417.51	9.058e-25	580.90
PMOS_1	-2.607	-509.51	579.73f	-962.82	-1.855	-509.51	607.85f	-962.82
PMOS_2	-2.607	-509.51	579.73f	-962.82	-1.855	-509.51	607.85f	-962.82

Table 3.22 presents the static leakage component in conventional NAND driver circuit and this value is reduced with the implementation of optimum bulk signal in NMOS & PMOS device separately. Correspond the threshold voltage of each device is increase as observed from **Table 3.23.** This reduction in static current leads to reduction in overall static power dissipation. Further the same is reduced by implementing with SBT technique as reported in **Table 3.23.** So SBT technique is also better option to minimize the leakage component.By the proposed technique the static power dissipation is reduced upto 35% in driver circuitry of Current Mode System.

3.12 Summary

In this chapter after making the assumption of signal transmission in deep submicron regime (DSM) for global interconnect i.e. the interconnection delay is dominant over the gate delay in deep submicron regime. It is because of the global wire interconnection resistance is very high when compare to output resistance of a driving gate. This assumption makes the three times improvement in delay for current mode over the voltage mode. Similarly, for the advantage in power dissipation the voltage swing over the interconnect line is kept very small, due to which the signal edge transition rate will decrease results in very small short circuit power dissipation and dynamic power dissipation over the interconnect line. Keeping receiving termination input impedance as low, provide better response in term of bandwidth increment. Further the static leakage component which dominant in current mode systems has been reduced by the technique of modeling the optimum bulk signal and with the help of Self bias transistor (SBT) technique. Tremendous improvement in static leakage current and power dissipation is recorded and reported in this chapter.

Chapter 4

MODELLING OF HIGHER ORDER SYSTEM USING TRANSMISSION LINE AND FOURIER METHOD

4.1 INTRODUCTION

Continuous technology miniaturization has facilitated high density chips leading to performance enhancement and more functionality. This has however led to increase in on-chip interconnect lengths. Consequently, interconnect delays have tremendously surged [117-118]. Hence, the need for research studies and modeling interconnects has become inevitable. Interconnect in integrated circuits is basically a wiring system used to distribute clock and other signals as well as to provide power or ground to various functional blocks [79]. Interconnects are broadly classified as local, semi-global and global interconnects. Local wires are very short and thin lines connecting logic gates within a functional block. Semi-global are generally considered sub-part of global wires. Global wires are wider and significantly longer as compared to local wires. The length of global interconnects range in milli-meters. Global wires are used to provide supply, ground and signals between functional blocks across the entire chip [79].

Although, technology scaling has helped reduce the gate delay extensively but simultaneously the interconnect delay has become more and more prominent which was ignored in earlier times. In the past, interconnects were modeled as a lumped capacitance [48]. With device scaling, interconnect cross-sectional area has also been scaled down [119]. In case of local wires, length is also getting reduced along with cross-sectional area because spacing between discrete components decreases. Hence, local wires merely affect the resistance and there by delay. The length of global wires is increasing due to increase in die size. Hence, its resistance is significantly increasing. The inter-metal layer space reduction is due to the use of wider wires for global interconnect. This results in increase in its capacitance [119]. These two factors have contributed to longer delays in global wires.

The adoption of low resistance materials to improve performance as well as working in GHz frequencies and faster rise times for high speed systems have made reactive component comparable to resistive component (i.e. $Z=R+j\omega L$) [120]. This has led to the emergence of

inductive effects such as overshoot/undershoot, inductive crosstalk etc. that can adversely affect signal integrity and reliability of the circuit [120]. Hence, inclusion of inductor in the interconnect modeling has become necessary to acknowledge inductive effect. Thus, there is an urgent requirement to model interconnects taking its impedance (inductive parasitics) into consideration to accurately determine its delay, inductance effect and various other effects on the logic circuits.

There is a recent trend of switching to low resistant materials with low k dielectrics for interconnects to achieve better speed or performance. For reliability purpose, interconnect material should be capable of carrying high current density as well as stability against thermal annealing, resistance against corrosion and good mechanical properties [121]. Historically, Aluminum (Al) has been used as interconnect material with SiO_2 as the dielectric due to its low resistivity as well as ease of deposition on Si and good adhesion to SiO_2. It does not contaminate Si wafer. But with technology shrinkage to sub-micron range, Al started to suffer from electro-migration due to its low activation energy (E_a) and low current carrying density (J) as mentioned in **Table 4.1** [121]. Electro-migration is the mass transport of a metal due to the momentum transfer between conducting electrons and metal atoms the activation energy is the minimum energy required for movement of an atom from a lattice position in a crystal. It causes voids and hillock formations between metal layers causing opens and short-circuits among the layers [122]. To overcome this problem, copper has been considered a better substitute because of its advantages over aluminum as given in **Table 4.1.**

Table 4.1 Comparison of Copper and Aluminum Properties [121]

Material	Resistivity (μΩ-cm at 20^{oC})	Melting point (^{O}C)	E_a for lattice diffusion (eV)	E_a for grain boundary diffusion (eV)
Al	2.67	660	1.4	0.4-0.8
Cu	1.68	1083	2.2	0.7-1.2

Due to high activation energy of copper wires, it can withstand upto five times more current density than aluminum wires [122]. Cu has not been used in prior technologies because of device reliability concerns as well as processing difficulties. Copper diffuses rapidly in

SiO_2in the presence of electric field which can contaminate Si wafer. The etching of Cu is very difficult [120]. To overcome these problems, trenches are patterned by first depositing ILD (inter-level dielectric) and then a barrier layer is deposited to resist Cu diffusion. On this barrier, Cu is deposited as shown in **Fig. 4.1** [120].

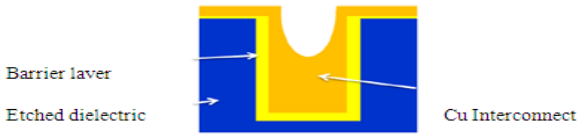


Fig. 4.1 Cross section schematic of trench showing the process of Cu deposition [120].

With technology advancement to deep sub-nanometer regime, copper has also started to suffer from electro-migration. Due to this, the occurrence of new phenomena such as grain boundary scattering and surface scattering have increased its resistivity as well as its resistance. Grain boundaries are the interfaces where crystals of different orientations meet. The difference in potential barrier at the grain boundary from the bulk causes scattering and reduces mobility. Surface scattering occurs when the cross section dimension of a wire becomes comparable to the mean free path of charge carriers [123]. The surface and grain boundary scattering resistivity is given by Fuchs and Sondheimer (FS), Mayadas and Shatzkes (MS) model respectively [123].

$$\frac{\rho_{gs}}{\rho_b} = \frac{1}{3[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)]} \tag{4.1}$$

Where, $$\alpha = (1/d_g)(p_{ns} + 1/p_{ns}) \tag{4.1a}$$

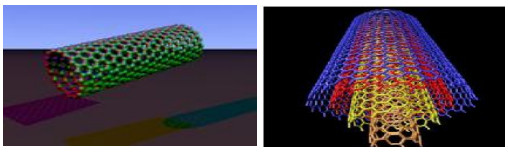
and

$$\frac{\rho_{ss}}{\rho_b} = 1 + \frac{3}{4}(1 - p_s)(\frac{l}{w}) \tag{4.2}$$

From equations (4.1) and (4.2), ρ_{gs} and ρ_{ss} are resistivity due to grain boundary and surface scattering respectively. ρ_b is the bulk resistivity. d_g is the average distance between grain boundaries and p_{ns} is the reflective coefficient denoting the fraction of electrons that are not scattered by the potential barrier at a grain boundary. p_s defines the fraction of electrons scattered specularly at the surface. l and w is MFP and wire width respectively.

The barrier layer does not scale as rapidly as the interconnect dimensions. Hence, the presence of high resistive barrier layer also worsens the effective resistivity of Cu [123].

More recently, carbon nanotubes (CNTs) have shown various improved electrical, thermal and mechanical properties as compared to Cu which has made them a promising candidate for future interconnects [124]. Carbon nanotubes are thick sheet of graphene rolled up into a seamless cylinder having very high aspect ratio (length/diameter) making it a quasi 1D structure [124]. CNTs are classified as single-walled (SWNTs) and multi-walled (MWNTs) carbon nanotube shown in **Fig. 4.2.** SWNTs have only one layer of graphene sheet with diameter in the range of 0.7 to 10 nm [93] [124-126]. Multi-walled carbon nanotubes consist of concentric CNT cylinders held within each other by Vander waals forces [124-128]. Its diameters range from a few to several hundred nanometers. The distance between shells is approximately 3.4Å which is the Vander waals distance for two graphite carbon lattices. For on-chip global interconnects, bundle of SWNTs and mixed SWNT/MWNTs are of recent attention dueto their superior properties [126]. In this chapter SWNT bundle is used for global interconnect modeling. An SWNT bundle consists of several SWNTs placed parallel to each other[126].



(a) (b)

Fig. 4.2 (a) SWNT, (b) MWNT [126].

CNTs can carry current density of approximately 4×10^{9} A/cm^2 which is three orders of magnitude higher than that of Cu [120]. Due to the presence of very stiff bond among carbon atoms i.e. sp^2 bond makes it highly inert and resistive to electro-migration because the activation energy required to break the bonds is very large with energy 7.7 eV [129-130]. It supports ballistic transport for longer range of length because of longer mean free path (MFP) which is given as MFP =1000d [130], where d is the diameter of the nanotube. **Table4.2** compares the properties of CNT with Cu [118]. At 22nm, current density is greater than 10^7A/cm^2 and copper tends to electro-migrate as its current density is limited to 10^7 A/cm^2 [120].

Section 4.2 covers the description of impedance equations for Cu and CNT interconnect. In Section 4.3, analytical modeling of Cu and CNT type of materials interconnect is modeled using Fourier analysis of periodic input signal and respective exact transfer functions. Closed

form solution of 50% delay and overshoot/undershoot formulation is also presented in this chapter.

Table 4.2 Comparison of Copper with CNT [120]

Parameters	**Copper at 22nm**	**CNT**
J (A/cm^2)	10^7	10^9
E_a (eV)	2.2	7
Temperature coefficient of ρ ($/^o$ C)	4×10^{-3}	-1.5×10^{-3}
Barrier layer	Required	Not required due to Sp^2 bond
MFP	40nm	1µm for $d = 1$nm
Thermal conductivity(W/mK)	400	6000

Comparison of approximated transfer functions used in various previous works with the exact transfer function is carried out in this chapter. Dependence of inductance effect on various parameters is discussed. SPICE set-up of Cu and CNT interconnect and comparison of SPICE with mathematical model is presented.

4.2 COPPER AND CNT IMPEDANCE RELATIONSHIPS

4.2.1 Parasitic of copper interconnect

Calculation of impedance of the interconnect requires its geometrical data. **Fig. 4.3** shows the cross-sectional view of the Cu interconnects in **Fig. 4.3** w and s are the width and spacing between metal layers respectively. l denotes the length. t specify the thickness of the wire and h is the height above the ground plane.

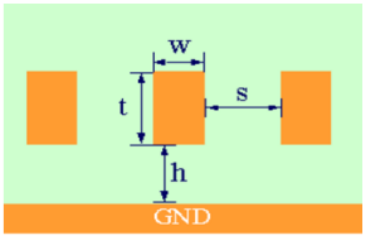


Fig. 4.3 Shows wire dimensions [108].

(i) Resistance: Resistance of a rectangular cross section is calculated using the standard equation [108] given as

$$R = \frac{\rho l}{wt} \tag{4.3}$$

where $\rho = \rho_{gs} + \rho_{ss}$

(ii) Capacitance: There are two types of capacitances in a single line. One is coupling capacitance *(C_C)* which is formed between two adjacent metal layers separated with a dielectric and the other is formed between the ground plane and the metal wire (C_g). Hence, total wire capacitance C_t [108] is given by equation (4.4) and shown in **Fig. 4.4.**

$$C_t = C_g + 2C_c \tag{4.4}$$

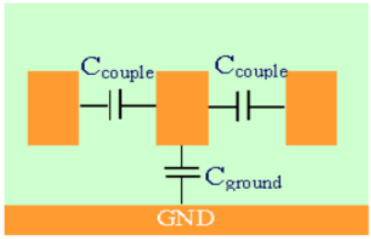


Fig. 4.4 Showing various capacitances between metal layers[108].

where,

$$C_g = \varepsilon[w/h + 2.22(s/(s + 0.7h))^{3.19} + 1.17(s/(s + 1.51h))^{.76}(t/(t + 4.53h))^{0.12}]$$

$$C_c = \varepsilon[\frac{1.41t}{s(h/(h + 2.6s))^{.09}} + .74(w/(w + 1.59s))^{1.14} + 1.16(w/(w + 1.87s))^{.16}(h/(h + 0.98s))^{0.12}] \tag{4.5}$$

(iii) Inductance: The inductance of the interconnect wire[108] can be expressed as reported in equation (4.6)

$$L_s = \frac{\mu_0 l}{2\pi}[\ln\left(\frac{2l}{W + t}\right) + \frac{1}{2} + \frac{0.22(W + t)}{l}] \tag{4.6}$$

4.2.2 Parasitics of SWNT bundle interconnect

An isolated SWNT can be represented by a RLC circuit where R, L& C values can be determined using the below mentioned equations derived from literature.

1) *Resistance:* The resistance of an isolated SWNT is very large and is divided into three categories viz. The fundamental/Quantum resistance, scattering resistance and the metal-nanotube imperfect contact resistance [124]. The fundamental resistance is given by the Landauer-Buttker formula [124] [131] &given by

$$R_{QSWNT} = h/4e^2 \tag{4.7}$$

and its value is about 6.45KΩ. This resistance is independent of length and appears as a lumped element. It is equally divided on either side of the nanotube. Scattering resistance comes into picture when the length of the interconnect becomes greater than the MFP length of the charge carriers. This longer length causes enhanced scattering. Scattering resistance [124] and given by equation (4.8)

$$R_{SSWNT} = h/4e^2(\frac{l}{\lambda}) \tag{4.8}$$

Where h is Planck's constant, $e$is the charge of an electron, $l$is the SWCNT length and $\lambda$is the MFP length. Scattering resistance distributes all along the length. Typically λ is taken 1μm. In this chapter, metal-nanotube contact resistance is taken ideal as the resistance arising from these imperfect contacts is often so high that it masks the observation of intrinsic transport properties [131]. Hence, total resistance is given by

$$R_{total} = R_{QSWNT} + R_{SSWNT} \tag{4.9}$$

2) *Capacitance:* Capacitance arises from three sources. First arises due to the quantum energy stored in the nanotube when it carries current known as Quantum capacitance (C_{QSWNT}) [124]. Quantum capacitance per unit length is given as

$$C_{QSWNT} = \frac{2e^2}{hv_F} \tag{4.10}$$

Where v_F is the Fermi velocity and $v_F$is approximated by≈ 8x10^5 m/s. An SWNT consists of four co-propagating quantum channels. Hence, the effective SWNT quantum capacitance is $4C_{QSWNT}$ [126]. The other two capacitances are electrostatic capacitance with the ground (C_{EGSWNT}) and coupling capacitance with any adjacent SWNTs (C_{ECSWNT}). The electrostatic capacitance per unit length between an SWNT and the ground plane is given by [126]

$$C_{EGSWNT} = 2\pi\varepsilon/cosh^{-1}(\frac{2h}{d})$$

(4.11)

Where h is the height of the nanotube above the ground and d is the diameter of the tube. ε is the permittivity of dielectric. Similarly, the coupling capacitance (C_{ECSWNT})per unit length is given as [126]

$$C_{ECSWNT} = \pi\varepsilon/cosh^{-1}(\frac{s}{d})$$

(4.12)

Where s is the inter-SWNT spacing. $4C_{QSWNT}$ appear in series with a parallel combination of C_{EGSWNT} and C_{ECSWNT} [126]. Hence, the total capacitance per unit length can be summarized as below in equation (4.13)

$$C_{total} = (C_{QSWNT} \times C_E)/(C_{QSWNT} + C_E)$$

(4.13)

Where $C_E = C_{EGSWNT} + C_{ECSWNT}$

3) *Inductance:* Two inductance associated with SWNT is kinetic inductance and magnetic inductance. The kinetic inductance (L_{KSWNT}) is due inertia of charge carriers since electrons do not instantaneously react to an applied voltage [126]. Kinetic inductance per unit length is given as

$$L_{KSWNT} = h/2e^2v_F$$

(4.14)

L_{KSWNT} per unit length evaluates approximately to 16nH/μm [124]. The effective kinetic inductance due to the presence of four parallel channels is $L_{KSWNT}/4$. The magnetic field produced between the ground plane and the tube give rise to magnetic inductance (L_{MSWNT}). The per unit length magnetic inductance [124]& given by equation (4.15)

$$L_{MSWNT} = \left(\frac{\mu}{2\pi}\right) / \ln\left(\frac{h}{d}\right)$$

(4.15)

Here, μ is the permeability. Hence, the total inductance per unit length is

$$L_{total} = L_{KSWNT}/4 + L_{MSWNT}$$

(4.16)

Since an isolated SWNT has very high resistance and inductance. Hence, bundling of SWNTS is done in which CNTs are placed in parallel to reduce its resistance and kinetic inductance as shown in **Fig. 4.5.**

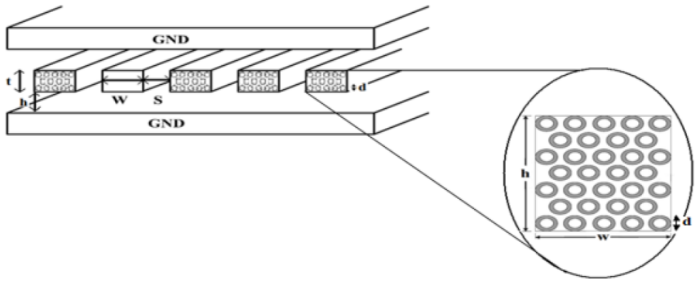


Fig. 4.5 The 2-D structural model of SWNT bundle interconnect.

The number of SWNTs [124] in a bundle can be found out by equation (4.17) as given below

$$n_{SWNT} = n_w n_t - (n_t - 1)/2; \quad \text{if } n_t \text{ is odd}$$
$$n_{SWNT} = n_w n_t - n_t/2; \quad \text{if } n_t \text{ is even} \tag{4.17}$$

where, n_w = number of vertical rows and n_h = number of horizontal rows. These are given as

$$n_w = \frac{w-d}{x}$$
$$n_h = \frac{t-d}{\sqrt{3}\frac{x}{2}} + 1 \tag{4.18}$$

where, x is the spacing between two CNTS in a bundle. In this work high density bundle SWNT ($x = d$) [124] is considered because it gives better performance in global wires [124]. The probability (P_m) [126] of tube to be metallic is considered as 1 which is the ideal case. Therefore the total resistance of SWNT bundle becomes [124]

$$R_{total-bundle} = (R_{QSWNT} + R_{SSWNT})/\, n_{SWNT} \tag{4.19}$$

Total inductance per unit length becomes [124]

$$L_{total-bundle} = L_{KSWNT}/4n_{SWNT} + L_{MSWNT} \tag{4.20}$$

As far as SWCNT bundle capacitance is concerned, the electrostatic and coupling capacitance occur mainly from the SWCNTs lying at the edges of the SWCNT bundle. These capacitances have been analyzed extensively in [126] by using Field Solver RAPHEL Tool & 3D Field Solver Fast Cap and Fast Henery. These are found to be equal to the respective capacitances of a Cu wire with the same cross-sectional dimensions. The effective quantum capacitance of a SWNT bundle is further reduced in a bundle and found to be negligible

compared to its electrostatic counterparts [126]. Equivalent circuit of SWCNT reported in **Fig. 4.6.**

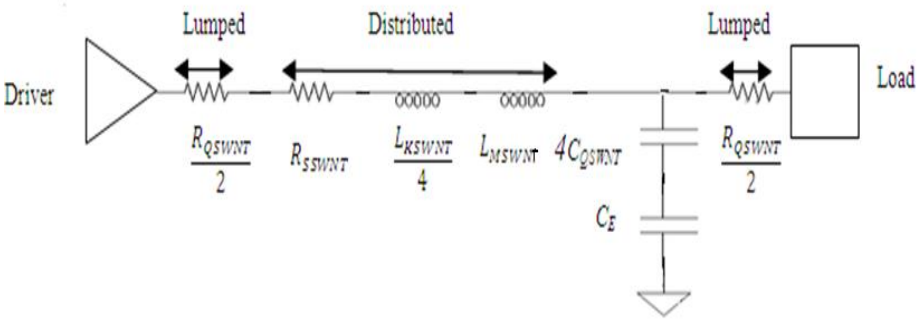


Fig. 4.6 Equivalent circuit diagram of SWCNT bundle.

By using the above electrical parameters of copper and SWCNT wires, analytical models are developed first and then analysis of transfer functions are reported in further sections.

4.3 ANALYTICAL MODELLING

4.3.1 Transfer function of Cu RLC interconnect

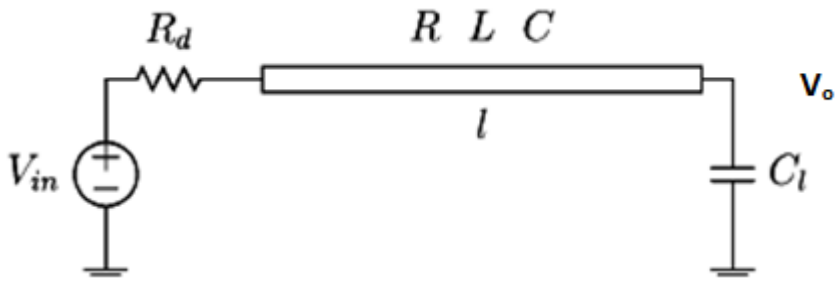


Fig. 4.7 Equivalent circuit model of a distributed copper *RLC* interconnect.

The frequency of operation in this work is taken in GHz and length in mille-meter range. Hence, the length becomes comparable or greater than the wavelength of the signal. Due to this, parasitic of interconnect get distributed all along the length and appear as a transmission line [48]. In **Fig.4.7** r, l, c are the resistance, inductance and capacitance per unit length of interconnect respectively. Therefore R= r $\times$ l Ω, L= l$\times$ l H and C= c$\times$ l F. Interconnect is excited by a voltage source serially connected with a driver resistance R_d. The load of the interconnect is capacitor C_l .This equivalent circuit is a linear time-invariant (LTI) system.

The ABCD parameters of the transmission line is given as

$$\begin{bmatrix} cosh\theta & Z_c sinh\theta \\ {Z_c}^{-1} sinh\theta & cosh\theta \end{bmatrix}$$

By using the above parameters, the above circuit model's input and output voltage and current can be represented as

$$\begin{bmatrix} V_{input} \\ I_{input} \end{bmatrix} = \begin{bmatrix} 1 & R_d \\ 0 & 1 \end{bmatrix} \begin{bmatrix} cosh\theta & Z_c sinh\theta \\ Z_c{}^{-1} sinh\theta & cosh\theta \end{bmatrix} \begin{bmatrix} 1 & C_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{output} \\ I_{output} \end{bmatrix}$$

Solving above, the exact transfer function at the far end of a line is given by equation (4.21)

$$H(s) = \frac{1}{\left[(1 + R_d C_l s)cosh\theta + \left(\frac{R_d}{Z_c} + Z_c C_l s\right) sinh\theta\right]}$$

where, $\theta = \sqrt{(R + sL)sC}$ and $Z_c = \sqrt{(R + sL)/sC}$.

The exact transfer function is compared with the approximated two pole transfer function reported in research paper [132-133] & four pole transfer function reported in research paper [134] and single L-type lumped model is also used to observe upto what frequency the approximated models are accurate when compared to exact transfer function reported in research paper[135]. When the hyperbolic function of exact transfer function of RLC interconnects is expanded into infinite series and is truncated upto two poles, we get the following two pole expression in equation (4.22)

$$H(s) = \frac{1}{[1 + sa + s^2 b]} \tag{4.22}$$

where

$a = R_d C_l + \frac{RC}{2} + R_d C + RC_l$ and

$b = \frac{R_d R C_l C}{2} + \frac{LC}{2} + \frac{R^2 C^2}{24} + LC_l + \frac{R_d R C^2}{6} + \frac{R^2 C_l C}{6}$

Similarly, the expression for four pole transfer function is presented in equation (4.23)

$$H(s) = \frac{1}{[1 + sa + s^2 b + s^3 e + s^4 f]} \tag{4.23}$$

where, a and b are same as defined above, the value of e & f is given below:

$$e = \frac{C^2 RL}{12} + \frac{R^3 C^3}{720} + \frac{LCR_d C_l}{2} + \frac{R_d C_l C^2 R^2}{24} + \frac{C_l RLC}{6} + \frac{C^2 L}{6} + \frac{RLCC_l}{6} + \frac{R_d R^2 C^3}{120} + \frac{R^3 C^2 C_l}{120}$$

$$f = \frac{C^2 L^2}{24} + \frac{C^3 R^2 L}{240} + \frac{C^2 R_d C_l RL}{12} + \frac{C^3 R^3 C_l R_d}{720} + \frac{CL^2 C_l}{6} + \frac{C^2 R^2 LC_l}{60} + \frac{RLC^3 R_d}{60} + \frac{R_d C^4 R^3}{5040} + \frac{C^3 R^4 C_l}{3050} + \frac{C^2 L^2}{24}$$

If we model a high frequency interconnect line with a single L-type lumped model, its transfer function is given as

$$H(s) = \frac{1}{[1 + s(R\_d + R)(C + C\_l) + s\text{^}2\,(L(C + C\_l)]}$$

(4.24)

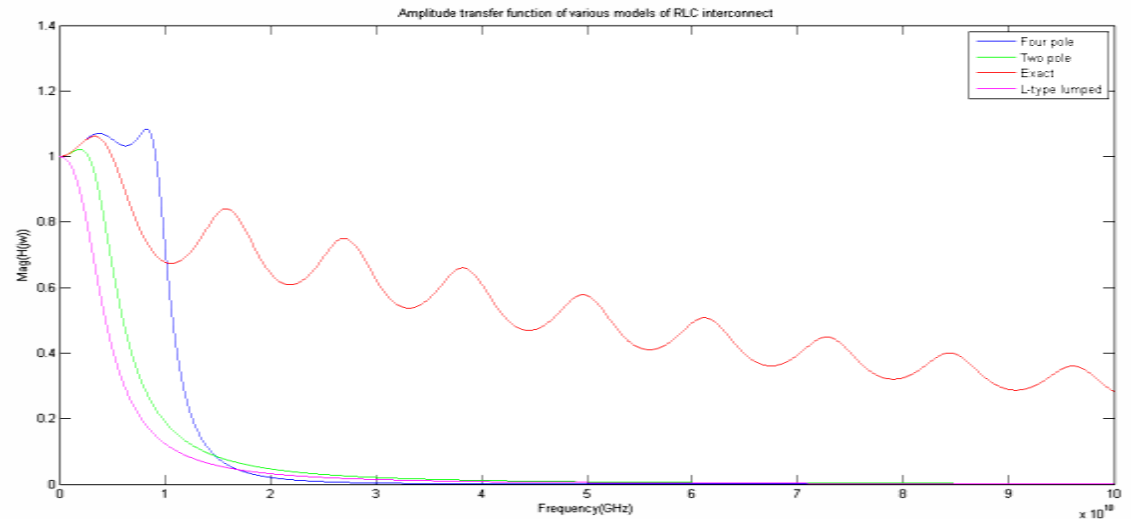


Fig. 4.8 (a)Amplitude transfer function of different models of copper interconnect (l=2000µm and at **65nm** Node,R_d and C_l is 30Ω and 50fF)

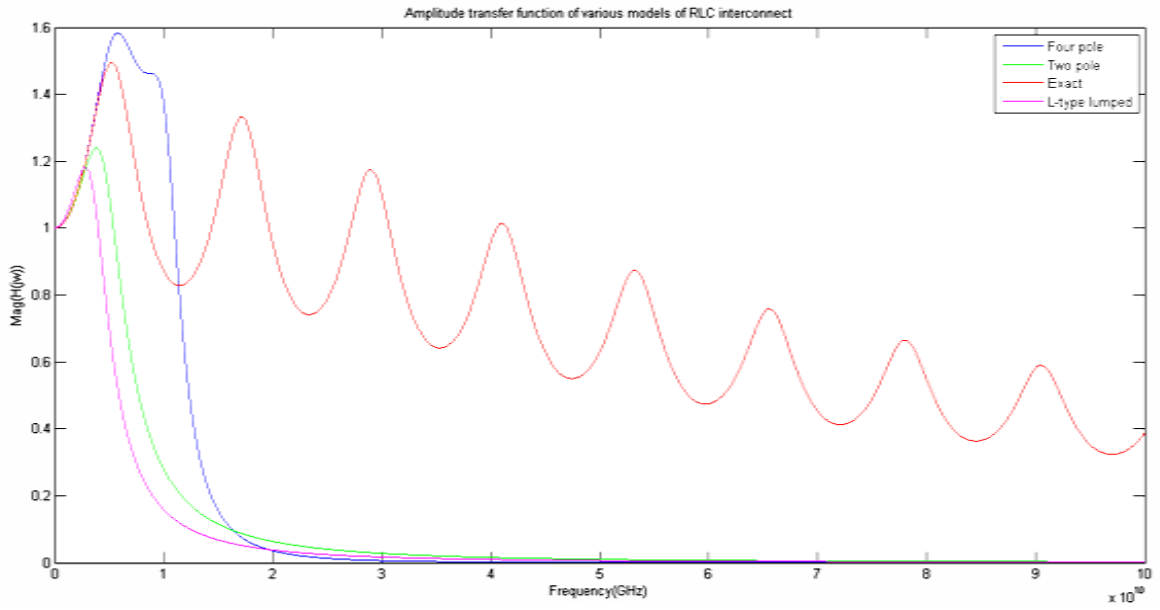


Fig. 4.8 (b) Amplitude transfer function of different models of and RLC copper interconnect. (l=2000µm and at **180nm** dimensions)

From **Fig. 4.8** (a) and **Fig. 4.8 (b)** it is observed that L- type lumped model shows the poorest approximation as compared to others and two pole model is accurate upto 5 GHz. Four pole

is accurate upto 9 GHz. Therefore, as the number of pole is increased in the RLC transfer function, it can follow the EXACT transfer function accurately for larger range of frequency as observed from the above plots of **Fig. 4.8** for copper type of material. Four pole transfer function plot is following the exact transfer for large of frequency. Maximum amplitude and inductive peaking is also decreased with technology scaling as observed from **Fig. 4.8 (a) & Fig. 4.8(b).**

4.3.2 Proposed Transfer function of SWCNT bundle RLC interconnect

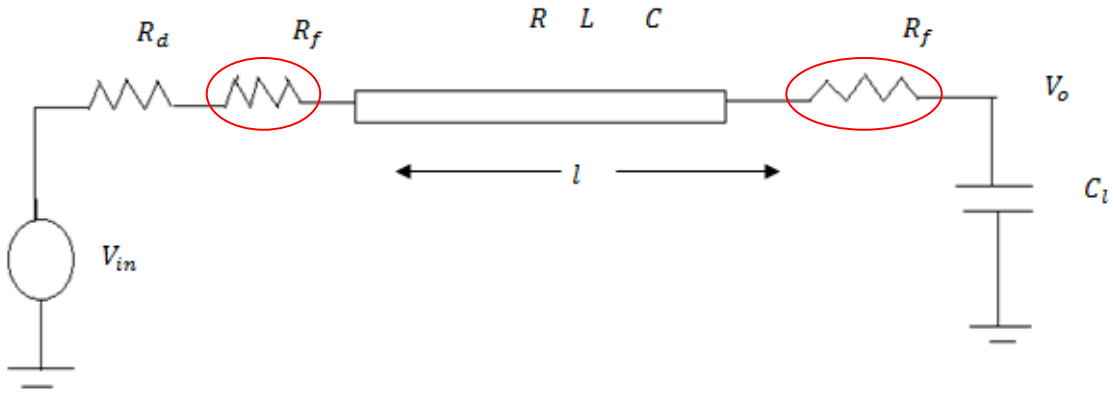


Fig. 4.9 Equivalent circuit model of a distributed *RLC* interconnect

In **Fig. 4.9**, R_{QSWNT} is the fundamental resistance of SWCNT. Other parameters are same as defined above in **Fig. 4.7**. Using the ABCD parameters of transmission line, the above circuit model's input and output voltage and current can be represented as:

$$\begin{bmatrix} V_{input} \\ I_{input} \end{bmatrix} = \begin{bmatrix} 1 & R_d + R_f \\ 0 & 1 \end{bmatrix} \begin{bmatrix} cosh\theta & Z_c sinh\theta \\ Z_c{}^{-1} sinh\theta & cosh\theta \end{bmatrix} \begin{bmatrix} 1 & R_f \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & C_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{output} \\ I_{output} \end{bmatrix}$$

Solving above, the exact transfer function from the input to the far end output of a line is given by equation (4.25)

$$H(s) = \frac{1}{\left[\left(1 + R_f C_l s + (R_f + R_d) C_l s\right) cosh\theta + \left(\frac{R_d + R_f}{Z_c} + \frac{s R_f C_l (R_f + R_d)}{Z_c} + Z_c C_l s\right) sinh\theta\right]} \quad (4.25)$$

where, $\theta = \sqrt{(R + sL)sC}$ and $Z_c = \sqrt{(R + sL)/sC}$

Two pole expressions from the above transfer function are given as in equation (4.26)

$$H(s) = \frac{1}{[1 + sa + s^2 b]}$$

(4.26)

where

$$a = \left(R_D + R_f\right) + RC_l + \frac{RC}{2} + C_l R_f + C_l\left(R_D + R_f\right)$$

$$b = LC_l + C_l C R_f\left(R_D + R_f\right) + \frac{1}{6}RC^2\left(R_D + R_f\right) + \frac{1}{6}R^2 C C_l + \frac{LC}{2} + \frac{R^2C^2}{24} + C_l\frac{R_f RC}{2} + \frac{RCC_l\left(R_D + R_f\right)}{2}$$

Similarly four pole expression from equation (4.25) is obtained as

$$H(s) = \frac{1}{[1 + sa + s^2 b + s^3 e + s^4 f]} \tag{27}$$

where

$$e = \frac{LC}{2}\left[\left(R_D + R_f\right)C + RC_l\right] + \frac{C^2R^2}{120}\left[\left(R_D + R_f\right)C + RC_l\right] + \frac{RC}{6}\left[C_l C R_f\left(R_D + R_f\right) + C_l L\right] + \frac{C^3RL}{12} + \frac{C^3R^3}{720} + \left(C_l R_f + C_l\left(R_D + R_f\right)\right)\left(\frac{LC}{2} + \frac{C^2R^2}{24}\right)$$

$$f = \left(C_l R_f + C_l\left(R_D + R_f\right)\right)\left(\frac{C^3RL}{12} + \frac{C^3R^3}{720}\right) + \frac{LC}{6}\left(C_l L + C_l C R_f\left(R_D + R_f\right)\right) + \frac{C^2R^2}{120}\left(C_l L + C_l C R_f\left(R_D + R_f\right)\right) + \frac{C^2RL}{60}\left(C_l L + C_l C R_f\left(R_D + R_f\right)\right) + \frac{C^3R^3}{5040}\left(C_l L + C_l C R_f\left(R_D + R_f\right)\right)$$

In the same way single L-type lumped model transfer function is given as in equation (4.28)

$$H(s) = \frac{1}{1 + s\left[C\left(R_D + R_f\right) + C_l\left(R_D + R_f\right) + C_l R_f\right] + s^2\left[C_l C R_f\left(R_D + R_f\right) + LC + C_l L\right] + s^3\left[C_l C R_f L\right]} \tag{4.28}$$

In **Fig. 4.10 (a)** the amplitude transfer function of SWCNT type of material is plotted for exact transfer function in 65nm Node, two pole, four pole, & L type lumped system functions. It is observed that for SWCNT type of material, four pole system functions is tracing the exact the transfer function with higher magnitudes of system functions, overshoots and undershoots. Four pole system is accurate upto 5GHz for SWCNT at 65nm node. But magnitude peaking is higher in case of SWCNT type of materials as compared to copper material reported in **Fig. 4.8 (a)** at 65nm Node.

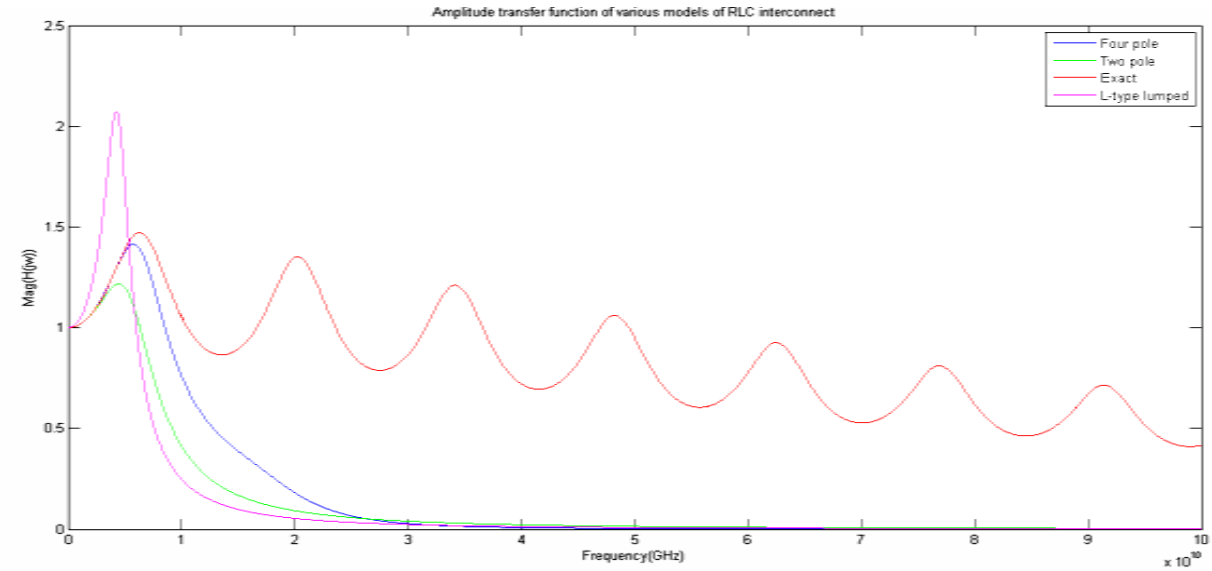


Fig. 4.10 (a) Amplitude transfer function of different models of SWCNT interconnect (l=2000µm and at **65nm** dimensions; R_d and C_l is 30Ω and 50fF)

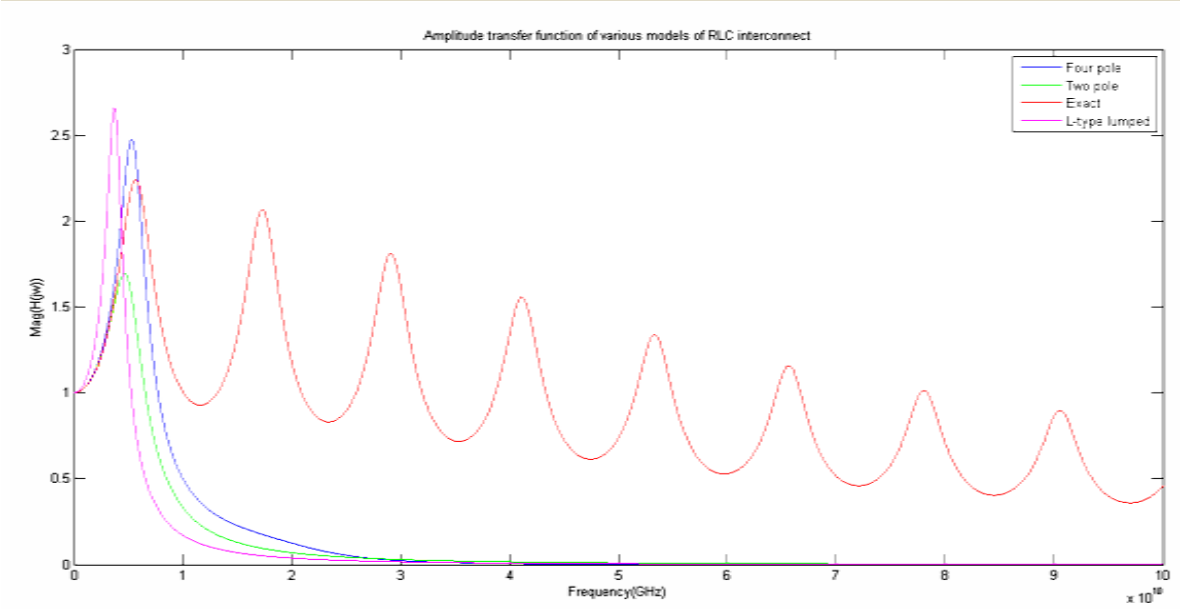


Fig. 4.10 (b) Amplitude transfer function of different models of and RLC SWCNT interconnect (l=2000µm and at **180nm** dimensions).

From **Fig. 4.10(b)**, it is observed that similar results are obtained in case of SWNT as for copper but magnitude peaking is higher in case of SWNT materials as observed from **Fig.4.10 (b).** But due to technology scaling resistance of wires increase and also the inductive peaking increases, is self-explanatory from the above results.

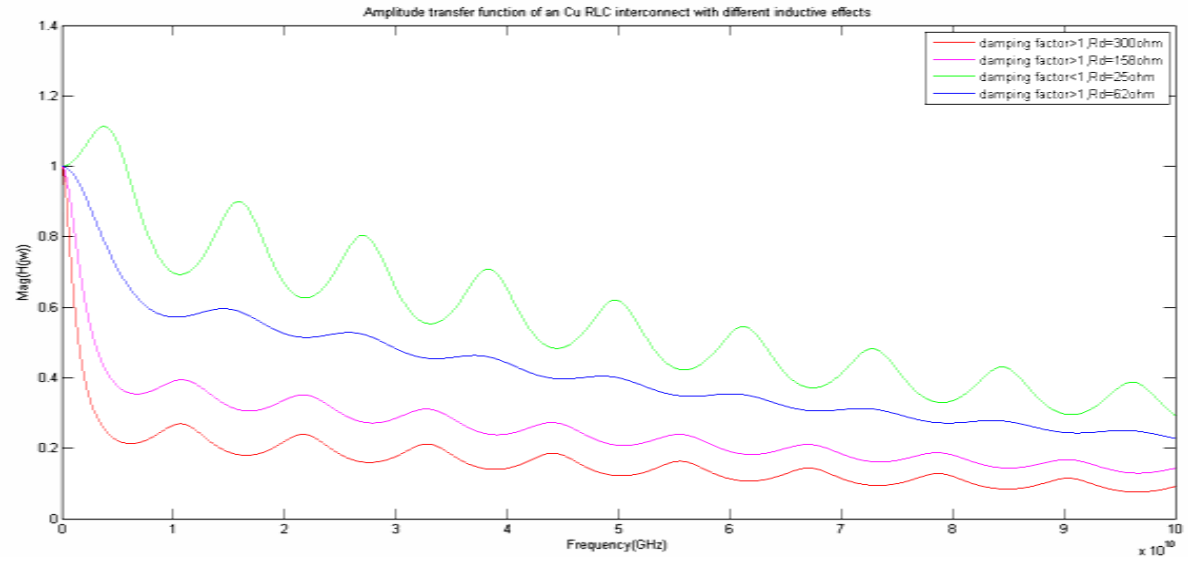
4.3.3 Dependence of Inductance effect on various parameters:

Due to strong inductive effect, reflections occur at the terminals causing high peaks in the transfer function. These high peaks/ reflections can be defined by a parameter known as damping factor ζ [136]. Increase in factor ζ decreases reflections and thereby reliability of circuit improves.

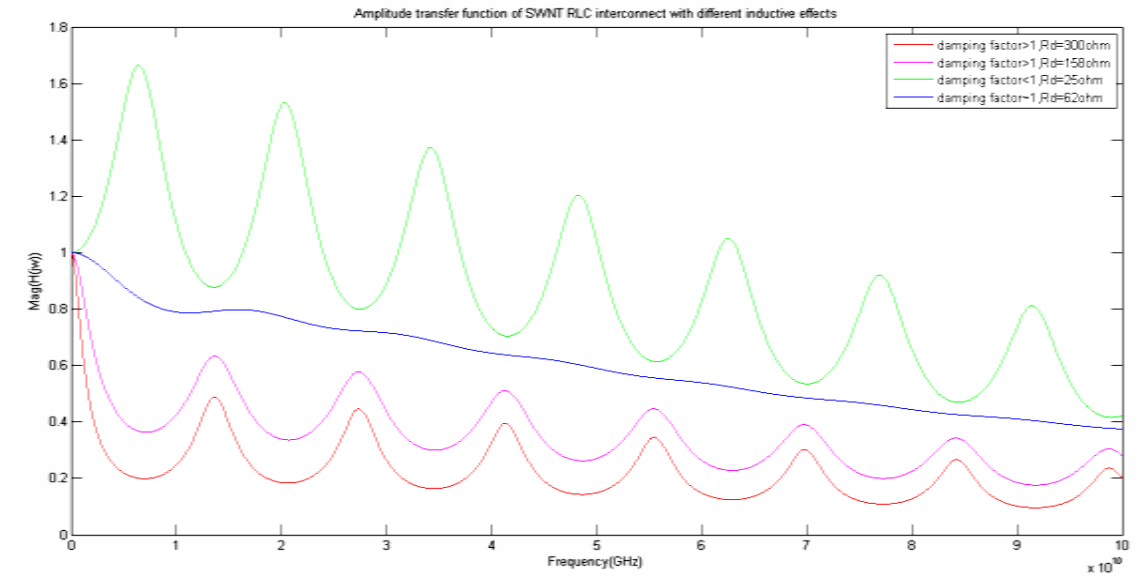
$$\zeta = \left(\frac{1}{2\sqrt{1+C}}\right)\left(\frac{R}{2Z_o} + \frac{R_d}{Z_o} + \frac{\tau_{C_l}}{\tau_f}\right) \tag{4.29}$$

where, $Z_o = \sqrt{L/C}$ is the characteristic impedance of a lossless transmission line. $\tau_{C_l} = C_l(R + R_d)$ is the time constant for charging the load capacitance and $\tau_f = \sqrt{LC}$ is the time of flight of the signals propagating across the transmission line. Time of flight is the time taken by the signal to propagate from source end to load end.

Thus, three different factors determine inductance effects in lines. First factor is the total line resistance to characteristic impedance of a lossless line. If this ratio increases, effect of inductance can be neglected. Therefore, the use of low resistance materials increases overshoots/undershoots. These materials degrade the reliability and integrity of the circuits. If the driver resistance increases relative to lossless characteristic impedance with reference to second factor in equation (4.29). It is observed that reflections are very low. Hence, inductance effect can be neglected. These effects are presented in **Fig. 4.11 (a)** and **(b)** for copper and SWCNT materials respectively.



(a) For Copper Interconnects



(b) For low resistance material SWCNT

Fig. 4.11 Different inductance effect on transfer function of interconnect by varying driver resistance R_d (at l=2000µm and **65nm** dimensions).

It is well known fact that with continuous shrinking of technology, driver resistance is getting scaled down. Hence damping factor $\zeta$is becoming prominent in the high speed circuits.If the ratio between the charging time constant of load capacitance and time of flight increases, inductive effect can be overlooked.

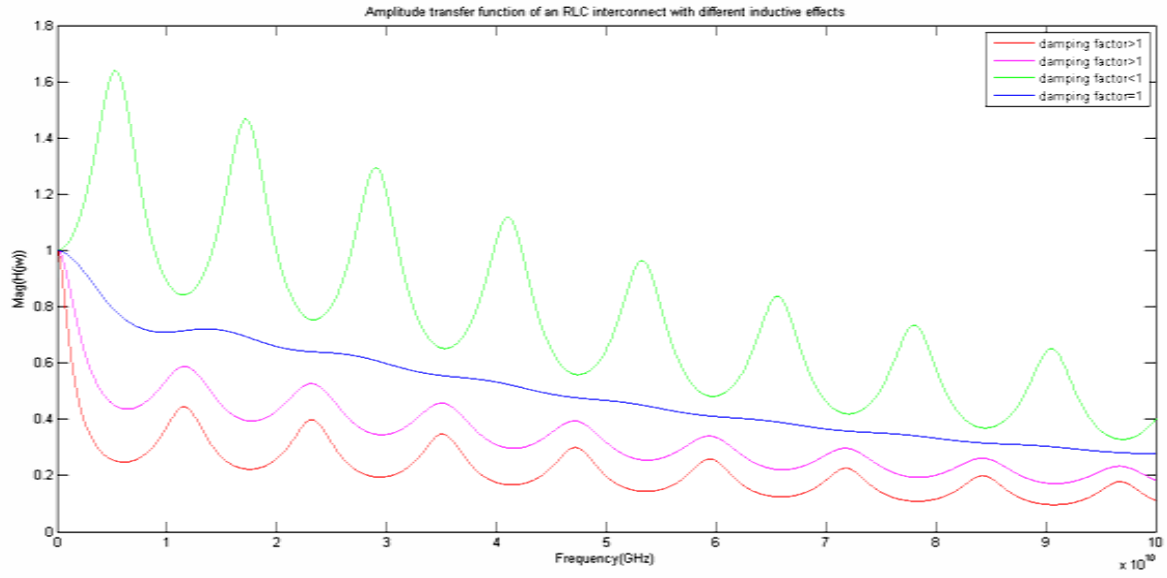


Fig. 4.12 (a) Different inductive effect on transfer function for **copper** interconnect by varying R_d (l=2000µm and at **180nm** dimensions)

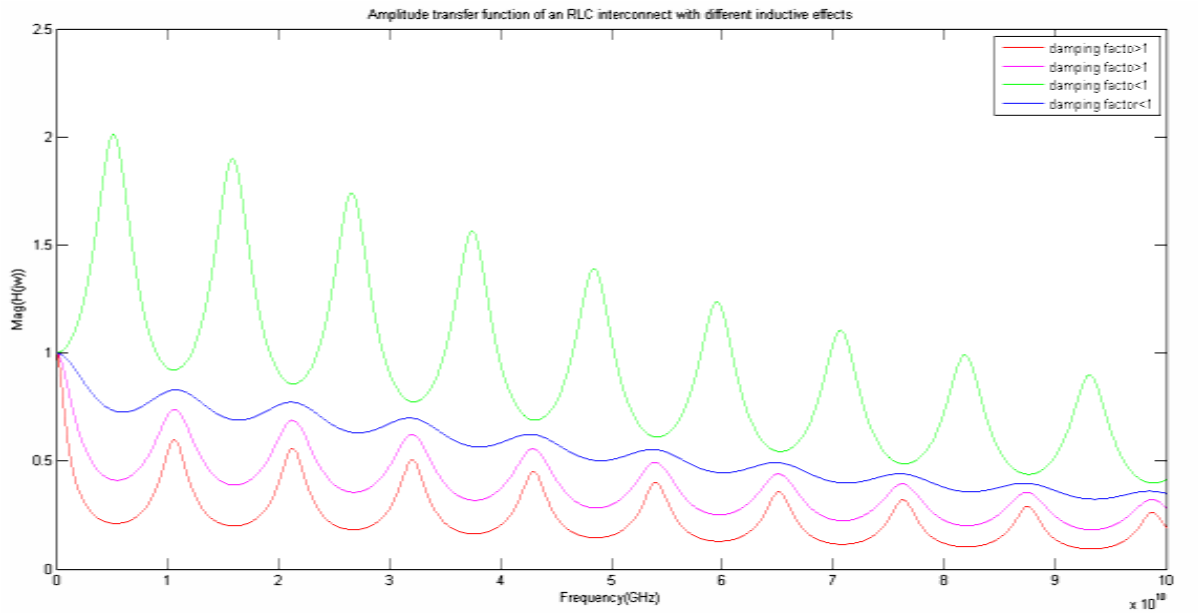


Fig. 4.12 (b) Different inductive effect on transfer function for **SWCNT** interconnect by varying R_d (l=2000µm and at **180nm** dimensions)

Comparing **Fig. 4.11(a)** and **(b),** it is found that for similar wire dimensions and load and driver conditions, inductive effect/ reflection is very high in case of SWNTs. The damping factor ζ increases with increase in load resistance. This increases R_d and the system approaches towards over-damped state. For the same value of R_d damping in Cu is large. In **Figs. 4.12 (a)** and **(b)** also present the inductive effects for copper and SWCNT interconnect at 180nm technology node. But inductive peaking is higher at 180nm node than 65nm node as observed from the **Fig. 4.11** and **Fig. 4.12.** This is due to the comparative smaller wire resistance at 180nm node than 65nm node.At smaller wire resistance damping is less than unity tends to higher inductive effects**.**

4.3.4 Fourier Series Analysis of Periodic Excitation Signal:

Input signal for the interconnect is taken as periodic ramp signal as shown in **Fig.4.13** and can be represented mathematically as in equation (4.30)

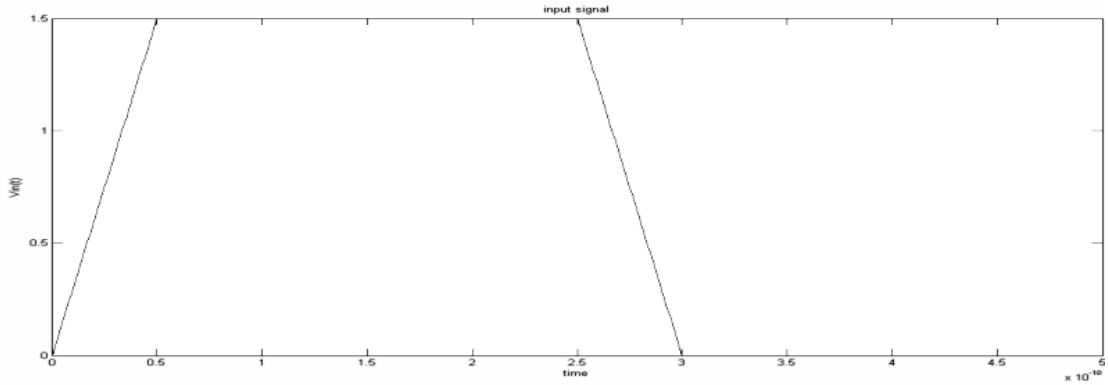


Fig. 4.13 Periodic ramp input signal

$$V_{input}\,(t) = \begin{cases} \left(\frac{t}{\tau}\right)V_{DD} & mT \le t \le mT + \tau \\ V_{DD} & mT + \tau \le t \le \left(m + \frac{1}{2}\right)T \\ \left(1 - \frac{t}{\tau} + \frac{T}{2\tau}\right)V_{DD} & (m + \frac{1}{2})T \le t \le \left(m + \frac{1}{2}\right)T + \tau \\ 0 & \left(m + \frac{1}{2}\right)T + \tau \le t \le (m+1)T \end{cases}$$

(4.30)

where, T is the period of $V_{input}\,(t)$, m is an integer and τ is the rise/fall time. Fourier series representation of the periodic ramp signal can be derived as follows. An input signal in terms of its harmonics can be represented in Fourier series as

$$V_{input}\,(t) = \; a_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega_0 t - \theta_n)$$

(4.31)

$$\theta_n = \; + \tan^{-1}\frac{b_n}{a_n}$$

(4.32)

$$A_n = \sqrt{a_n^2 + \; b_n^2}$$

(4.33)

where, $\omega_0 = 2\pi/T$ is the angular frequency and A_n and φ_n are the amplitude and phase of the nth-harmonic order.

$$a_0 = \frac{1}{T}\int_0^T V_{input}\,(t)dt$$

$$= \left[\int_0^{\tau}\frac{T}{\tau}V_{DD}\,dt + \int_{\tau}^{T/2} V_{DD}\,dt + \int_{T/2}^{T/2+\tau}\left(1 - \frac{t}{\tau} + \frac{t}{2\tau}\right)V_{DD}\,dt\right]$$

$$= \frac{V_{dd}}{T}\left[\left|\frac{t^2}{2\tau}\right|_0^{\tau} + \left|t\right|_{\tau}^{T/2} + \left|1 - \frac{t^2}{2\tau} + \frac{t}{2\tau}\ t\right|_{T/2}^{T/2+\tau}\right]$$

$$a_0 = \frac{V_{DD}}{T}\left[\frac{\tau}{2} + T - \frac{\tau}{2} - \frac{T}{2}\right]$$

$$\therefore\ a_0 = \frac{V_{DD}}{2}$$

(4.34)

$$a_n = \frac{2V_{DD}}{T}\left[\int_0^{\tau}\frac{1}{\tau}(t\cos n\omega_0 t)dt + \int_{\tau}^{T/2}\cos n\omega_0 t\ dt + \int_{T/2}^{T/2+\tau}\cos n\omega_0 t\ dt - \frac{1}{\tau}\int_{T/2}^{T/2+\tau}(t\cos nw_0 t)dt + \frac{T}{2\tau}\int_{T/2}^{T/2+\tau}\cos nw_0 t\ dt\right]$$

$$= \frac{2V_{DD}}{T}\left[\frac{1}{\tau}\left[\left|\frac{t\sin n\omega_0 t}{n\omega_0}\right|_0^{\tau} - \int_0^{\tau}\frac{\sin n\omega_0 t}{n\omega_0}\right] + \left|\frac{\sin n\omega_0 t}{n\omega_0}\right|_{\tau}^{T/2} + \left|\frac{\sin n\omega_0 t}{n\omega_0}\right|_{T/2}^{T/2+\tau} - \left[\frac{1}{\tau}\left|\frac{t\sin n\omega_0 t}{n\omega_0}\right|_{T/2}^{T/2+\tau} - \int_{T/2}^{T/2+\tau}\frac{\sin n\omega_0 t\ dt}{n\omega_0}\right] + \frac{T}{2\tau}\left|\frac{\sin n\omega_0 t}{n\omega_0}\right|_{T/2}^{T/2+\tau}\right]$$

$$= \frac{4V_{DD}}{T\,n^2\omega_0^2\,\tau}[\cos nw_0\tau - 1\,]$$

$$\therefore\ a_n = \frac{T}{\tau}\frac{V_{DD}}{n^2\pi^2\tau}[\cos nw_0\tau - 1\,] \qquad for, n \neq even$$

(4.35)

$$b_n = \frac{2}{T}\int_0^{\tau} V_{input}\,(t)\sin nw_0 t\ dt$$

$$= \frac{2}{T}V_{dd}\left[\frac{1}{\tau}\int_0^{\tau}(t\sin nw_0t)\,dt + \int_0^{T/2}\sin nw_0t\,dt + \int_{T/2}^{T/2+\tau}\sin nw_0t\,dt - \frac{1}{\tau}\int_{T/2}^{T/2+\tau}(\mathrm{t}\sin nw_0t)\,dt + \frac{T}{2\tau}\int_{T/2}^{T/2+\tau}\sin nw_0t\,dt\right]$$

$$= \frac{2}{T}V_{DD}\left[\frac{1}{\tau}\left[\left|\frac{-t\cos nw_0t}{n\omega_0}\right|_0^{\tau} - \int_0^{\tau}\frac{-\cos nw_0t}{n\omega_0}\right] + \left|\frac{-\cos nw_0t}{n\omega_0}\right|_{\tau}^{T/2} + \left|\frac{-\cos nw_0t}{n\omega_0}\right|_{T/2}^{T/2+\tau} - \frac{1}{\tau}\left[\left|\frac{-t\cos nw_0t}{n\omega_0}\right|_{T/2}^{T/2+\tau} + \int_{T/2}^{T/2+\tau}\frac{\cos nw_0t}{n\omega_0}\right] + \frac{T}{2\tau}\left|\frac{-\cos nw_0t}{n\omega_0}\right|_{T/2}^{T/2+\tau}\right]$$

$$\therefore\ b_n = \frac{TV_{DD}}{\tau n^2\pi^2}\sin\omega_0\tau \qquad for, n \neq even$$

(4.36)

Now, putting equation (4.35), (4.36) in equation (4.33)

$$A_n = \sqrt{a_n^2 + b_n^2}$$

$$= \frac{T\,V_{DD}}{\tau\,n^2\pi^2}\sqrt{(\cos n\omega_0\tau - 1)^2 + (\sin n\omega_0\tau)^2}$$

$$= \frac{TV_{DD}}{\tau\,n^2\pi^2}\sqrt{(1 + 1 - 2\cos n\omega_0\tau)}$$

$$= \frac{TV_{DD}}{\tau\,n^2\pi^2}\sin\frac{n\omega_0\tau}{2}$$

$$\therefore\ A_n = \frac{2TV_{DD}}{\tau\,n^2\pi^2}|\sin\varphi|$$

(4.37)

Now, putting equation (4.35), (4.37) in equation (4.32)

$$\theta = \tan^{-1}\left(\frac{\sin n\omega_0\tau}{\cos n\omega_0\tau - 1}\right)$$

$$= \tan^{-1}\left(-\cot\frac{n\omega_0\tau}{2}\right)$$

$$= \tan^{-1}(\tan^{-1}(90 + \theta))$$

$$\therefore\ \theta = 90 + \tfrac{n\omega_0\tau}{2} \quad (4.38)$$

Now, putting equation (4.34), (4.38) in equation (4.31)

$$V_{input}(t) = \frac{V_{DD}}{2} + \sum_{n=1,3\ldots odd} A_n\cos\left(n\omega_0t - 90 - \frac{n\omega_0\tau}{2}\right)$$

$$= \frac{V_{DD}}{2} + \sum_{n=1,3\ldots odd} A_n \sin\left(n\omega_0 t - \frac{n\omega_0\tau}{2}\right)$$

$$\therefore\ V_{input}\ (t) = \frac{V_{DD}}{2} + \sum_{n=1,3\ldots odd} A_n \sin(n\omega_0 t + \varphi_n) \tag{4.39}$$

$$\varphi_n = -\frac{n\omega_0\tau}{2}$$

$$\therefore\ A_n = \frac{2TV_{dd}}{\tau\, n^2\pi^2}\,|\sin\varphi|$$

From equation (4.39), $V_{input}\ (t)$ has a dc component and odd-harmonics. It can be seen that A_n decreases quadratically with number of harmonics, therefore the first few harmonics would be enough to define $V_{input}\ (t)$.

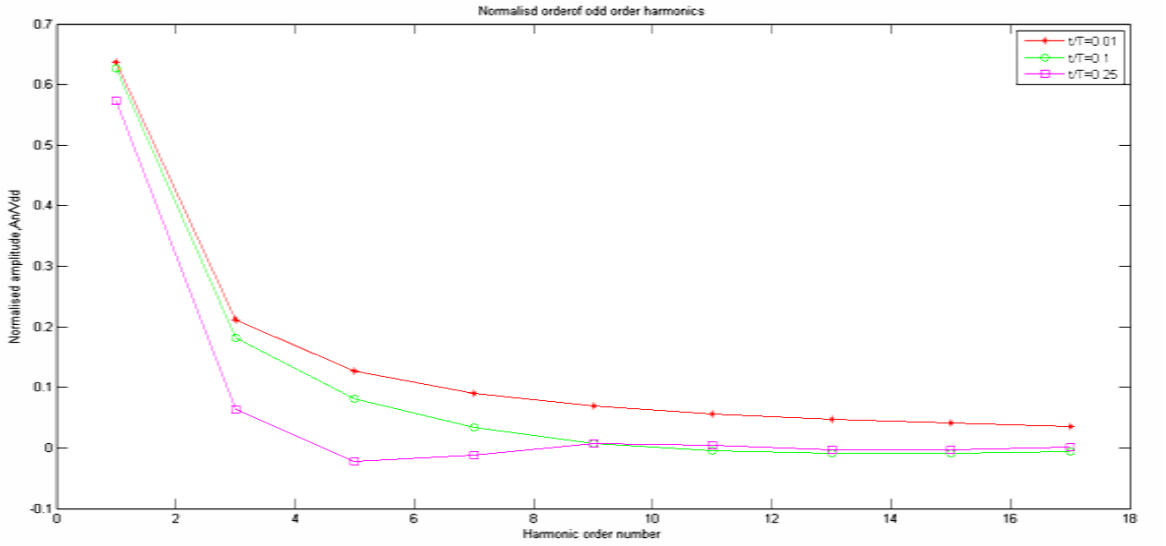


Fig. 4.14 Harmonic order versus normalized amplitude (A_n/V_{DD}) with different τ/T

From **Fig. 4.14**, it is observed that as the number of harmonics increases, the normalized amplitude decreases, but the rate of decreasing slows down with decrease in τ/T ratio. The same can be observed from **Fig. 4.14** and amplitude function.

4.3.5 Time Domain Response of The Interconnect:

The circuits shown in **Fig. 4.7** and **Fig. 4.9** are linear and time invariant. Superposition principle can be applied to obtain the time domain output since input signal is represented by summation of harmonics and a linear system.

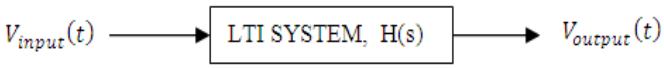


Fig. 4.15 Block diagram of LTI system.

The exact transfer function of Cu and SWNT can be represented at each angular frequency as

$$H(s)|_{S=j\omega} = A(\omega)e^{j\beta\omega} \tag{4.40}$$

From equation (4.21) and (4.25), H(0)=1. Therefore, the output is

$$\therefore\ V_{output}\ (t) = \frac{V_{dd}}{2} + \sum_{n=1,3\ldots odd} A_n{}'\sin(n\omega_0 t + \varphi_n{}') \tag{4.41}$$

$$A_n{}' = A_n A(n\omega_0)$$

$\varphi_n{}' = \varphi_n + \beta(n\omega_o)$

Few lower order harmonics would be sufficient to define the output. In this work 3rd and 5th order harmonic of the output is considered and are known as OUT3 (Fb3) and OUT5 (Fb5) respectively.

4.3.6 Formulation of 50% delay:

In this work, 50% delay is assumed to be less than $\frac{T}{2} - \tau/2$. Closed from solution of the output is obtainable while considering 3rd order or 5th order harmonics. For three harmonics, output is given as

$$V_{output}\ (t) = \frac{V_{dd}}{2} + A_1'\sin(\omega_0 t + \varphi_1') + A_3'\sin(3\omega_0 t + \varphi_3') \tag{4.42}$$

To find the 50% delay, $V_{output}\ (t) = V_{dd}/2$ is set. Using multiple-angle formulas [137], a third-order trigonometric expression can be obtained as followed

$$A_1'\sin(\omega_0 t + \varphi_1') + A_3'\sin(3\omega_0 t + \varphi_3') = 0$$

Putting $\omega_o t = \theta$

$$=> A_1'[\cos\varphi_1'\sin\theta + \sin\varphi_1'\cos\theta] + A_3'[\cos\varphi_3'\sin 3\theta + \sin\varphi_3'\cos 3\theta] = 0$$

$$=> A_1'[\cos\varphi_1'\sin\theta(\sin^2\theta + \cos^2\theta) + \sin\varphi_1'\cos\theta(\sin^2\theta + \cos^2\theta)]$$
$$+ A_3'[\cos\varphi_3'(3\sin\theta\cos^2\theta - \sin^3\theta) + \sin\varphi_3'(\cos^3\theta - 3\sin^2\theta\cos\theta)] = 0$$

$$=> (A_1'\cos\varphi_1' - A_3'\cos\varphi_3')\sin^3\theta + (A_1'\sin\varphi_1' - 3A_3'\sin\varphi_3')\sin^2\theta\cos\theta$$
$$+ (A_1'\sin\varphi_1' + 3A_3'\cos\varphi_3')\sin\theta\cos\theta + (A_1'\sin\varphi_1' + A_3'\sin\varphi_3')\cos^3\theta = 0$$

$$=> a_3\tan^3\theta + a_2\tan^2\theta + a_1\tan\theta + a_0 = 0$$

$$a_3 z^2 + a_2 z^2 + a_1 z + a_0 = 0 \tag{4.43}$$

Where $z = \tan(\omega_o t)$

$$\text{At,} \quad t_{t=T/2} = \tan^{-1} z_o \,/\omega_o$$

$a_3 = (A_1^{'}\cos\varphi_1^{'} - A_3^{'}\cos\varphi_3^{'})$

$a_2 = (A_1^{'}\sin\varphi_1^{'} - 3A_3^{'}\sin\varphi_3^{'})$

$a_1 = (A_1^{'}\sin\varphi_1^{'} + 3A_3^{'}\cos\varphi_3^{'})$

$a_0 = (A_1^{'}\sin\varphi_1^{'} + A_3^{'}\sin\varphi_3^{'})$

A third-order expression has either one or three real roots. If equation (4.43) has only one real root z_o, the output waveform crosses only once from low-to high during the first half of a period, therefore, the undershoot is greater than $V_{dd}/2$. From this real root, the 50% delay can be expressed as

$$t_{delay} = \frac{tan^{-1} z_o}{\omega_0} - \frac{\tau}{2} \tag{4.44}$$

The value of $tan^{-1} z_o$ is in the range of [0,π]. If equation (4.43) has three real roots, the output waveform crosses three times during the first half of the period. Hence, the undershoot is less than $V_{DD}/2$. In this case, the output waveform is not shaped like a square wave and can no longer represent logic values. Similar process can be followed for OUT5 to calculate its delay. OUT5 is given as:

$$V_{output}\,(t) = V_{DD}/2 + A_1^{'}\sin(\omega_0 t + \varphi_1^{'}) + A_3^{'}\sin(3\omega_0 t + \varphi_3^{'}) + A_5^{'}\sin(3\omega_0 t + \varphi_5^{'}) \tag{4.45}$$

4.3.7 Formulation of overshoot/undershoot:

To determine the extremum i.e. minimum or maximum value, derivative of equation (4.42) is taken as described below

$$\frac{dV_{out}}{dt} \approx A_1^{'}\omega_0\cos(\omega_0 t + \varphi_1^{'}) + 3A_3^{'}\omega_0\cos(3\omega_0 t + \varphi_3^{'}) \tag{4.46}$$

Putting equation (4.46) equal to 0 and applying multiple angle formulas, a third-order trigonometric expression can be obtained as

$$A_1^{'}\omega_0\cos(\omega_0 t + \varphi_1^{'}) + 3A_3^{'}\omega_0\cos(3\omega_0 t + \varphi_3^{'}) = 0$$

Putting $\omega_o t = \theta$

$$
\begin{aligned}
=> & A_1^{'}\omega_0[-\sin\varphi_1^{'}\sin\theta\,(\sin^2\theta+\cos^2\theta)+\cos\varphi_1^{'}\cos\theta\,(\sin^2\theta+\cos^2\theta)] \\
& + 3A_3^{'}\omega_0[-\sin\varphi_3^{'}(-\sin^3\theta+3\sin\theta\cos^2\theta) \\
& + \cos\varphi_3^{'}(\cos^3\theta-3\sin^2\theta\cos\theta)] = 0 \\
=> & (-A_1^{'}\omega_0\sin\varphi_1^{'}+3A_3^{'}\omega_0\sin\varphi_3^{'})\sin^3\theta+(A_1^{'}\omega_0\cos\varphi_1^{'}-9A_3^{'}\omega_0\cos\varphi_1^{'})\sin^2\theta\cos\theta \\
& + (-A_1^{'}\omega_0\sin\varphi_1^{'}-9\,A_3^{'}\omega_0\sin\varphi_3^{'})\sin\theta\cos^2\theta \\
& + (A_1^{'}\omega_0\cos\varphi_1^{'}+3A_3^{'}\omega_0\cos\varphi_3^{'})\cos^3\theta = 0 \\
=> & b_3\sin^3\theta+b_2\sin^2\theta\cos\theta+b_1\sin\theta\cos^2\theta+b_0\cos^3\theta = 0 \\
=> & b_3\frac{\sin^3\theta}{\cos^3\theta}+b_2\frac{\sin^2\theta}{\cos^2\theta}+b_1\tan\theta+b_0 = 0 \\
=> & b_3tan^3\theta+b_2tan^2\theta+b_1\,tan\,\theta+b_0 = 0 \\
& b_3w^3+b_2w^2+b_1w+b_o = 0
\end{aligned}
$$

(4.47)

where, $w = \tan(\omega_o t)$

$b_3 = (-A_1^{'}\omega_0\sin\varphi_1^{'}+3A_3^{'}\omega_0\sin\varphi_3^{'})$

$b_2 = (A_1^{'}\omega_0\cos\varphi_1^{'}-9A_3^{'}\omega_0\cos\varphi_1^{'})$

$b_1 = (-A_1^{'}\omega_0\sin\varphi_1^{'}-9\,A_3^{'}\omega_0\sin\varphi_3^{'})$

$b_0 = (A_1^{'}\omega_0\cos\varphi_1^{'}+3A_3^{'}\omega_0\cos\varphi_3^{'})$

The real roots of equation (4.47) give the time of extremum. The time obtained can be less thanτ_f. This behavior occurs because the voltage response described by equation (4.41) is a steady-state response. The extremum which occurs before τ_f is the response to the previous period of the input signal. For the response to the current period, the time when the extremum occurs shall be:

$$
t_{ex} = \begin{cases} \arctan w_0 & \arctan w_0 > \tau_f \\ \arctan w_0 + \dfrac{\tau}{2} & \arctan w_0 \le \tau_f \end{cases}
$$

(4.48)

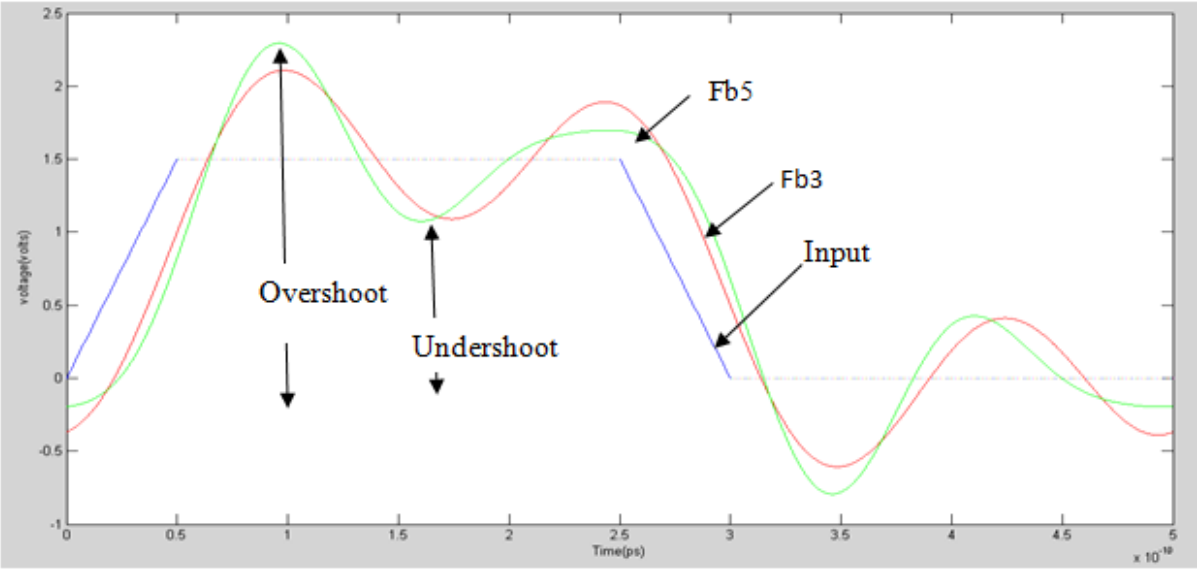
where, w_0 is a real root of equation (4.47). Inserting t_{ex} into equation (4.42), the corresponding extremum is given as:

$$
V_{extremum} = \frac{V_{dd}}{2}+A_1^{'}\sin(\omega_0 t_{ex}+\varphi_1^{'})+A_3^{'}\sin(3\omega_0 t_{ex}+\varphi_3^{'})
$$

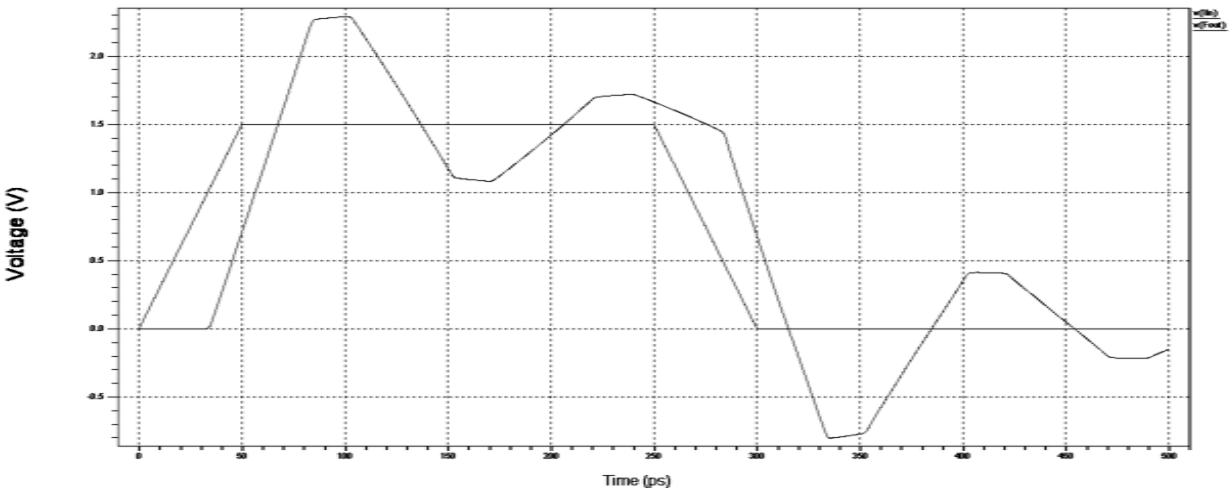
(4.49)

4.3.8 Comparison of time domain response of Out3 (Fb3) and Out5 (Fb5) with SPICE

From **Fig. 4.15 (a)** and (**b)** it is clearly visible that OUT3 (Fb3) and OUT5 (Fb5) follow the SPICE simulated result. But OUT5 shows more accuracy as compared to OUT3. Hence, if the number of harmonics is increased further, accuracy will also increase.



(a) MATLAB Simulated (Out3) Fb3 and (Out5) Fb5 Harmonics.



(b) SPICE Simulated OUT3 (Fb3) and OUT5 (Fb5) With Input Signal

Fig. 4.15(a) Output Graph from OUT3 (Fb3) and OUT5 (Fb5) Model of Cu Interconnect (b) SPICE output graph of Cu interconnect.

4.4 SIMULATIVE ANALYSIS AND RESULTS

4.4.1 SPICE Setup

For the simulation purpose, a periodic pulse signal is taken with period T= 500ps. The rise and fall time τ is set to 50 ps. The values of the interconnect dimensions at various technology is referred from the PTM website and is stated below in **Table 4.3**. Different K values are used for different technologies as mentioned in the website and following the ITRS trends.

Table 4.3 Dimensions of interconnect at various technology nodes [108]

Technology (nm)	Width(w) (µm)	Space(s) (µm)	Thickness(t) (µm)	Height(h) (µm)	K_{ILD}
180	0.8	0.8	1.25	.65	3.5
130	0.6	0.6	1.20	.45	3.2
90	0.5	0.5	1.20	.3	2.8
65	0.4	0.4	1.20	0.2	2.4

4.4.2 Copper RLC Interconnect:

The RLC interconnect of length l is divided into 200 L-type basic lumped segments. The black box view of the interconnect is shown in **Fig 4.16** and each black box view has basic L-type lumped segment as its entity shown in **Fig 4.17**.

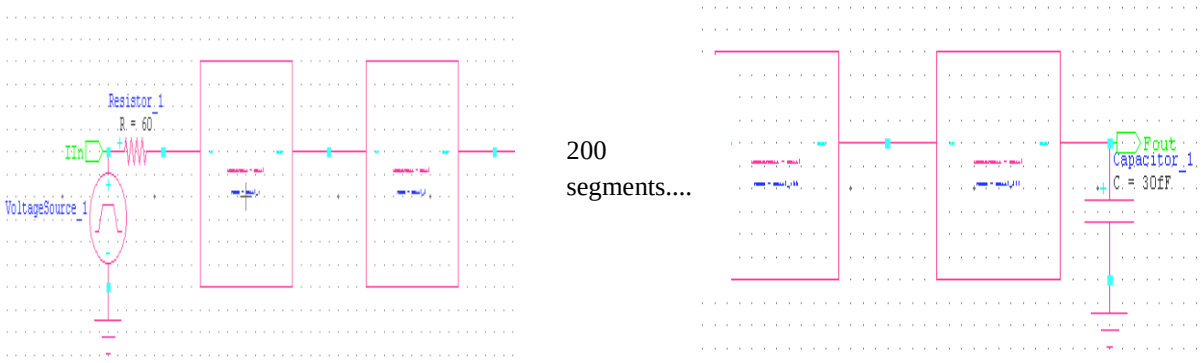


Fig. 4.16 Black box view of the RLC interconnect.

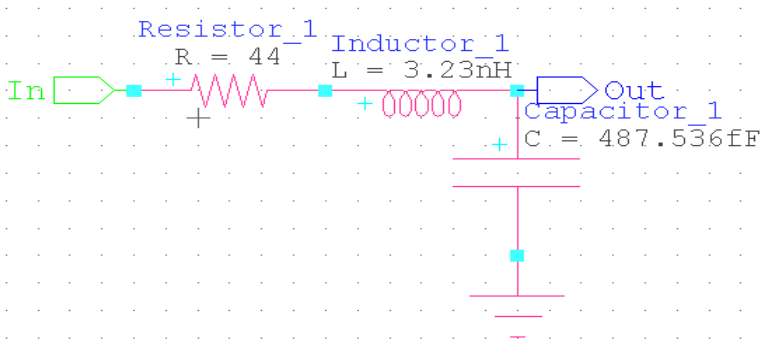


Fig. 4.17 Basic L-type lumped entity.

4.4.3 SWCNT Bundle RLC interconnect:

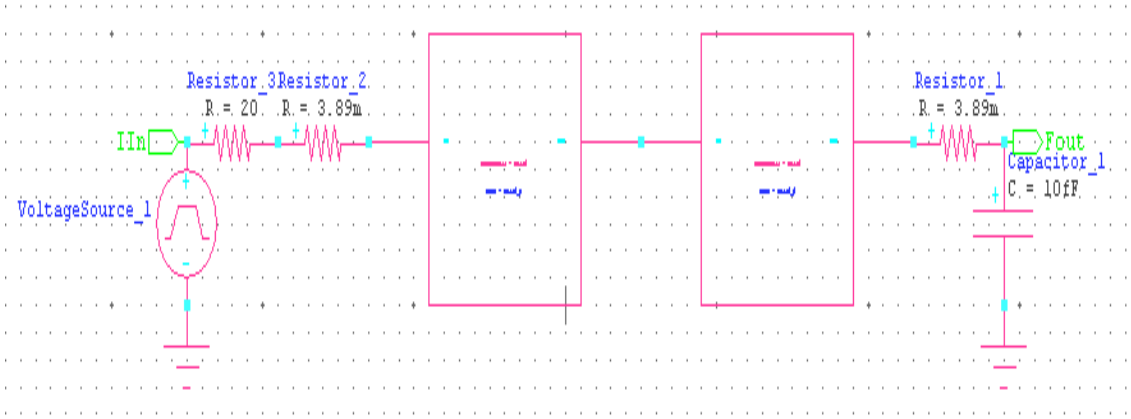
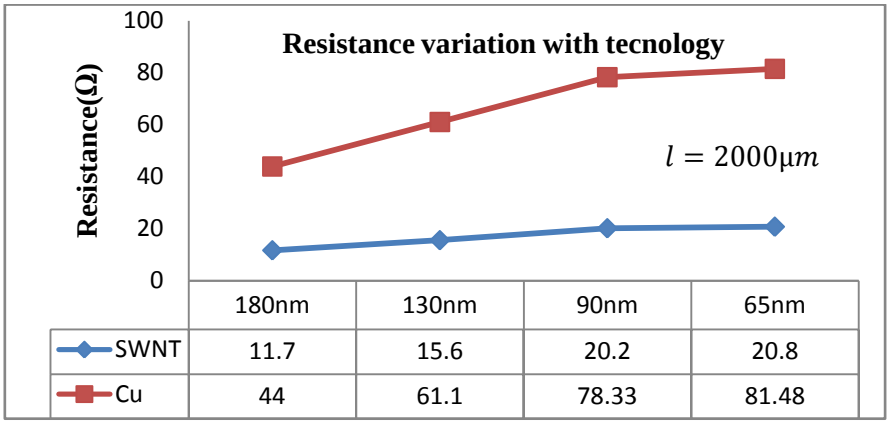


Fig. 4.18 Black box view of SWNT bundle interconnection & each black box consists of 100 segments of basic L-type lumped entity.

SWNT bundle interconnect has two additional series resistance at input and output in **Fig 4.18**. These resistances signify the fundamental resistance of the SWCNT bundle interconnects. Dimensions for SWCNT bundle interconnects is taken same as that of copper interconnect.

Diameter d of a SWCNT is taken as $1\mu m$ and x, the spacing between two CNTs is taken equal to diameter considering densely packing of CNTs. MFP (Mean free path) is set to $1\mu m$. In this dissertation, the length of interconnect is always taken larger than the MFP such that scattering resistance has its significance on the performance parameters. Also the contact of SWNTs with metal layers is also considered to be ideal.

4.4.4 Resistance Variation of Copper And SWNT Bundle Interconnect At Different Technology Nodes



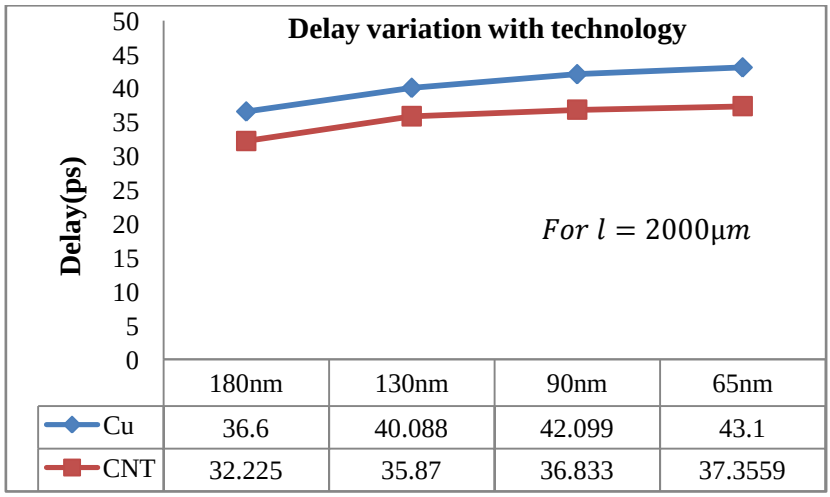
	180nm	130nm	90nm	65nm
SWNT	11.7	15.6	20.2	20.8
Cu	44	61.1	78.33	81.48

Fig. 4.19 Copper and SWNT's resistance variation with technology

From **Fig. 4.19** it is observed that resistance of SWCNT bundle is much less than copper and the rate of increase in resistance of copper is much larger than that of SWNT bundle. This is due to fact that in case of copper, charge carriers start to scatter after few nano-meters (MFP of copper is 40-50nm where it shows ballistic conduction) resulting in increase of its resistance rapidly. But in case of SWNT bundle, charge carriers do not scatter over large distance as MPF is very large for CNTs which is shown to be proportional to $1000d$[10].It is essential for global interconnects to have lower delays for high speed integration.

4.4.5 Performance Comparison of Copper And SWNT Bundle Interconnect For Delay

Delay Variation with Technology

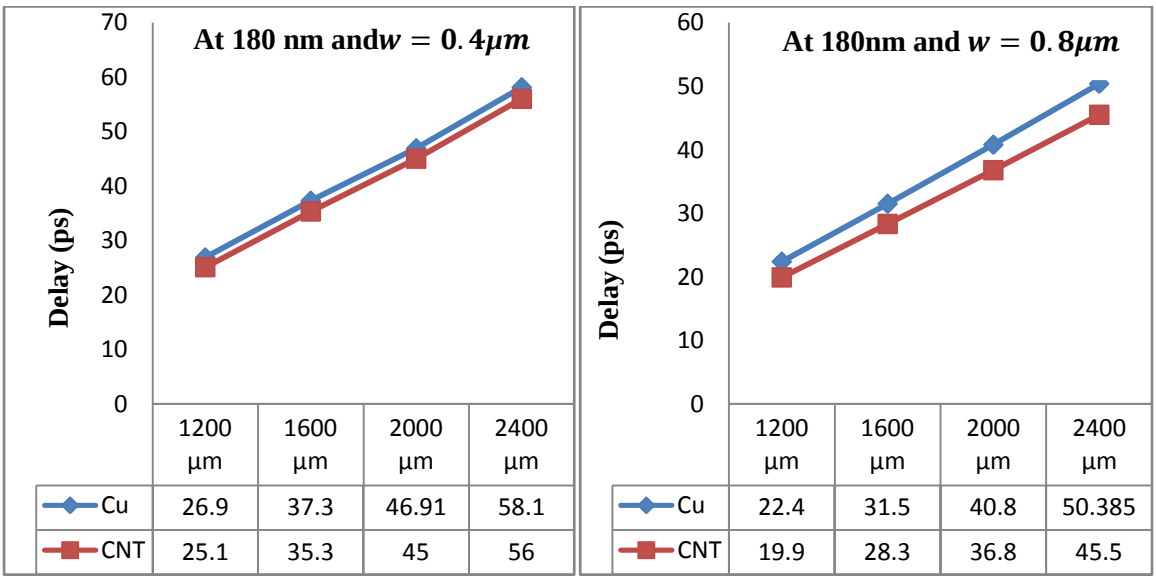


	180nm	130nm	90nm	65nm
Cu	36.6	40.088	42.099	43.1
CNT	32.225	35.87	36.833	37.3559

Fig. 4.20 Delay comparison of copper with SWNT bundle at $l = 2000\mu m$

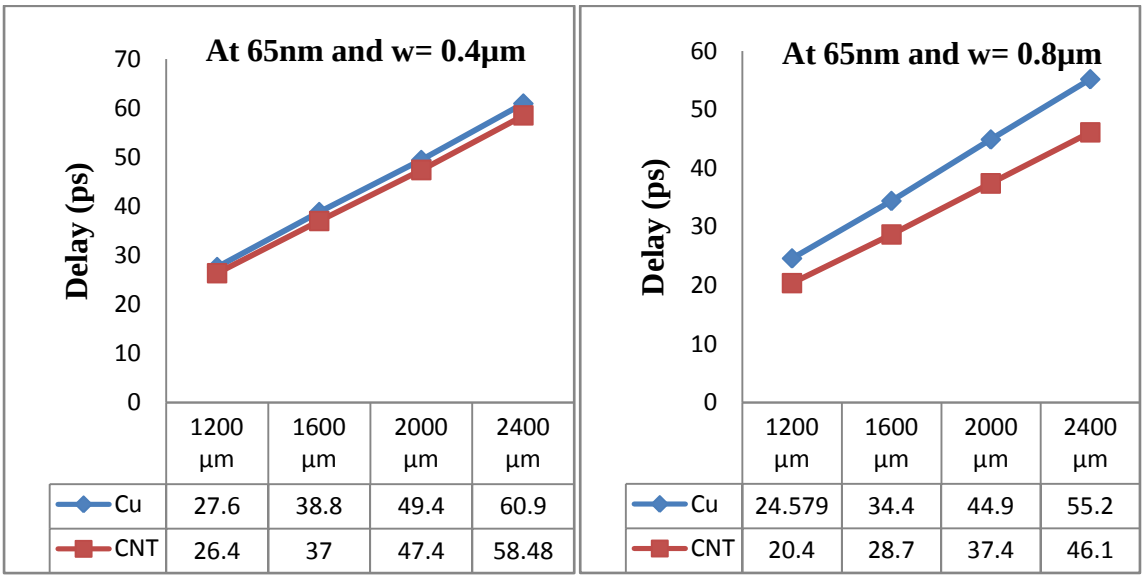
For delay simulation driver resistance R_d is 30Ω and load capacitance C_l is 50fF. From **Fig.4.20,** it is observed that SWNT delay is lower than the copper delay. This is due to lower resistance of SWNT bundles at longer lengths due to ballistic conduction. Hence, due to the above facts, SWNT bundle proves to be a prospective candidate for high speed VLSI designs for global wires at nano and sub-micron meter regimes.

4.4.6 Delay Variation with Length (l) and Width (w)



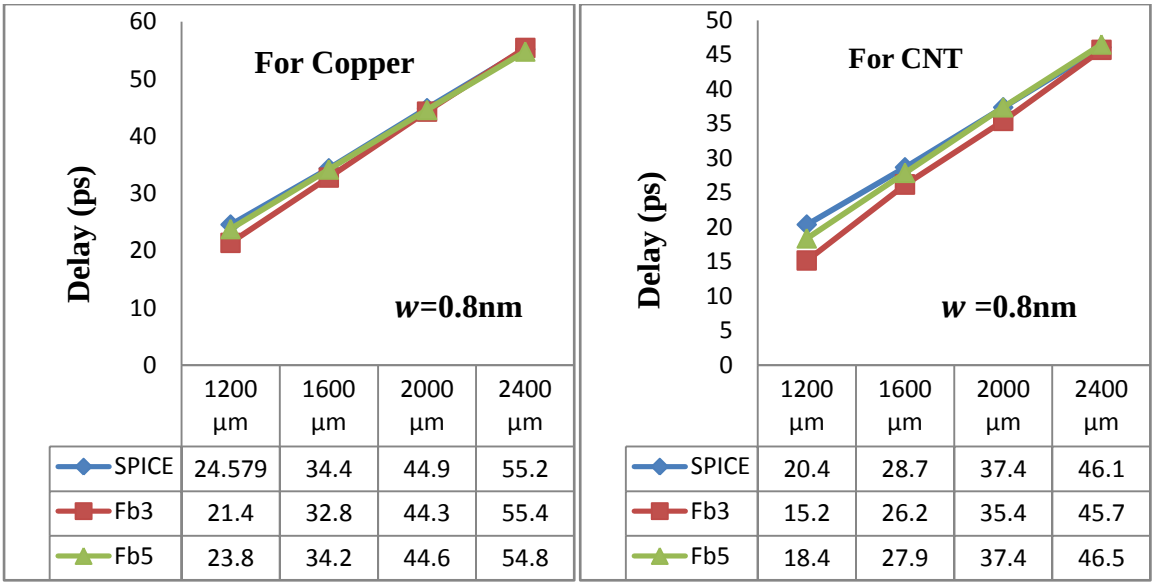
(a) **(b)**

Fig. 4.21 Comparison of CNT with copper at **180nm** (a) $w = 0.4\mu m$ (b) $w = 0.8\mu m$



(a) **(b)**

Fig. 4.22 Comparison of CNT with copper at **65nm** (a) $w = 0.4\mu m$ (b) $w = 0.8\mu m$.



(a) **(b)**

Fig.4.23 Comparison of SPICE Delay Results with OUT3 (Fb3) and OUT5 (Fb5) Modeling at 65 nm technology for $w = 0.8nm$ (a) Copper (b) SWNT bundle.

From **Fig. 4.21 (a) & (b), Fig. 4.22 (a) & (b)** and **Fig. 4.23(a)** & **(b)** it is clearly visible that with increase in length, delay of both the materials increases because scattering resistance of SWNT bundle and resistance of copper is directly proportional to its length.

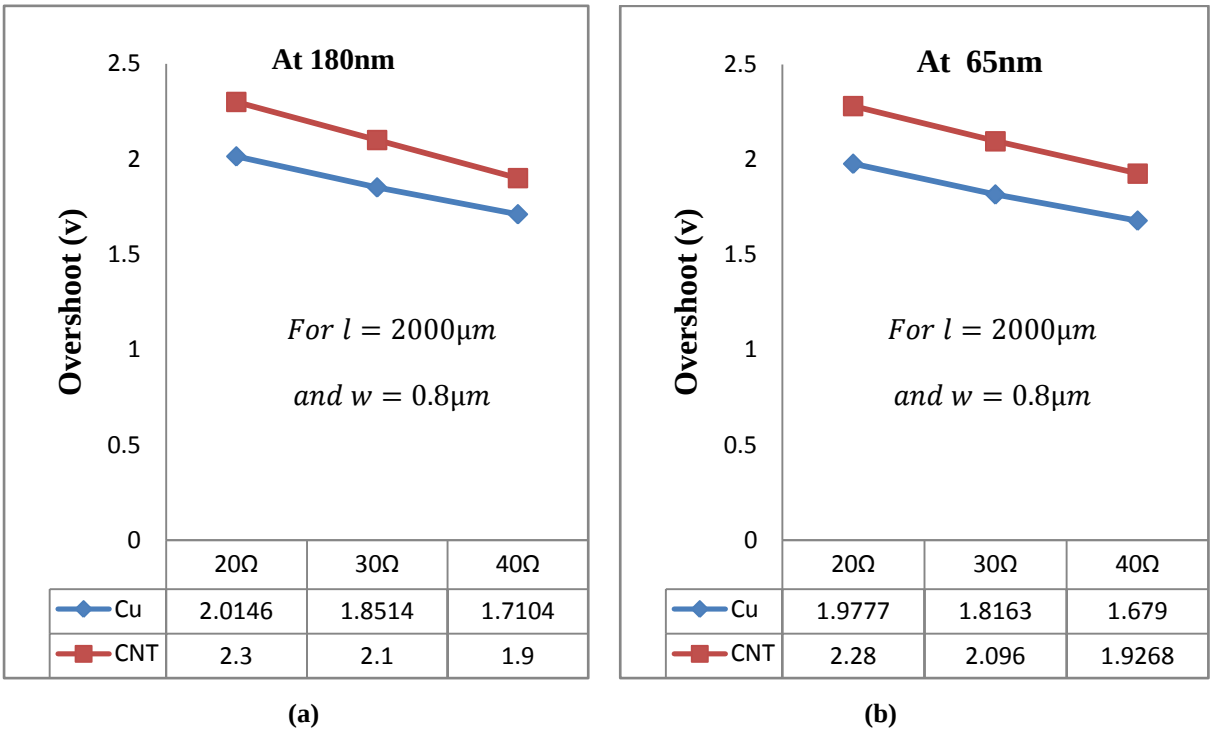
But the difference in delay between copper and SWNT bundle is not vast for wider widths as compared to narrow widths as observed from **Fig. 4.21** and **Fig. 4.22**due to resistance of both the material is comparable at wider widths. At narrow widths, SWNT's rate of increase in delay is very low as compared to that of Copper because copper resistivity increases rapidly at narrow widths due to surface scattering and grain boundary effects. These effects are absent in CNTs as observed from **Fig. 4.23 (a)** and **(b).**

As resistance decreases at wider widths the delays are as large as compared to narrow widths dimensions due to increase in capacitance at greater pace. The increase in capacitance is because of decrease in spacing between metal layers known as pitch reduction.For longer lengths and narrow widths (a global wire characteristic), SWNTs give desirable performance.

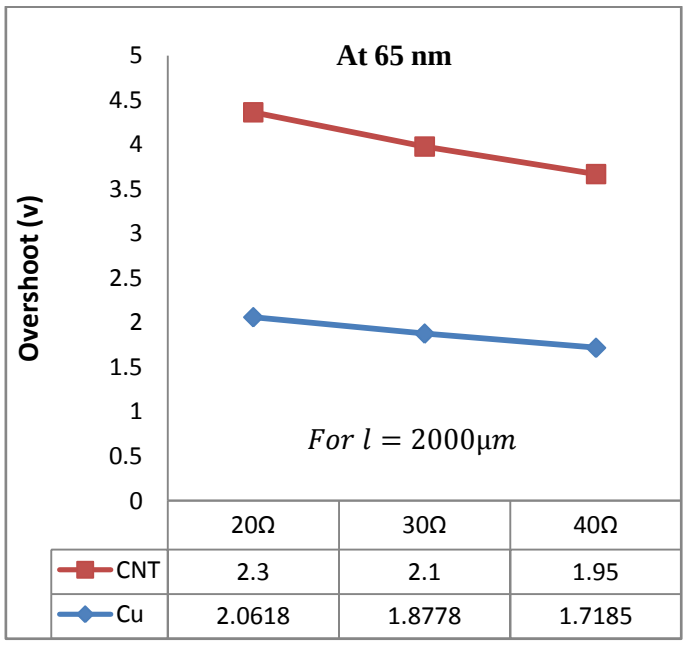
As technology scaled down from 180nm to 65nm as shown in **Fig 4.21** and **Fig. 4.22**, delay increases for both the materials but it is still very low in SWNTs as compared to copper. At lower technology nodes, densely packed SWNTs give better results and performance. **Fig**

4.23 (a) and **Fig. 4.23 (b)** compares SPICE results with the OUT3 (Fb3)and OUT5 (Fb5) results at 65nm technology. OUT3 (Fb3) and OUT5 (Fb5) proves to be highly precise &accurate.

4.4.7 Overshoot Variation with Driver Resistance



(a) **(b)**



(c)

Fig. 4.24 Comparison of SPICE overshoot results of copper and SWNT bundles (a)at 180nm for $w = 0.8\mu m$ (b) at 65nmfor $w = 0.8$ (c) at 65nm for $w = 1.4\mu m$

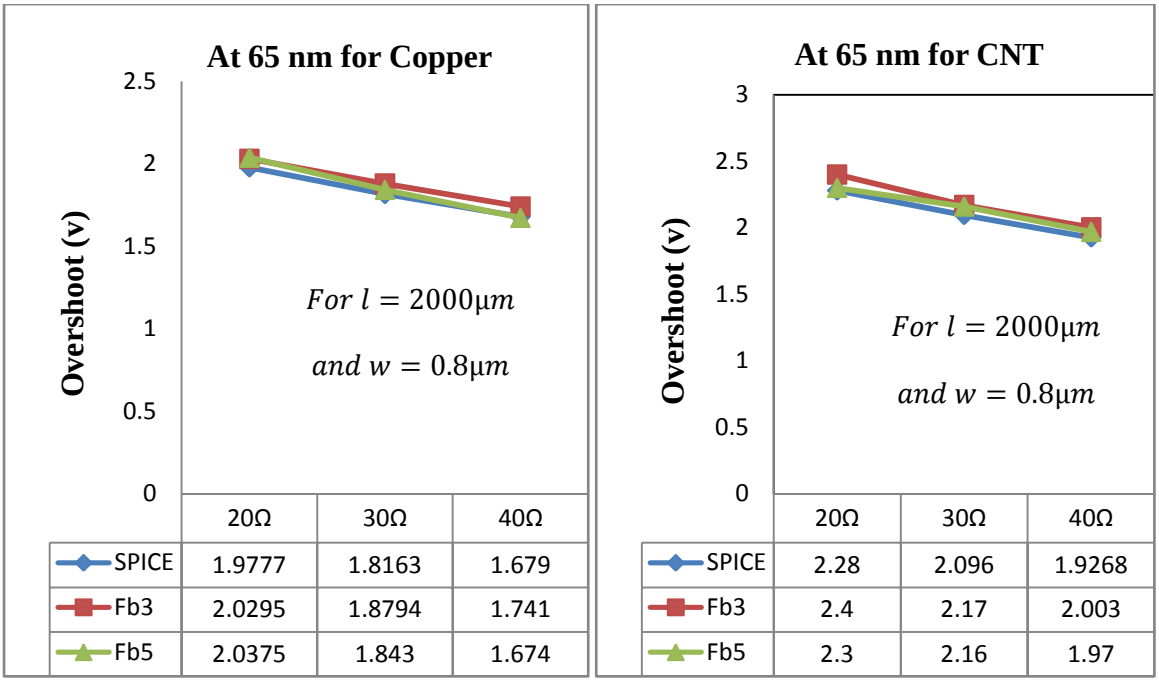
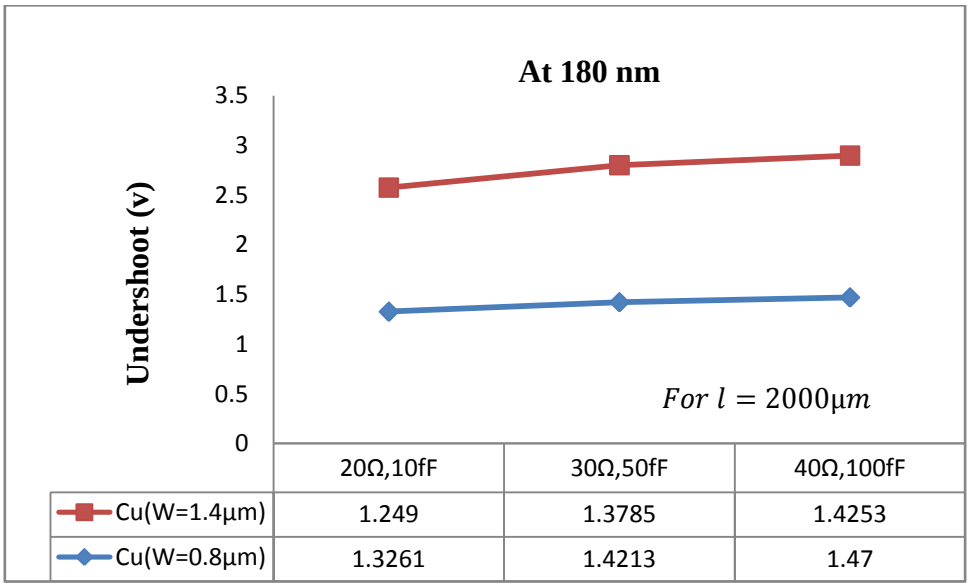


Fig. 4.25 Comparison of SPICE overshoot results with OUT3 (Fb3) and OUT 5 (Fb5) at 65nmfor $w = 0.8\mu m$ (a) copper (b) SWNT.

Fig 4.24 (a), (b) and (c) shows the variation of overshoot with driver resistance. It is observed that as the driver resistance is increased, the inductive effect (ζ) diminishes because of prominance of resistance in the impedance, Z=R+j ω L. Hence, if the interconnect resistance increases, inductive effect can be neglected. This would further simulatneouly degrade the interconnect's speed.

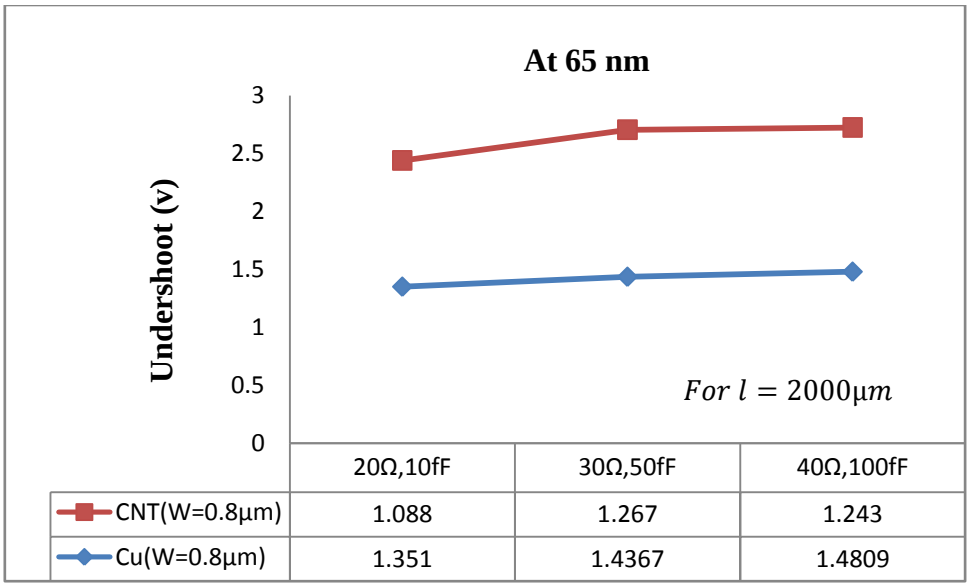
It can be seen from the above graphs **Fig. 4.24(a), (b) and (c)** that the overshoot is large in SWNT bundles as compared to copper. This is because of lower resistance of SWNT bundles. Also moving from higer technology nodes to lower nodes, overshoots decreases as seen from Fig. **4.25 (a), (b)** due to increases in resistance at lower nodes.For wider widths, overshoot increases as observed from **Fig 4.24 (b) and (c)** due to resistance decrement.**Fig.4.25 (a) and (b),** demonstrate that results of OUT3 (Fb3) and OUT (Fb5) matches with SPICE results with high accuracy.

4.4.8 Undershoot Variation with Driver Resistance



	20Ω,10fF	30Ω,50fF	40Ω,100fF
Cu(W=1.4μm)	1.249	1.3785	1.4253
Cu(W=0.8μm)	1.3261	1.4213	1.47

(a)

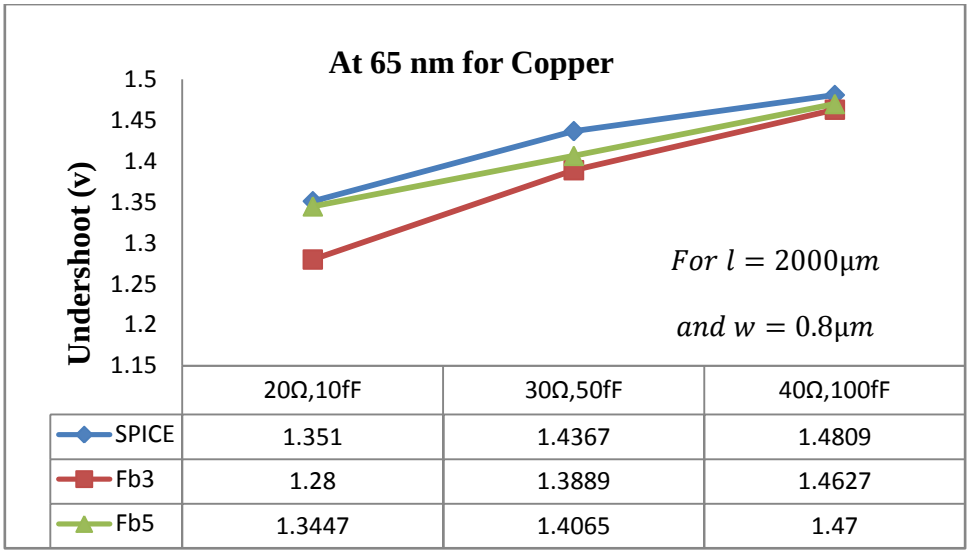


	20Ω,10fF	30Ω,50fF	40Ω,100fF
CNT(W=0.8μm)	1.088	1.267	1.243
Cu(W=0.8μm)	1.351	1.4367	1.4809

(b)

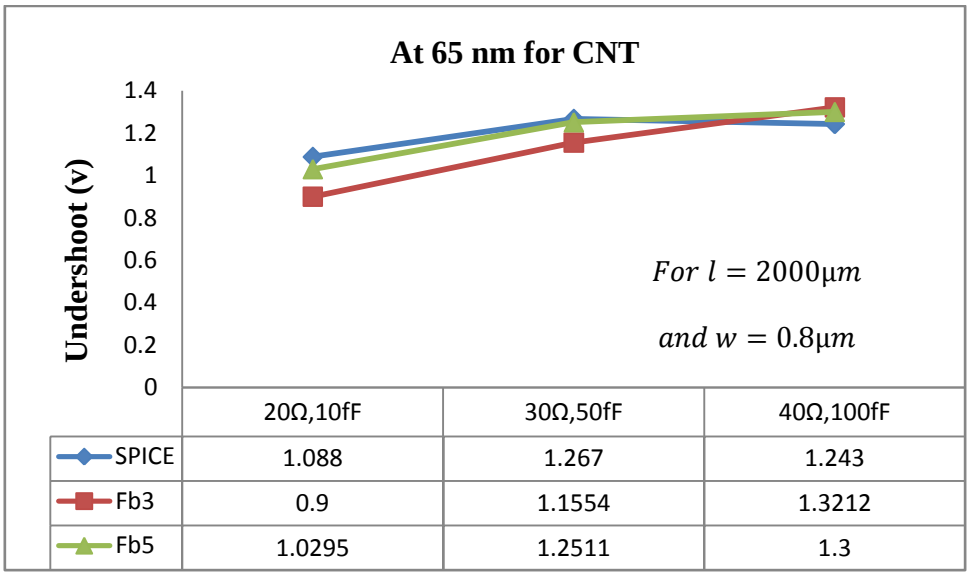
Fig. 4.26 (a) SPICE Undershoot Comparison at different widths at **180nm**

(b) Undershoot comparison of CNT and Copper at **65nm**



	20Ω,10fF	30Ω,50fF	40Ω,100fF
SPICE	1.351	1.4367	1.4809
Fb3	1.28	1.3889	1.4627
Fb5	1.3447	1.4065	1.47

(a)



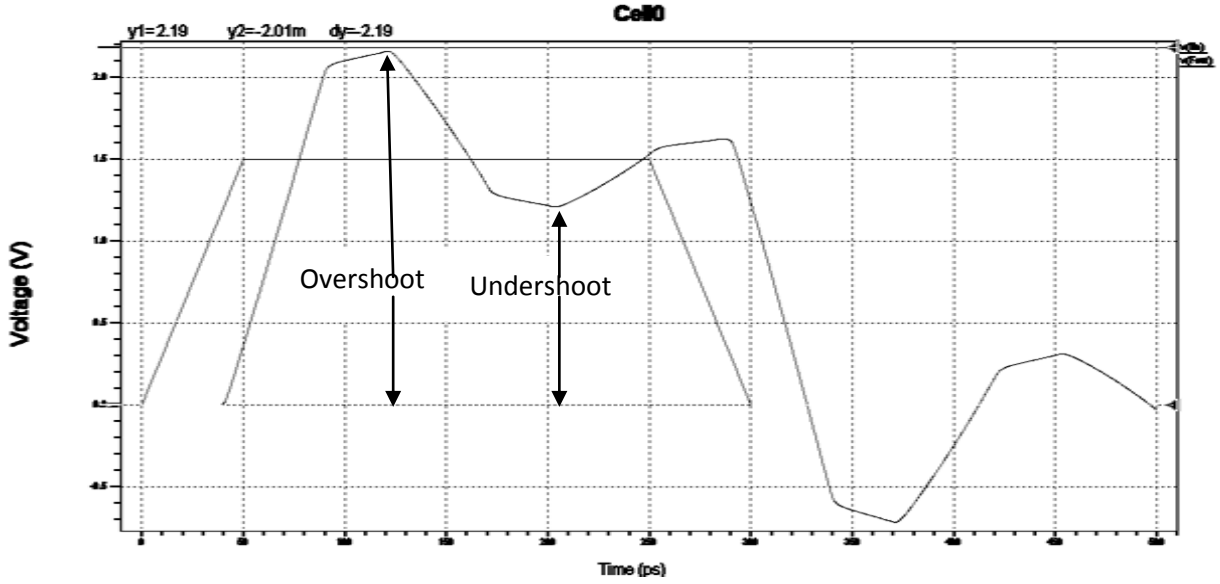
	20Ω,10fF	30Ω,50fF	40Ω,100fF
SPICE	1.088	1.267	1.243
Fb3	0.9	1.1554	1.3212
Fb5	1.0295	1.2511	1.3

(b)

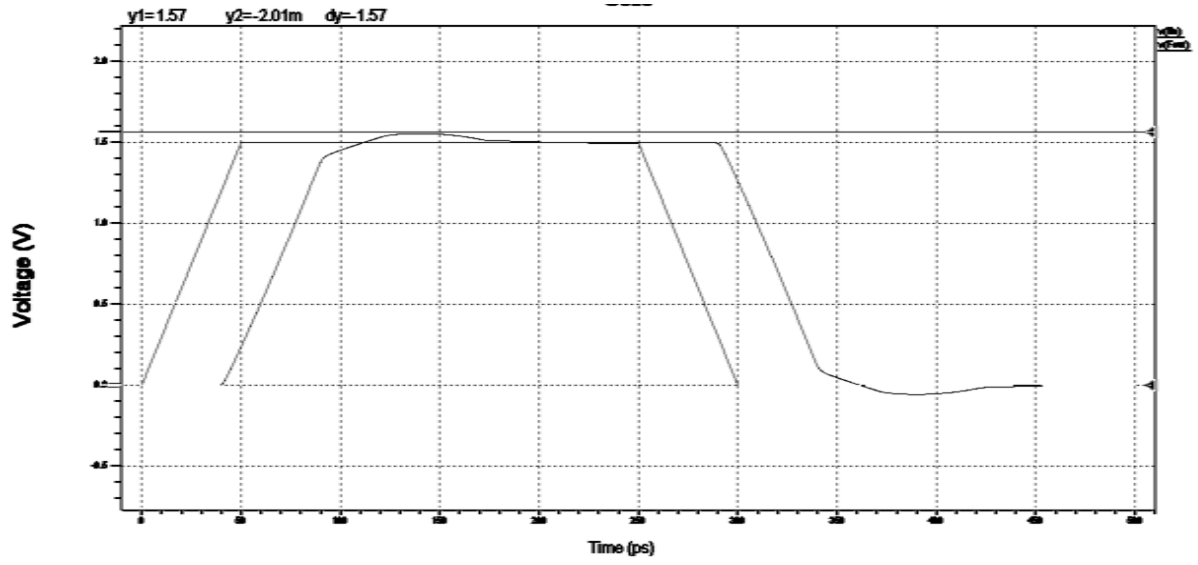
Fig. 4.27 Comparison of SPICE undershoot results with OUT3 (Fb3) and OUT5 (Fb5) at 65 nm for $w = 0.8\mu m$ (a) copper (b) SWNT.

Fig. 4.26 (a), (b) and **Fig. 4.27 (a), (b)**shows the variation of undershoot with driver resistance and varying load capacitor. It is observed that as the driver resistance is increased, the inductive effect (ζ) diminishes because of prominance of resistance in the impedance, Z=R+j ω L. Therefore, if the interconnect resistance increases, inductive effect can be neglected. But this would simulatneouly degrade the interconnect's speed. Load variation has slight impact on oveshoot and unershoot.

Also undershoot increases with increase in width as shown in **Fig 4.26 (a).**By switching to lower technology the underhoots are decreased. The reason is same as defined for overshoots.**Fig. 4.27 (a), (b)** shows that OUT3 (Fb3) and OUT5 (Fb5) are very accurate.



(a)



(b)

Fig. 4.28 Graph showing the variation of overshoot and undershot with R_d (a) $R_d = 10\Omega$ (b)$R_d = 60\Omega$.

It is observed in **Fig. 4.28(a) and (b)** for $R_d = 60\Omega$, inductive effect can be neglective as the systemapproaches to overdamped system.

4.5 SUMMARY

In this chapter the fitness of CNT bundles as a future interconnects has been investigated. For various properties of CNT bundles and Cu interconnects have been compared and observed that CNT's are free from the problem of electro-migration, surface and grain boundary scattering with high activation energy. High current carrying capacity is also considered for emerging technology. Further Fourier series is used for representation of practical on-chip signals has been exploited and found to be one effective technique for time domain solution for *RLC* interconnect. This mechanism is highly suitable in circuit level designs and early transient behavior of periodic signals can be estimated. Non approximated amplitude transfer function for Cu and SWCNT material is analysed and high amplitude peaks are observed as expected in SWCNT. With the help of damping factor, inductance effect is monitored in three different ways by using total line resistance, driver resistance, and time constant of load with characteristic impedance and time of flight of line respectively. It is observed that for low resistance materials increases overshoots. Hence, performance and reliability degrades. Using trigonometric methods relationships for 50% delay, overshoot and undershoot are formulated for Cu and SWCNT. These are verified by SPICE simulations with variation in technology and driver resistance. The results are found within an average error of about 0.6% in case of Fb5 and 3.7% for Fb3 are in close agreement with SPICE simulation. This presents exact modelling of fundamental resistance and inductance effect of SWCNT interconnects. From the modelling it is observed that the inductive effect is dominating in SWCNTs. It is also observed that the accuracy of SWCNT/Cu can be further improved if higher order harmonics are considered.

In the succeeding chapter the application of low swing in SRAM architecture has been presented to study the voltage swing effect on the data-lines/bit-lines and the performance dependency on the parasitic associated with the data-lines.

Chapter 5

MODELLING AND UTILIZATION OF LOW SWING ON DATA-LINES AND LOW IMPEDANCE RECEIVER

5.1 INTRODUCTION

In this chapter the bit-line voltage swing in case of memory architectures is studied. In case of SRAM column Input/Output circuitry, which includes bit-line precharge circuits, column multiplixers, read and write circuits have been investigated and performance analysed. Memory architecture is mapped equivalent to current mode interconnect system as reported in **Fig. 5.1 (a).** Long bit-lines/data-lines are considered as a long interconnect line. Further the effect of voltage swing with long data-lines is explored as an application of low swing in memory architecture. Current mode interconnect system consist of driver interconnect and receiver circuit with a resistive loading is presented below in **Fig. 5.1 (a).**

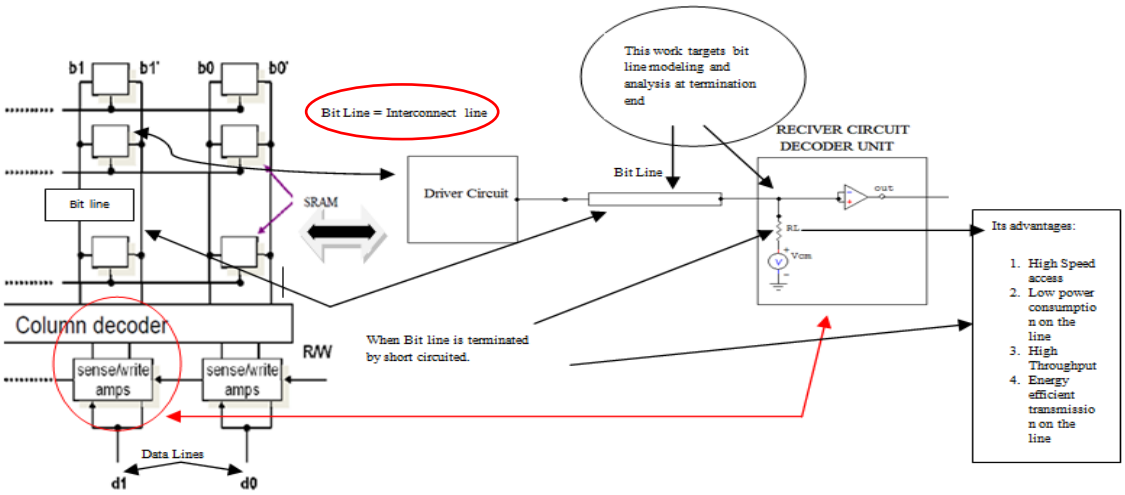


Fig. 5.1 (a) Memory architecture with data and databar lines and equivalent representation.

In this arrangement SRAM cell are taken as driver circuit to transmit a signal on long bit-lines/data-lines. And sensing circuitry is considered as receiver circuitry for detecting and decoding the low swing signal of data-line into corresponding logic value. One column circuitry arrangement of **Fig. 5.1 (a)** is presented in highlighted form with **Fig. 5.1 (b)** for detailed analysis of data-lines signal dependency with voltage swing, cell currents and cell size is investigated further. As the voltage swing on data-line is related with SRAM cell current. Because of this SRAM cell is taken as a driver circuit on data-line/bit-line, which are

considered as interconnect line for the analysis of effect of voltage swing in practical applications like as memory architectures. Impact and importance of voltage swing is already discussed in previous chapters. So in this chapter we are focussed towards the implementation of effect of voltage swing in practical circuits.

To study the practical effect of the interconnect lines, voltage swing and cell current dependency on data-lines is investigated. During the write and read operations, the data-lines (also called as bit-lines) are kept at high voltage, initially near to V_{DD} rails in case of memories. The circuits components depend on the type of sensing circuit to be utilized for precharge the bit-lines for read operation. **Fig. 5.1** (b) presents one of the possible precharge circuit configuration arrangements.

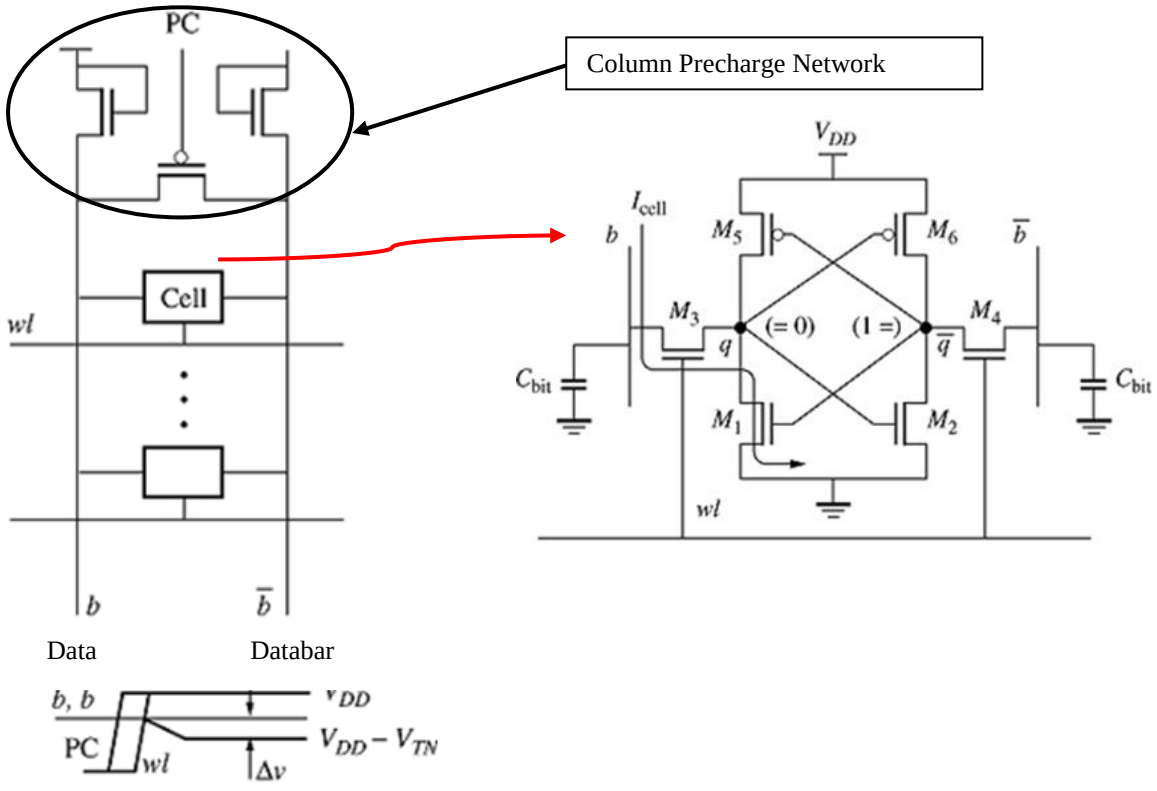


Fig. 5.1 (b) SRAM column pull up configuration (with 6T Memory Cell).

The precharge network can also be implemented by the other way as mentioned below in **Fig.5.2**. A precharge signal PC is applied to the pull ups and a third transistor called as the balance transistor, connected between the two data line in order to equalize their voltage level

at data and data bar lines. When the world line (wl) goes high, on data-line remains high and the other falls at a linear rate until wordline (wl) goes low. The difference between the datalines is fed into a voltage sensing latch –based amplifier that is triggered when the differential voltage exceeds a certain threshold.

(a) (b)

Fig. 5.2 Possible precharge networks.

Circuit shown in **Fig. 5.1 (b)** is designed using NMOS as diode connected enhancement load operating in saturation region. Hence, the maximum available voltage swing on the data line is $V_{DD} - V_T$. Balanced transistor is biased by PC signal and, it helps in equalizing the potential on both the data lines. As the data line is precharge to high potential, PC signal becomes turned off and then worldline reaches to high. At this point of instant, the pull-ups are still ON. The current will start to flow through one of them into the cell side with the stored "0" as shown in **Fig. 5.1 (b).** A steady state output level will be achieved by the corresponding data lines as reported in the **Fig. 5.1 (b)**. This type of configuration is suitable for differential voltage sensing amplifiers. This lower voltage is suitable for proper biasing & output swing.

The read circuitry of SRAM architecture works only when the world line becomes high. SRAM cell transistor will draw a current from highly capacitive column during read operation. Hence the data lines potential drops slowly and results in larger access times. In case of reduction of access time, the memory should be designed for small voltage change on one column or data line. More than two amplifying stages are required to generate a valid logic output. This is valid when the voltage difference between data and databar is approximately 100-200mV. In memory architecture the data-lines are sometime called as bit-lines. Bit-lines are very large and lengthy with high value of capacitance. These numbers of

bit-lines/data-line and capacitance associated with the data-lines increases as size of memory increases. Hence, the design of cell requires efficient selection of all six transistor of **Fig. 5.1 (b)** for successfully read and write operation. As the cell is symmetric, only designing of three transistors is more important. That may be M_1, M_3, M_5 or M_6, M_4& M_2. The important issue is to select the size by the way that minimizes the area and provides good performance, better read and write stability and good cell read current.

Hence, the design process of SRAM structure is discussed and presented for 200mV of voltage swing on the data lines in required time for different technology node. Dependency of voltage swing with time, cell current, data line capacitance and cell transistors is investigated and analysed.

Moreover, SRAM Cell deign parameters includes the Cell Area & Power Consumption. The major design effort in SRAM designs is minimising the Cell Area & Power Consumption. Hence, millions of cells can be placed on a chip. At steady state the power consumption of the cell is controlled by sub-threshold leakage currents. Hence, larger threshold voltage is often used in memory circuits. For minimization of these leakage components in a cell an optimum bulk signal has been developed. With the help of optimum bulk signal threshold of the transistor is raised and leakage by each device in 6T cell is controlled. With the help of optimum signal the power dissipation is also optimised. For minimization of cell area the cell design ratio and cell transistor are modelled and designed keeping in view the minimum the size area of cell without degrading the output response of cell.

5.2 VOLTAGE SWING AND CELL CURRENT DEPENDENCY ON DATA-LINES

In this section the voltage swing dependency with the 6T transistors is explored. In **Fig. 5.3** the portion A & B are symmetric to each other & the designing of transistor size M_3, M_1& M_5 will be same as M_6, M_4& M_2. During the read operation of SRAM cell the design process of access transistor in 6T cell is prime important i.e. M_3. For modelling the read operation, the prior value on $q$is assumed at "0" and $\bar{q}$ is set at the value of "1" as shown in **Fig. 5.3**. It must be ensured that the stored values that for read stability, logic values must not disturbed in the read cycle. The main problem is that as the current start to flow through M_3 and M_1, the potential at the output node q will start to rise up and it will make M_2 to turn ON. Due to this voltage of node $\bar{q}$ will start to drop. It should not drop below the threshold voltage of inverter as shown in **Fig. 5.3**. In this situation the alteration of state of the cells can be avoided by proper sizing the transistors M_1 and M_3. This can be achieved by making the pull down

transistor (M_1) stronger than the access transistor (M_3). In other words M_1 should be greater than M_3 in size. The voltage of node q should not exceed the value of threshold of NMOS (V_{TN}). Hence the read cycle establish the relation between the two devices. The relationship between cell current $I_{6T\ cell}$ as shown in **Fig. 5.3** and data-line capacitance can be given by equation (5.1)

$$I_{6TCell} = C_{data\ Line} \frac{dV}{dt} \tag{5.1}$$

$$\frac{dV}{dt} = \frac{I_{6TCell}}{C_{data\ Line}} \tag{5.2}$$

From the equation (5.2) it is clear that $I_{6T\ cell}$ is dependent on the rate of change of voltage on data line and large data line capacitance. $\frac{dV}{dt}$ provides the information about the rate of discharge of data-lines. If a rapid full swing discharge is required, then $I_{6T\ cell}$ larger value is desired. To accomplish above task it is necessary to make the size of access transistor and pull down network transistors of big sizes. Due to big size transistors the area and power dissipation will be larger. Because of presence of millions of such cells, power dissipation becomes huge. To apply a different approach, it is necessary to add a sensing unit to data-lines for detecting the small voltage difference.

An example for designing the read operation in SRAM and concluding the effect of voltage swing with respect to various design parameters is considered.

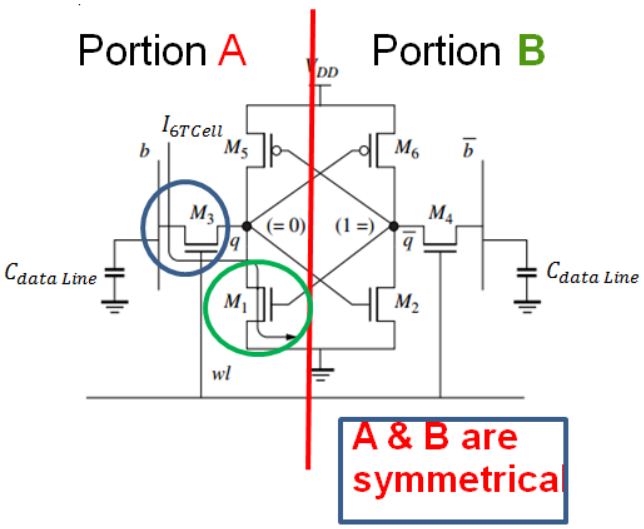


Fig. 5.3 Access transistor modeling during read operation.

DURING READ CYCLE: Portion A is designed, i.e. for a read operation cell current M_3 M_1 transistors are designed. For Read cycle, if $q = 0$ & $\bar{q} = 1$ are stored, then these should remain as it is.This will become possible only when potential of q<threshold voltage of M_2 [138].

Thus,

$$\frac{W_1}{L_1}\frac{\mu_n C_{ox}}{\left(1+\frac{V_q}{E_{CN}L_1}\right)}\left[(V_{DD}-V_{T1})V_q-\frac{V_q^2}{2}\right]=\frac{W_3 v_{sat} C_{ox}(V_{DD}-V_q-V_{T3})^2}{(V_{DD}-V_q-V_{T3})+E_{CN}L_3} \tag{5.3}$$

$$\frac{W_1}{W_3}\cong 2.77$$

Whereas, $\mu_n, C_{ox}, v_{sat}, E_{CN}, E_{CN}L, V_q$ represent electron mobility, oxide capacitance, velocity saturation, Critical field, Critical Field x L, Voltage at node q respectively.

This value of device size actually depends on the desired rate of change of the data-line voltage & the delay time and $I_{6T\,cell}$ (cell current). If the data-line is designed for 200mV of voltage transition achieved in time of 2ns with a total data-line capacitance of 2pF. The$I_{6T\,cell}$ cell current can be calculated as:

$$I_{6TCell} = C_{data\ Line} \times \frac{\Delta V}{\Delta t} = 199.62\mu A \tag{5.4}$$

The current through M_3 device can be computed as:

$$I_{6TCell} = \frac{W_3 v_{sat} C_{ox}\left(V_{DD}-V_q-V_{TH3}\right)^2}{\left(V_{DD}-V_q-V_{TH3}\right)+E_{CN}L_3} \tag{5.5}$$

Here $v_{sat} = 8 \times \frac{10^6 cm}{s}, C_{ox} = \frac{1\mu F}{cm^2}, V_{DD} = 1.8V, V_q = 0.1V, V_{TH} = 0.5V.$

This results in:$W_3 = 0.416\mu m$

$$=> W_1 = 1.15\mu m$$

With these sizes of the access transistors and pull down network are implemented. The transistors W_5 and W_3 have the relations of device size given by equation (5.6)

$$\frac{W_3}{1.5} = W_5$$

(5.6)

The size of these devices can further be reduced if the effect of body is incorporated with design equation as reported in equation (5.3). It means that the ratio $\left(\frac{W_1}{W_3}\right)$ can further be reduced. The device sizes are optimized by simulative sweep analysis techniques and presented in Table 5.1. Further these design parameters has calculated at various technology node such as 350nm, 250nm, 180nm and130nm.The impact of voltage swing and cell current is introduced with technology scaling and reported in **Fig. 5.4**.

Table 5.1 Calculation of Cell current at Different Voltage Swing & Device Sizes with $\mathrm{dt} = 2\mathrm{ns}, \mathrm{C_{data\ Line}} = 2\mathrm{pF}, \mathrm{V_{DD}} = 1.8, \mathrm{V_{TH}} = 0.5\mathrm{V}, \mu_n = \frac{270\,\mathrm{cm}^2}{\mathrm{V-sec}}, \mathrm{V_q} = 0.1\mathrm{V}, \mathrm{v_{sat}} = 8 \times \frac{10^6\mathrm{cm}}{\mathrm{s}}, \mathrm{E_c} = 6 \times \frac{10^4\mathrm{V}}{\mathrm{cm}}$

Data line Voltage Swing (mV)	I_{6TCell} (µA)	W_3 Access Transistor (µm)	W_1 Pull Down Tran. (µm)
50	50	0.104	0.289
100	100	0.208	0.578
150	150	0.313	0.867
200	200	0.417	1.16
250	250	0.521	1.44
300	300	0.625	1.73
350	350	0.729	2.02
400	400	0.833	2.31
450	450	0.938	2.60

The calculations presented above and discussed in **Table 5.1** match for voltage swing of 200mV.Voltage swing on the long data-lines is related to cell current$(I_{6T\ Cell})$ and cell ratio $\left(\frac{W_1}{W_3}\right)$is also related with the cell current.

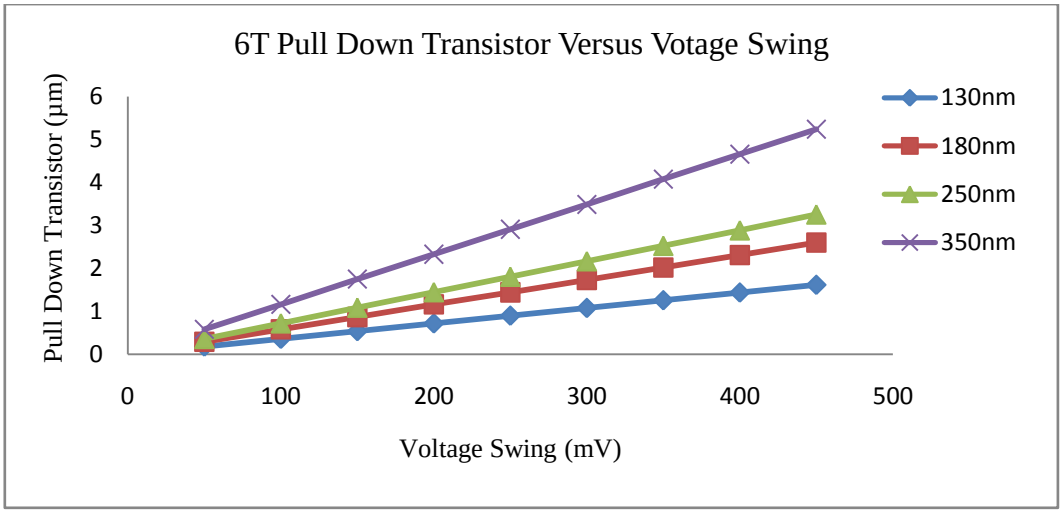


Fig. 5.4 Voltage swing variation at different technology node.

Table 5.2 Optimized value of Access Transistor (M_3), Pull up (M_5) & Pull down Transistor (M_1) at 180nm Technology Node

Device Sizes	Read Delay (ps)	Write Delay (ps)	Power Consumption (µW)
$(W_1 = 1.15\mu m, W_3 = 0.416\mu m \; \& W_5 = 0.277\mu m)$	33.8	11.69	26.43
$(W_1 = 1.05\mu m, W_3 = 0.406\mu m \; \& W_5 = 0.265\mu m)$	31.16	11.50	25.63
$(W_1 = 1.00\mu m, W_3 = 0.396\mu m \; \& W_5 = 0.255\mu m)$	30.93	16.02	24.95
$(W_1 = 0.95\mu m, W_3 = 0.370\mu m \; \& W_5 = 0.230\mu m)$	31.01	16.12	23.26
$(W_1 = 0.80\mu m, W_3 = 0.340\mu m \; \& W_5 = 0.220\mu m)$	NF	NF	22.57

NF : stand for Not found

The optimized read and write delay with power consumption at 180nm technology node are presented in **Table 5.2** and optimized sizes are within the value of $(W_1 = 0.95\mu m, W_3 = 0.370\mu m \; \& W_5 = 0.230\mu m)$ these dimensions. Cell area is saved by 17.39% for pull down network & access transistor area is saved by 11.05% become smaller. Power consumption is minimized by 11.99% for 200mV voltage swing and corresponding cell current of 200µA. For any value of cell current & voltage swing on data-lines/bit-lines can be optimized for calculated values.

Furthermore, the same is explored for the 1M bit Serial SRAM device by Microchip Technology Inc. 23A1024 practical SRAM design specifications, as the cell read current of 3.3mA at operating voltage range 2.5 to 5.5V, 20MHz clock rate and stand by current 4µA at 85℃ . The density of chip is 1024k bits. Now the calculation at read current of 3.3mA at voltage at 2.5V is presented below at 180nm technology node.

5.3 CELL CURRENT DEPENDENCY OF MICROCHIP SRAM OF 1MB SIZE

In this section the cells design parameters and their dependency on voltage swing for read current for 1Mb SRAM by Microchip Technology Inc. 23A1024 is presented and investigated. From the data sheet of SRAM 23A1024 the cell read current of 3.3mA is reported at 2.5V with a clock rate of 20MHz. The corresponding cell size and voltage swing calculation are presented below. The exact calculation is provided with approximate size of SRAM access transistor and pull down transistor sizing. The value used for achieving the required cell current is presented in **Table 5.3**. The cell current of 3.45mA is achieved at voltage swing of 450mV with the cell ratio of 3.45. Here, the calculated cell current matches the value of cell current of 1Mb SRAM by microchip technologies.

Table 5.3 Calculation of Cell Current at Different Voltage Swing & Device Sizes with 180nm Node, $dt = 30ps, C_{data\ Line} = 230fF, V_{DD} = 2.5V, V_{TH} = 0.5V, \mu_n = \frac{270\,cm^2}{V-sec}, V_q = 0.1V, v_{sat} = 8 \times \frac{10^6 cm}{s}, E_c = 6 \times \frac{10^4 V}{cm}$

Data line Voltage Swing (mV)	I_{6TCell} (mA)	W_3 Access Transistor (µm)	W_1 Pull Down Tran. (µm)
50	0.383	0.411	1.426
100	0.767	0.823	2.84
150	1.15	1.23	4.26
200	1.53	1.65	5.68
250	1.92	2.06	7.10
300	2.30	2.47	8.52
350	2.68	2.88	9.94
400	3.07	3.29	11.4
450	3.45	3.70	12.8
500	3.83	4.11	14.2

The impact of data-line/bit-line capacitance on cell current and cell ratio is investigated for 200mV of voltage swing at 2ns. It is observed that as the capacitance associated with

interconnect line increases then the cell current also increases. This is reported in **Fig. 5.5** for 200mV of voltage swing.

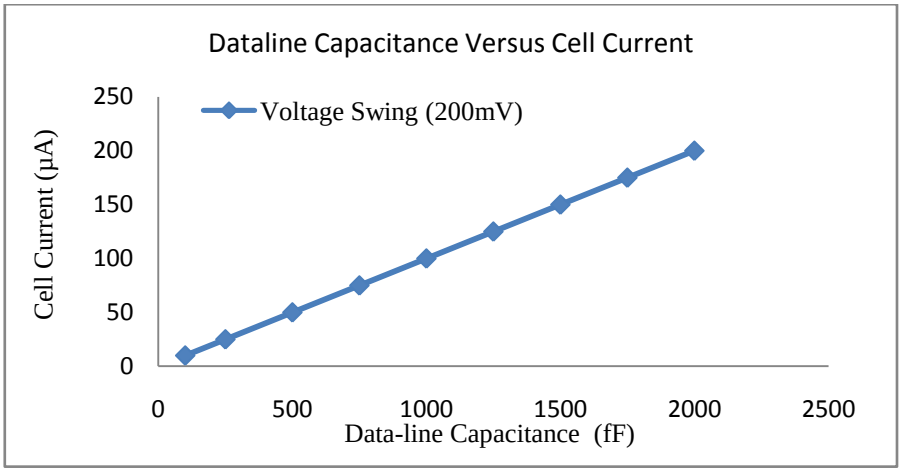


Fig. 5.5 Cell current variation with data-line capacitance at constant voltage swing.

Voltage swing is an important design parameter from power dissipation point of view in current mode signaling. Due to the low impedance termination voltage swing on the interconnect line remains always very small. The small voltage swing helps in minimization of dynamic power component on the line as well as responsible for small charging and discharging time constant. The current mode signaling technique is helpful in applications like SRAM sensing circuits. This part of voltage swing of SRAM can further be modeled for sensing the small voltage swing on data-lines.

5.4 MODELING & SIMULATION OF LOW IMPEDANCE RECEIVERS FOR CURRENT MODE SCHEMES

In this section modeling and simulation of receiver circuits reported in [21] are presented and verified by SPICE simulations. This works presents the mathematical formulations and verification by small signal model analysis for all the receiver circuits reported in [21].

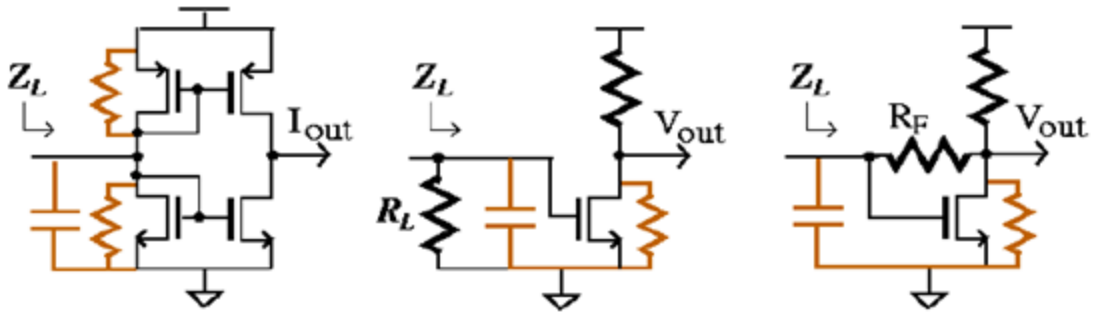
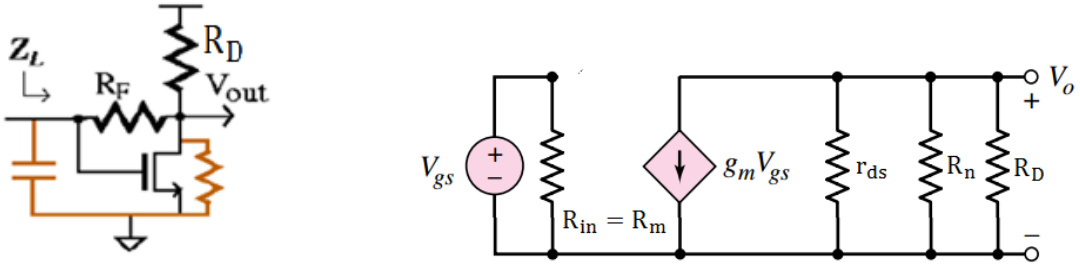


Fig. 5.6 Low impedance receiver topology for Current Mode Schemes [21].



(a) (b)

Fig. 5.7(a) Receiver Circuit-1and (b) its Small signal model.

In the receiver circuit 1 **Fig. 5.7 (a)** R_D and R_F are taken as drain and feedback resistor. Small signal Model of **Fig. 5.7 (a)** is reported in **Fig. 5.7 (b)**. For the analysis of input and output impedance of receiver topology R_D and R_F are taken as 150 kΩ and 50 kΩ respectively. And the value of G_{DS} is directly taken from output file and corresponding r_{ds} is calcuted.

$$G_{DS} = 8.0409\mu \qquad \text{(Appendix1)}$$

$$r_{ds} = \frac{1}{G_{DS}} = 124.36\ k\Omega \qquad (5.7)$$

$$R_n = \frac{R_F}{\left(1+\frac{1}{A_v}\right)} = \frac{50000}{1+0.5} = 33.22k\Omega \qquad (5.8)$$

$$R_m = \frac{R_F}{(1+A_v)} = \frac{50000}{1+2} = 16.67k\Omega \qquad (5.9)$$

$$R_{out} = R_n||R_D||r_{ds} = 33.22k\Omega\ ||150\ k\Omega||124.36k\Omega \qquad (5.10)$$

$$R_{in} = R_m \qquad (5.11)$$

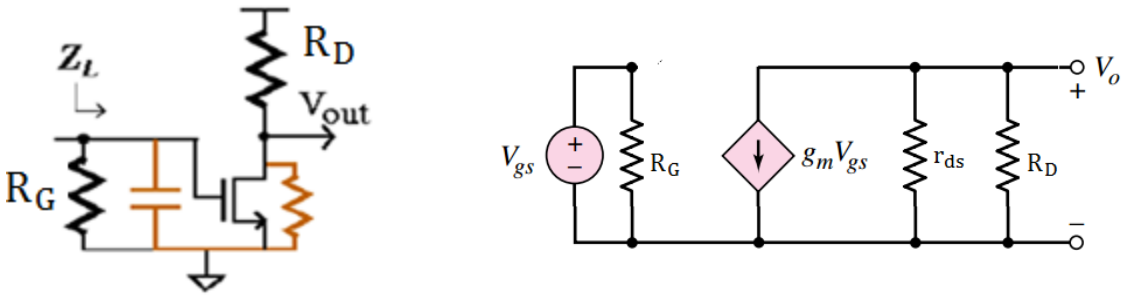
With these entire design variables the value of input and output impedance is computed using SPICE simulation program. And the output is attached as a reference in Appendix1. The simulated output value as such as :

Table 5.4 Simulated versus Theoretical values of input and output impedance

	Simulated Values	Theoretical values
A_v = Gain	2	2
Input resistance	16.68 $k\Omega$	16.67 $k\Omega$
Output resistance	28.81 $k\Omega$	22.32 $k\Omega$

In this topology the input impedance obtained is 16.67kΩ. So the value of this impedance is reduced further in Circuit 2.

Receiver circuit 2 of **Fig. 5.6** small signal model and input impedance calculation is reported in **Fig. 5.8**. SPICE output file is added in Appendix 2 for reference. For Circuit 2 the obtained input impedance of the circuit is 5kΩ.



(a) (b)

Fig. 5.8 (a) Receiver Circuit 2 (b) Small Signal Model of Circuit 2

In this circuit 2 of **Fig. 5.8** by setting the value of R_D and R_G and G_{DS} form output file (Appendix 2) are taken and according the calculation for the receiver circuit 2 of **Fig. 5.8** (b) are presented.

$$R_D = 150\ k\Omega$$

$$R_G = 5\ k\Omega$$

$$G_{DS} = 8.1769\mu \quad \text{(Appendix 2)}$$

$$r_{ds} = \frac{1}{G_{DS}} = 122.29\ k\Omega \quad (5.12)$$

$$R_{in} = R_G = 5\ k\Omega \quad (5.13)$$

$$R_{out} = R_D || r_{ds} = 122.29\ k\Omega || 150k\Omega = 67.37k\Omega \quad (5.14)$$

Using this receiver circuit 2 the value of gain is obtained is 5.579 and with simulations a high of input and output impedance is obtained. The current sensing circuits always needs low value of input impedances. By using circuit topology 3, input impedance has been reduced further and small signal modelling is presented in receiver Circuit 3.

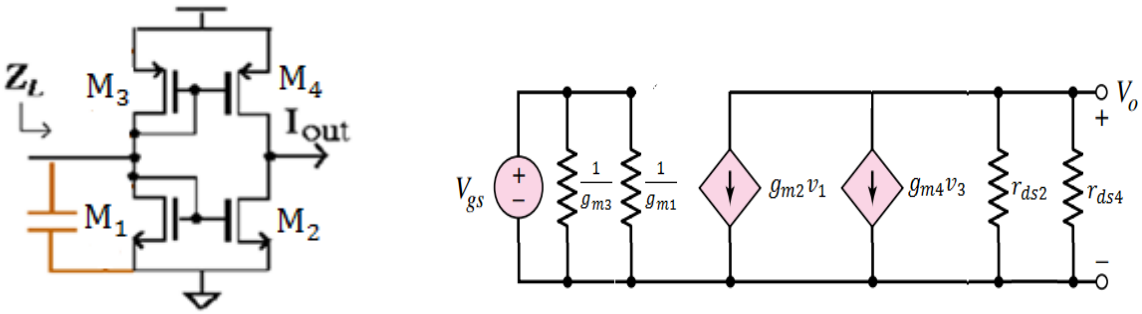


Fig. 5.9 (a) Receiver Circuit 3 (b) Small Signal Model

Small signal Model Analysis for the circuit 3 is presented below. The value of G_{DS2} G_{DS4} , g_{m3}, g_{m1} has been taken from output file which is attached as reference in Appendix 3. The values are such as:

$$G_{DS2} = 9.167\mu$$

$$G_{DS4} = 27.087\mu$$

$$g_{m3} = 112.21\mu$$

$$g_{m1} = 3.46m$$

Further the value for r_{ds2} and r_{ds4} are calculated as :

$$r_{ds2} = \frac{1}{G_{DS\,2}} = 109.1\ k\Omega \quad (5.15)$$

$$r_{ds4} = \frac{1}{G_{DS\,4}} = 36.92\ k\Omega \quad (5.16)$$

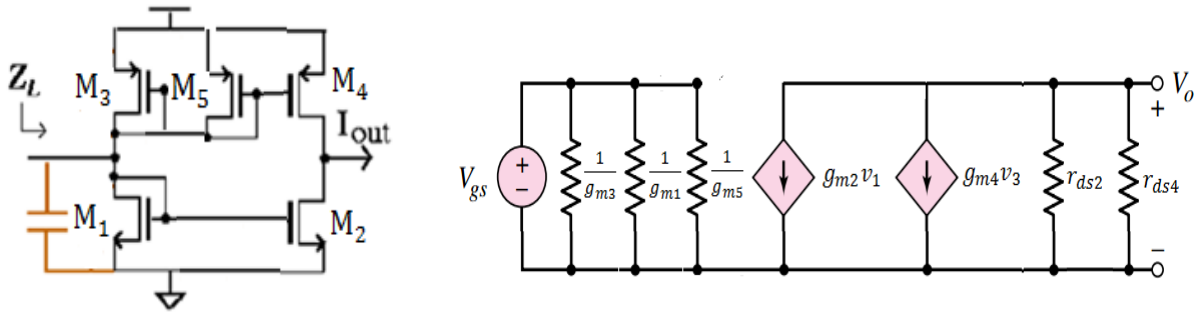
And the value of input impedance will be such as the parallel combination of output resistance of M_3 and M_1. And output impedance will be the parallel combination of M_2 and M_4. The calculation for both the input and output impedance is presented below.

$$R_{in} = {}^{1}/_{g_{m3}} \,||\, {}^{1}/_{g_{m1}} = 8.912k\Omega||289.01\ k\Omega \tag{5.17}$$

$$R_{in} = 280\ \Omega$$

$$R_{out} = r_{ds2}||r_{ds4} = 109.1\ k\Omega||36.92k\Omega = 27.58k\Omega \tag{5.18}$$

The value of gain is obtained is 5.05 form simulation results. This value of gain has been used in further calculations. In this configuration the input impedance has been reduced upto the value of 280Ω. This arrangement of transistors can be named as Modified improved Wilson current mirror configuration. The current from input side of receiver termination is mirrored at the output terminal. Further the load configuration has been modified and presented in **Fig. 5.10** with small signal model calculation. SPICE output file is added in Appendix 3 for reference.



(a) (b)

Fig. 5.10 Modified Receiver Circuit 4 (b)Small Signal Model for Modified Circuit

Small signal model analysis of modified receiver circuit 4 is presented below. The following data value is taken from SPICE output file for calculations (Appendix 4):

$$G_{DS2} = 9.167\mu$$

$$G_{DS4} = 27.087\mu$$

$$G_{DS5} = 13.068\mu$$

$$g_{m3} = 112.21\mu$$

$$g_{m1} = 3.4594\ m$$

$$r_{ds2} = \frac{1}{G_{DS\,2}} = 109\ k\Omega \tag{5.19}$$

$$r_{ds4} = \frac{1}{G_{DS\,4}} = 36.92\ k\Omega \tag{5.20}$$

$$r_{ds5} = \frac{1}{G_{DS\,5}} = 76.52\ k\Omega \tag{5.21}$$

$$R_{in} = 8.91k\Omega \| 0.289\ k\Omega \| 76.52k\Omega = 249\ \Omega \tag{5.21}$$

$$R_{out} = r_{ds2} \| r_{ds4} = 109\ k\Omega \| 36.92k\Omega = 27.58\ k\Omega \tag{5.22}$$

The value of gain is 5 is obtained from simulative analysis. This value of gain has been used further for calculation of input and output impedance. In Table 5.5 the comparison for input impedance of receiver circuit for all the configurations is presented.

Table 5.5 Comparison of input impedance of receiver circuit

	Input Impedance	Output Impedance
Receiver Circuit 1	16.68 $k\Omega$	28 $k\Omega$
Receiver Circuit 2	5 $k\Omega$	67.37 $k\Omega$
Receiver Circuit 3	257 Ω	27.58 $k\Omega$
Modified Receiver Circuit	249 Ω	27.58 $k\Omega$

For receiver circuit 4 configurations, the input impedance achieved is 249 Ω using current mirror load configuration. SPICE output file is added in Appendix 4 for reference.

5.5 SUMMARY

In this chapter the practical application of interconnects as data-lines / bit-lines for computing and studying the effect of the voltage swing in SRAM architecture has been carried out. This has been accomplished with the help of examples and for a practical 1Mb SRAM designed by Microchip Technologies. From this analysis it is investigated that voltage swing on the data-line/bit-line is dependent on the cell ratio and on cell read current. Voltage swing dependency on the data-line capacitance associated with the global bit-lines is also dealt-with. Further, for the receiver part of a current mode system, mathematical modelling of low input impedance receivers is presented and a minimum of 249Ω input impedance is achieved. The work presented in the current chapter provides a practical application and utility of the interconnect lines studied in the previous chapters.

Chapter 6

CONCLUSION AND FUTURE SCOPE

VLSI interconnect have been studied for several decades for low power and high density Network on a Chip. Understanding of Current Mode interconnects for microelectronics is a complex and continually evolving challenge. In this thesis the fitness of Cu and CNT bundles as a future interconnects has been investigated using various mathematical Models by keeping in view the material requirement of interconnect. Various properties of CNT bundles and Cu interconnects have been compared. It has been found that CNTs are free from the problem of electro-migration, surface and grain boundary scattering with high activation energy and high current carrying capacity and considered as emerging technology.

6.1 CONTRIBUTIONS OF THE THESIS

In this thesis three mathematical models are proposed using different approaches for formulation of delay for global VLSI interconnects. In the proposed Model I $R_{eff}C_T$ the delay of RLC interconnects line is formulated by incorporating the line inductance in terms of effective impedance. Using this approach the results for both the signaling technique i.e. voltage and current mode signaling are found in close agreement between analytical and simulation for long interconnect lines.

Inductance effect can be reduced by increasing width and thickness of line. It can also be reduced by the low value of permittivity and permeability of the surrounding dielectric. Damping factor (DF) of RLC interconnect line is also exploited for avoiding the effect of same. DF is also useful and important parameter which helps in mitigating the inductance effect of a line.

The proposed Model-I $R_{eff}C_T$ is compared with Elmore Delay Model. After comparison it has been observed that the relative average error between them is 1.01% where as maximum error is 1.7% and minimum is 0.49% for 2mm to 10mm length of interconnect. By using the proposed approach $R_{eff}C_T$ model generates the equivalent results to Elmore Model on

comparison. It is further observed that the error for smaller length is greater than the longer lengths. It remains within the range of 3% for longer length whereas for smaller length the average error is 33%. Hence it is not suitable for smaller length. Its suitability is better for longer length of interconnects. The dominance of inductance effect is large for smaller length of interconnect. For global length the inductance effect remains to be very small for 6 to 10mm length of interconnect.

The proposed Model-I $R_{eff}C_T$ are compared with the results of the previous works. It is found that the CM signalling delay decrease for all lengths (2mm to 10mm) by an average value of 4.59% whereas for 4mm to 10mm lengths the results of proposed model in Current mode signaling decrease by an average value of 1.73%.

When compared the delay value of the proposed model current mode system to Sakurai delay, it has been observed that delay due to current mode system is 2.22 times lesser for longer length of interconnect. Hence, CM signaling is highly suitable for global length of interconnects.

CM delay decreases up to 67% when compared to voltage mode signaling and this increment remains almost same for 2mm to 10mm length of interconnect line. Hence, the throughput due to current mode system has increased maximum by 263% for 2mm length of line whereas for 10mm line it is increased by 200%.

By using current mode signaling the throughput has reached up to the value of 9Gbps for 10mm line whereas 2mm line it becomes 200Gbps. Thus there is a huge increment in throughput,but it decreases with the length of interconnects.

Using the proposed Model-II R_0C_0, the value of line impedance and capacitance are generated using the asymptotic value of characteristic impedance of RLC interconnected line. On the basis of this model the results are estimated for voltage and current scheme. The proposed Model II R_0C_0 delay in VM scheme has decreased by the 25.61% when compared to Eudes model for 10mm line. VM schemes show superior performance at global lengths when compared to the other existing models. Analytical results of proposed Model-II are compared with the SPICE simulations. After comparison it has been observed that the average error for all length is nearly 1.84%, whereas maximum error is 2.3%. The asymptotic

value of characteristic impedance is used for estimation of effective resistance and capacitance by exploiting the relationships ofα and β which are attenuation constant and phase constant respectively. The mathematical formulation developed by the proposed approach results in a superior and better performance.

For Current Mode Signaling the delay of proposed Model-II decreases upto 53%, 35%, and 20% for 10mm, 8mm, 6mm lines respectively, whereas for 2mm length & 4mm length lines it increases by 75%, when compared to the previous works. Hence, the suitability of proposed model is valid for global length of interconnects (i.e. top level global interconnects ranges from 15mm- 20mm).

Throughput for the R_0C_0 in Model-II increases up to 200% for 10 mm line, with the value of throughput being 33Gbps for CM (10mm) and it becomes maximum upto 42Gbps for 2mm line using Model-II, whereas the R_{eff} C_T Model I with CM model gives 9Gbps for 10mm line.

Model-III, gives the similar results of Model I by using the transmission line approach. The approach is different in both mathematical formulations. In this section a first order transfer function is investigated for current versus voltage mode signalling. The step response and bandwidth is also estimated for various length of VLSI interconnects. The rise time is calculated and verified for output signal form 10% to 90% of settling time within the tolerance of 2%. The dc coefficient on interconnect line is a useful parameter for exact calculation of power consumption on the line. The bandwidth is further estimated for different length of interconnect. Current mode signalling is found to be superior in bandwidth when compared to voltage mode systems. This proposed closed form representation is convenient for step input analysis and for bandwidth estimation for any length of interconnect line.

The technique of repeater insertion with optimal number repeaters to be inserted and size of repeater is investigated for current and voltage mode schemes. The results are found such as by using the current mode with proposed Model II R_0C_0 the delay factor reduced by an average value 2.67. Number of repeaters, reduce by an average value of 2.28 using current mode schemes. Thus if the same performance is required by voltage mode (VM) as compared to current mode (CM) system, it is necessary to increase the number of repeaters in voltage mode (VM) by the factor 2.28.

The proposed Mode III is validated at scaled technology at 45nm node and materialistic comparison with Al/Cu/CNT is obtained. The relative average error between analytical and SPICE simulation for CNT type material for Global interconnect 0.450%. Further for Local and intermediate interconnects is 2.1% and 3.9% respectively. It is found that CNT provides 81.78% reduction in delay when compared to Al and 86.80% when compared to Copper. In DSM the superiority factor for current mode scheme comparative to voltage mode remains 66.66%, once the load is shorted at termination end. Current Mode scheme dissipates 0.015pJ energy where as VM consume 0.045pJ for single bit transmission across the interconnect using CNT material. It has been observed that Current Mode signalling is three time superior than VM signalling.

From the power dissipation model it is clear that dynamic power dissipation component reduces drastically using CM schemes. Using current mode scheme the calculated average power is approximately 0.552mW in CM whereas in voltage mode the same dynamic power component is dominating drastically and average value approaches 4.735mW in VM. Hence, it is in fact a superior technique in terms of the saving the power or avoiding excess power dissipation in the clock network & global buses used in microcontrollers/microprocessors.

In this research work cell area is saved by 17.39% for pull down network & access transistor area is saved by 11.05% become smaller. Power consumption is minimized by 11.99% for 200mV voltage swing and corresponding cell current of 200µA. Similarly static power dissipation component in current mode signaling is dominating due to the low resistance path or low impedance termination at the load end. Using the proposed techniques of optimum bulk, self bias transistors (SBT) and stacking drivers the leakage components in driver and receiver circuit of current mode system is reduced.

In this research work the applicability of low swing is investigated with SRAM cell and column pull circuitry used in memory architectures. The cell read current dependency with voltage swing, access transistor & pull down network of back to back connected inverters is explained. The area of memory cell and power dissipation can be optimised. Because voltage swing of datalines/bitlines is very important for sizing of memory cells and for exact calculation of dynamic power component on datalines.

Ideally zero input impedance receivers are required for sensing the signal at the termination end in current mode schemes. This research work also investigated the modeling and simulation of low input impedance receivers which are reported in the literature. The achieved the input resistance of receiver circuit is 250Ω.

Further Fourier series is used for representation of practical on chip signals, this method is found to be effective technique for time domain solution for *RLC* interconnect. This mechanism is highly suitable in circuit level designs and transient behavior of periodic signals. Non approximated amplitude transfer function for Cu and SWCNT material is also analysed and high amplitude peaks are observed as expected in SWCNT. With the help of damping factor, inductance effect is monitored in three different ways using total line resistance, driver resistance and time constant of load with characteristic impedance and time of flight of line respectively. It is also observed that for low resistance materials there is increase in overshoots. Due to increase in overshoots performance and reliability degrades. Using trigonometric multiple angle formulae 50% delay, overshoot and undershoot are formulated for Cu and SWCNT. These are also verified by SPICE simulations with variation in technology and driver resistance. It is also observed within an average error of about 0.6% in case of fifth order (Fb5) and 3.7% for third order (Fb3) of harmonics are in close agreement with SPICE simulation. This research work presents exact modelling of fundamental resistance and inductance effect of SWCNT interconnects. SWCNT's found with high inductance effects. The accuracy can be further improved if numbers of harmonics are increased.

6.2 FUTURE SCOPE

The end of one research work is always a beginning and provides a scope for another.

- The mathematical models proposed in the present work can further be investigated for modelling the crosstalk. Noise analysis can also be incorporated. Ideal zero input impedance receiver can be searched and correspondingly the signals can be demodulated using efficient receiver circuits. The exact transfer function without truncation of transmission line can be solved for higher orders such 5^{th} and 7^{th} and 9^{th}order, so that the exact values of the delays may be calculated.

- In the modelling for SWCNT materials the impact of other components such as scattering resistance, quantum capacitance etc. can be incorporated and the value of delay, throughput, overshoot and undershoot can be estimated. Impact of process variation and noise on voltage swing can be investigated in case SRAM column architecture.

- In this research work the mathematical modelling and simulation work is carried out for different Models but no hardware implementation is presented. In future scope, the hardware implementation can be done to compare the experimental results with analytical and simulation results.

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APPENDIX

Model File

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**
**                    MOSIS PARAMETRIC TEST RESULTS
**
**         RUN: T26X (LO_EPI)                    VENDOR: TSMC
**   TECHNOLOGY: SCN018                          FEATURE SIZE: 0.18 microns
**
**T26X SPICE BSIM3 VERSION 3.1 PARAMETERS
**
**SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Aug 15/02
* LOT: T26X                WAF: 1011
* Temperature_parameters=Default
**
.MODEL NMOS NMOS (                          LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3796589
+K1      = 0.5935169    K2      = 2.38533E-3  K3      = 1E-3
+K3B     = 3.1905105    W0      = 1E-7        NLX     = 1.786849E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.7203781    DVT1    = 0.4308344   DVT2    = 0.0467521
+U0      = 269.0634518  UA      = -1.188565E-9  UB    = 1.930877E-18
+UC      = 2.224818E-11  VSAT   = 9.67502E4   A0      = 2
+AGS     = 0.4169677    B0      = -1.063955E-8  B1    = -1E-7
+KETA    = -7.704208E-3  A1     = 7.99632E-4  A2      = 0.999873
+RDSW    = 105          PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 2.025957E-9  LINT   = 1.028309E-8
+XL      = -2E-8        XW      = -1E-8       DWG     = -6.4982E-10
+DWB     = 1.217904E-8  VOFF    = -0.0901723  NFACTOR = 2.3820479
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.448044E-3  ETAB   = -2.754731E-4
+DSUB    = 0.0110906    PCLM    = 1.0622551   PDIBLC1 = 0.3172281
+PDIBLC2 = 3.755701E-3  PDIBLCB = -0.1        DROUT   = 0.783102
+PSCBE1  = 5.995957E10  PSCBE2  = 5.686023E-8  PVAG    = 0.3568363
+DELTA   = 0.01         RSH     = 6.7         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = 0           LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = 0            CAPMOD  = 2           XPART   = 0.5
+CGDO    = 7.45E-10     CGSO    = 7.45E-10    CGBO    = 1E-12
+CJ      = 9.725136E-4  PB      = 0.7292509   MJ      = 0.3610145
+CJSW    = 2.269386E-10  PBSW   = 0.6351005   MJSW    = 0.1
+CJSWG   = 3.3E-10      PBSWG   = 0.6351005   MJSWG   = 0.1
+CF      = 0            PVTH0   = -2.139932E-3  PRDSW  = -1.2311975
+PK2     = 1.860342E-3  WKETA   = 1.76355E-3  LKETA   = -5.667186E-3
+PU0     = -0.2295277   PUA     = -2.87112E-11  PUB    = 0
```

```
+PVSAT   = 1.427606E3     PETA0   = 1E-4          PKETA   = -1.196986E-3    )
*
.MODEL PMOS PMOS (   LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7          NCH     = 4.1589E17     VTH0    = -0.4215645
+K1      = 0.5955538     K2      = 0.0265154     K3      = 0
+K3B     = 10.7990376    W0      = 1E-6          NLX     = 7.393151E-8
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.3622323     DVT1    = 0.2560341     DVT2    = 0.1
+U0      = 119.2085214   UA      = 1.656038E-9   UB      = 1E-21
+UC      = -1E-10        VSAT    = 1.840486E5    A0      = 1.7659056
+AGS     = 0.4199318     B0      = 9.960505E-7   B1      = 3.37199E-6
+KETA    = 0.0126497     A1      = 0.4537105     A2      = 0.3
+RDSW    = 201.0196067   PRWG    = 0.5           PRWB    = -0.5
+WR      = 1             WINT    = 0             LINT    = 2.42201E-8
+XL      = -2E-8         XW      = -1E-8         DWG     = -2.790988E-8
+DWB     = 5.977646E-9   VOFF    = -0.1035186    NFACTOR = 1.8044589
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0079869     ETAB    = -0.115204
+DSUB    = 0.940025      PCLM    = 1.9711817     PDIBLC1 = 0
+PDIBLC2 = 0.0195957     PDIBLCB = -1E-3         DROUT   = 5.830459E-4
+PSCBE1  = 2.224265E9    PSCBE2  = 6.4242E-10    PVAG    = 10.2269693
+DELTA   = 0.01          RSH     = 7.6           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 6.52E-10      CGSO    = 6.52E-10      CGBO    = 1E-12
+CJ      = 1.156829E-3   PB      = 0.8604313     MJ      = 0.4161985
+CJSW    = 1.800318E-10  PBSW    = 0.6161205     MJSW    = 0.2735145
+CJSWG   = 4.22E-10      PBSWG   = 0.6161205     MJSWG   = 0.2735145
+CF      = 0             PVTH0   = 1.121114E-3   PRDSW   = 12.2644118
+PK2     = 1.671328E-3   WKETA   = 2.478808E-3   LKETA   = -2.85111E-3
+PU0     = -1.8187729    PUA     = -7.23748E-11  PUB     = 1E-21
+PVSAT   = -50           PETA0   = 1E-4          PKETA   = 2.650105E-3     )
```

Typical values used for calculation at different technology node

		0.35um		0.25um		0.18um		0.13um		
Name	Symbol	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	Units
Chaneel length	L	400 nm	400nm	250 nm	250nm	200 nm	200nm	100nm	100nm	
Supply Voltage	V_{DD}	3.3	3.3	2.5	2.5	1.8	1.8	1.2	1.2	V
Oxide Thickness	t_{ox}	75	75	60	60	35	35	22	22	Å
Oxide Capacitance	C_{ox}	0.5	0.5	0.7	0.7	1	1	1.6	1.6	$\mu F /cm^2$
Threshold Voltage	V_{TO}	0.6	-0.6	0.5	-0.5	0.5	-0.5	0.4	-0.4	V
Body- effect term	γ	0.6	0.6	0.4	0.4	0.3	0.3	0.2	0.2	$V^{1/2}$
Fermi Potential	$2\lvert\emptyset_F\rvert$	0.8	0.8	0.84	0.84	0.84	0.84	0.88	0.88	V
Junction Capacitance Cofficient	C_{jo}	2	2	2	2	1.6	1.6	1.6	1.6	$fF /\mu m^2$
Built-in Junction Potential	$\emptyset_B$	0.8	0.8	0.85	0.85	0.9	0.9	1	1	V
Grading Cofficient	m	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	-
Nominal Mobility (Low vertical field)	μ_0	540	180	540	180	540	180	540	180	$\frac{cm^2}{V-s}$
Effective Mobility (High Vertical field)	μ_e	270	70	270	70	270	70	270	70	$\frac{cm^2}{V-s}$
Critical Field	E_c	6×10^4	24×10^4	6×10^4	24×10^4	6×10^4	24×10^4	6×10^4	24×10^4	V/cm
Critical field x L	E_cL	2.4	9.6	1.5	6	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	12.5	30	12.5	30	$k\Omega/\square$
	v_{sat}	8×10^6	8×10^6	8×10^6	8×10^6	8×10^6	8×10^6	8×10^6	8×10^6	Cm/s

APPENDIX 1

OUT PUT FILE

DC ANALYSIS - temperature=25.0

v(In) = 6.0000e-001

v(Vdd) = 1.8000e+000

v(Vout) = 4.7261e-001

i1(vSource_v_dc_1) = -8.8492e-006

i2(vSource_v_dc_1) = 8.8492e-006

i1(vSource_v_ac_1) = -2.5477e-006

i2(vSource_v_ac_1) = 2.5477e-006

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS - temperature=25.0

	0
	MMOSFET_N_1
MODEL	NMOS
TYPE	NMOS
REGION	Saturation
ID	11.39697u
IBS	0.
IBD	-2.37495a
VGS	600.00000m
VDS	472.61348m
VBS	0.
VTH	421.71753m
VDSAT	162.05617m
BETA	786.23677u
RS	0.
RD	0.
GM	89.28626u
GDS	8.04095u
GMB	13.01286u
GBD	5.02514a
GBS	5.02514a
CDTOT	211.26614f
CGTOT	493.16608a
CSTOT	259.80578f
CBTOT	470.65690f
CGS	313.09868a
CGD	139.06635a
CGB	41.00106a
CBD	211.11912f
CBS	259.47472f

	1	2
	RResistor_1	RResistor_2
R	150.00000K	50.00000K
VDROP	1.32739	-127.38652m
CURRENT	8.84924u	-2.54773u
POWER	11.74637u	324.54652n

APPENDIX 2

OUTPUT FILE

* BEGIN NON-GRAPHICAL DATA

DC ANALYSIS - temperature=25.0

v(In) = 6.0000e-001

v(Vdd) = 1.8000e+000

v(Vout) = 2.9895e-001

i1(vSource_v_dc_1) = -1.0007e-005

i2(vSource_v_dc_1) = 1.0007e-005

i1(vSource_v_ac_1) = -1.2000e-004

i2(vSource_v_ac_1) = 1.2000e-004

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS - temperature=25.0

0

MMOSFET_N_1

MODEL	NMOS
TYPE	NMOS
REGION	Saturation
ID	10.00698u
IBS	0.
IBD	-1.50228a
VGS	600.00000m
VDS	298.95264m
VBS	0.
VTH	430.85719m
VDSAT	156.89348m
BETA	784.29622u
RS	0.
RD	0.
GM	82.81661u
GDS	8.17695u
GMB	12.07090u
GBD	5.02514a
GBS	5.02514a
CDTOT	225.81790f
CGTOT	493.80429a
CSTOT	259.80543f
CBTOT	485.20710f
CGS	312.94156a
CGD	139.86884a

1 2

RResistor_1 RResistor_2

R	150.00000K	5.00000K
VDROP	1.50105	600.00000m
CURRENT	10.00698u	120.00000u
POWER	15.02095u	72.00000u

* VOLTAGE SOURCES

3 4

vSource_v_dc_ vSource_v_ac_

VOLTAGE	1.80000	600.00000m
CURRENT	-10.00698u	-120.00000u
POWER	-18.01257u	-72.00000u

APPENDIX 3

OUTPUT FILE

* BEGIN NON-GRAPHICAL DATA

DC ANALYSIS - temperature=25.0

v(In) = 6.0000e-001

v(N_1) = 1.2000e+000

v(Vout) = 9.7405e-001

i1(vSource_v_dc_1) = -3.7328e-005

i2(vSource_v_dc_1) = 3.7328e-005

i1(vSource_v_ac_1) = -4.3898e-004

i2(vSource_v_ac_1) = 4.3898e-004

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS - temperature=25.0

	0	1	2	3
	MMOSFET_N_1	MMOSFET_N_2	MMOSFET_P_1	MMOSFET_P_2
MODEL	NMOS	NMOS	PMOS	PMOS
TYPE	NMOS	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	460.60568u	15.69941u	-21.62812u	-15.69941u
IBS	0.	0.	0.	0.
IBD	-3.01508a	-4.89473a	3.01508a	1.13544a
VGS	600.00000m	600.00000m	-600.00000m	-600.00000m
VDS	600.00000m	974.04805m	-600.00000m	-225.95195m
VBS	0.	0.	0.	0.
VTH	415.01325m	395.32734m	-280.19192m	-282.83306m
VDSAT	165.82600m	176.79465m	-223.93842m	-222.56041m
BETA	29.17184m	791.66548u	440.88285u	440.80787u
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	3.45940m	104.59952u	112.20568u	77.21838u
GDS	307.03777u	9.16694u	13.06790u	27.08714u
GMB	504.26677u	15.25241u	7.36971u	5.18212u
GBD	5.02514a	5.02514a	5.02514a	5.02514a
GBS	5.02514a	5.02514a	5.02514a	5.02514a
CDTOT	207.44025f	180.95251f	87.94371f	107.97044f
CGTOT	18.23012f	486.30405a	1.57079f	1.58363f
CSTOT	271.74279f	259.80628f	126.50421f	126.51087f
CBTOT	463.84771f	440.35055f	213.20815f	233.17802f
CGS	11.60022f	313.45700a	965.87781a	960.35948a
CGD	5.11199f	131.92323a	432.90179a	451.58312a
CGB	1.51791f	40.92381a	172.01466a	171.69222a
CBD	202.03844f	180.81284f	87.50607f	107.47497f
CBS	259.47472f	259.47472f	125.48410f	125.48410f

* VOLTAGE SOURCES

VOLTAGE	1.20000	600.00000m
CURRENT	-37.32753u	-438.97757u
POWER	-44.79303u	-263.38654u

* BEGIN NON-GRAPHICAL DATA

SMALL-SIGNAL TRANSFER FUNCTION - temperature=25.0

v(Vout) / vSource_v_ac_1 = -5.0151e+000

Input resistance at vSource_v_ac_1 = 2.5696e+002

Output resistance at v(Vout) = 2.7583e+004

* END NON-GRAPHICAL DATA

APPENDIX 4

OUTPUT FILE

* BEGIN NON-GRAPHICAL DATA

DC ANALYSIS - temperature=25.0

v(In) = 6.0000e-001

v(N_1) = 1.2000e+000

v(Vout) = 9.7405e-001

i1(vSource_v_dc_1) = -5.8956e-005

i2(vSource_v_dc_1) = 5.8956e-005

i1(vSource_v_ac_1) = -4.1735e-004

i2(vSource_v_ac_1) = 4.1735e-004

* END NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS - temperature=25.0

	0	1	2	3
	MMOSFET_N_1	MMOSFET_N_2	MMOSFET_P_1	MMOSFET_P_2
MODEL	NMOS	NMOS	PMOS	PMOS
TYPE	NMOS	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	460.60568u	15.69941u	-21.62812u	-15.69941u
IBS	0.	0.	0.	0.
IBD	-3.01508a	-4.89473a	3.01508a	1.13544a
VGS	600.00000m	600.00000m	-600.00000m	-600.00000m
VDS	600.00000m	974.04805m	-600.00000m	-225.95195m
VBS	0.	0.	0.	0.
VTH	415.01325m	395.32734m	-280.19192m	-282.83306m
VDSAT	165.82600m	176.79465m	-223.93842m	-222.56041m

SMALL-SIGNAL TRANSFER FUNCTION - temperature=25.0

v(Vout) / vSource_v_ac_1 = -5.0151e+000

Input resistance at vSource_v_ac_1 = 2.4894e+002

Output resistance at v(Vout) = 2.7583e+004

* END NON-GRAPHICAL DATA

BETA	29.17184m	791.66548u	440.88285u	440.80787u
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	3.45940m	104.59952u	112.20568u	77.21838u
GDS	307.03777u	9.16694u	13.06790u	27.08714u
GMB	504.26677u	15.25241u	7.36971u	5.18212u
GBD	5.02514a	5.02514a	5.02514a	5.02514a
GBS	5.02514a	5.02514a	5.02514a	5.02514a
CDTOT	207.44025f	180.95251f	87.94371f	107.97044f
CGTOT	18.23012f	486.30405a	1.57079f	1.58363f
CSTOT	271.74279f	259.80628f	126.50421f	126.51087f
CBTOT	463.84771f	440.35055f	213.20815f	233.17802f
CGS	11.60022f	313.45700a	965.87781a	960.35948a
CGD	5.11199f	131.92323a	432.90179a	451.58312a
CGB	1.51791f	40.92381a	172.01466a	171.69222a
CBD	202.03844f	180.81284f	87.50607f	107.47497f
CBS	259.47472f	259.47472f	125.48410f	125.48410f

	4
	MMOSFET_P_3
MODEL	PMOS
TYPE	PMOS
REGION	Saturation
ID	-21.62812u
IBS	0.

Profile of the Research Scholar

Sunil Jadav received the B.Tech. degree in Electronics & Communication Engineering from the Guru Jambheshwar University of Science & Technology, Hissar Haryana, India, in 2007 and the M.Tech degree in VLSI Design & Automation from National Institute of Technology, Hamirpur, Himachal Pradesh, India in 2010. In 2011, he joined YMCA University of Science & Technology, Faridabad, Haryana, India (State University), as an Assistant Professor in Electronics Engineering Department. Currently he is also pursuing Ph.D. degree in Electronics Engineering Department of YMCA University of Science & Technology Faridabad. Before joining YMCAUST, he also worked as Assistant Professor in Electronics & Communication Engineering Department of National Institute of Technology, Hamirpur. During his work in N.I.T Hamirpur, he has effectively utilized and worked on various VLSI CAD Tools/Semiconductor Process and on field programmable gate array architecture development and low-power circuit design. He has published more than 28 papers in refereed journals and Conferences. His research interests include analog IC design/CAD with particular emphasis in low-power electronics for portable computing and wireless communications, and High Speed Low power VLSI Interconnect. He is also active member of professional bodies such as: ISTE, IE(India), IAENG and coordinator of Indian Green Building Council (IGBC) student chapter at YMCAUST Faridabad.

LIST OF PUBLICATIONS

List of Published Papers:

1. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**RLC equivalent RC delay model for global VLSI interconnect in current mode signaling**, has been published in International Journal of Modeling & Simulation **(Taylor-Francis)** Vol. 35 Issue 1, 2015. (UGC Approved).
2. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**A Superior Delay Estimation Model for VLSI Interconnect in Current Mode Signaling**, has been published in **World Academy of Science Engineering & Technology (France)** Vol. 9 , No 2, 2015. (UGC Approved)
3. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Carbon Nanotube Based Delay Model For High Speed Energy Efficient on Chip Data Transmission Using: Current Mode Technique**" has been published in International Journal of Electrical & Electronics Engineering by **Wireilla Scientific Publications (New South Wales, Australia)**, Vol. 3 No. 4, 2014.
4. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Current Mode signalling for Global VLSI interconnect:-A Review**" has been published in **YMCAUST Journal of Research**, Vol. 2, Issue 1, Jan 2014.
5. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Close form delay model for on chip signalling with resistive load termination using: Current mode technique**, in (ICIIS), pp. 1-6 Gwalior,India 2014. (IEEE Explore)
6. Sunil Jadav Munish Vashishath Rajeevan Chandel "**Sub-threshold Leakage Reduction of 6T SRAM Cell Using Optimum Bulk Bias**, has been published in National Conference on Recent Development in Electronics, Jan. 2013.
7. Sunil Jadav Munish Vashishath, Rajeeevan Chandel, Vikrant "**Design And Performance Analysis Of Ultra Low Power 6t SRAM Using Adiabatic Technique**" has been published in International Journal of VLSI &Communication Systems, pp 95-105, Vol.3, No. 3, 2012.

List of Paper Accepted for Publication

1. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Estimation of Different Parasitic for Current Mode Receiver System"** has been accepted for publication in **International Journal of Electronics Engineering Research (IJEER).** (UGC Approved Journal)

List of Paper Under Communication:

1. Sunil Jadav, Rajeevan Chandel, Munish vashishath "**Modelling of Overshoot and undershoot for CNT based interconnect for Higher Order of System**" is under Communication in **International Journal of Electronics (Taylor-Francis).**
2. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**A Novel Delay Model for Step Analysis and Bandwidth Estimation of VLSI Interconnects for Current Mode Signalling**" is under communication in **Journal of Communication Technology and Electronics.** (UGC Approved Journal/Springer)