Dec 2018

B.Tech. IV SEMESTER

Digital Electronics (E-208)

Time: 3 Hours | Max. Marks:60

Instructions:
1. *It is compulsory to answer all the questions (2 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART -A

Q1 (a) Write the truth table of AND and OR logic gates. (2)

(b) What are the advantages of digital systems? (2)

(c) What are minterms? (2)

(d) What are the applications of decoders? (2)

(e) Implement the NOT operation using 2×1 multiplexer. (2)

(f) Write the truth table of S-R and J-K flip flop. (2)

(g) Which is the fastest logic family? (2)

(h) What is advantage of CMOS logic family? (2)

(i) Give the specifications of Digital to analog converters. (2)

(j) Which is the fastest analog to digital converter? (2)

PART -B

Q2 (a) Explain the Exces-3 and Gray codes. (5)

(b) Implement the EX-OR and EX-NOR operations using NAND gates only. (5)

Q3 (a) Minimize following function and implement it using minimum number of NAND gates. $F(w,x,y,z)=\sum m(2,3,4,5,6,7,9,11,12,13)$ (5)

(b) Minimize the function $F(a,b,c,d)= \sum m(0,5,7,8,9,10,11,14,15)$ using Quine-McCluskey method. (5)

Q4 (a) Design and implement the full adder using minimum number of gates. (5)

(b) Implement the 8×1 multiplexer using 4×1 multiplexers. (5)

Q5 (a) Design a 3-bit synchronous counter using JK flip-flops. (5)

(b) Draw and explain the circuit of TTL logic family. (5)

Q6 (a) Draw and explain the circuit of successive approximation type analog to digital convertor. (5)

(b) Explain the interfacing of CMOS and TTL logic family. (5)

Q7 Write the short notes on following: (I) FPGA (II) PLA (10)

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