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December, 2019

M.Tech. (ECE) III SEMESTER

Electronic System Design (MECE304)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART - A

1. (a) Compare negative and positive logic. (1.5)

(b) What are the basic methods for the transmission of digital information? (1.5)

(c) Distinguish between digital and analog IC's. (1.5)

(d) Convert 0.7510 to binary using the double-dabbed method. (1.5)

(e) How many cells a n-variable K-map can have? (1.5)

(f) How does realization of a logic function using multiplexer is better than with normal gates? (1.5)

(g) Is it possible to share the product terms between different outputs in a PAL? Justify the answer. (1.5)

(h) What do mean by self starting type counter? (1.5)

(i) How is the state of a memory element specified? (1.5)

(j) Compare state diagram and state table. (1.5)

PART - B

2. (a) Using Quine McCluskey method of tabular reduction method minimize the given combinational single output function $f(W, X, Y, Z) = \Sigma m(0, 1, 5, 7, 8, 10, 14, 15)$. (10)

(b) Two square waves of frequency 1 kHz and 2 kHz are applied as inputs to NAND and NOR gates. Draw the output waveforms in each case. (5)

3. (a) Differentiate between a prime implicant and a non-prime implicant, and an essential prime implicant and a non-essential prime implicant. (5)

(b) Reduce the following function using K Map and identify the prime implicant and essential prime implicant. (10)

4. $A_8A_4A_2A_1$ is a 8421 BCD input to a logic circuit whose output is a 1 when $A_8 = 0$, $A_4 = 0$ and $A_2 = 1$, or when $A_8 = 0$ and $A_4 = 1$. Design the simplest possible logic circuit for the same. (15)

5. (a) Explain the design Steps For Traditional Synchronous Sequential Circuits. (5)

(b) Choose a decoder and use for explaining the design Steps For Next State Decoders. (10)

6. (a) How can we Synchronize Two Systems And Choosing Controller? (5)

(b) What are the parameters for selecting a controller? (5)

(c) Compare CPLD and FPGA. (5)

7. Design and explain the steps involved in case of a sequence detector using Mealy type model. (15)
