Examination Roll No.....

J.C Bose UNIVERSITY OF SCIENCE& TECHNOLOGY, YMCA

B. TECH. 4th SEMESTER

DIGITAL ELECTRONICS (EC232C)

Time: 3 Hours | Max. Marks:75

Note:
1. *It is compulsory to answer the questions of Part -1. Limit your answers within 20-40 word in this part.*
2. *Answer any four questions from Part -2 in detail.*
3. *Different parts of the same question are to be attempted adjacent to each other.*
4. *Assume suitable standard data wherever required, if not given.*

PART -1

Q1 (a) What is race around condition? (1.5)

(b) What is the minimum number of flip flips required to design a Mod-12 ripple counter? (1.5)

(c) Differentiate between ripple and synchronous counter. (1.5)

(d) What are the various types of shift register? (1.5)

(e) What are error correcting codes? (1.5)

(f) What are the various applications of counters? (1.5)

(g) Differentiate between edge triggering and level triggering. (1.5)

(h) What is the difference between SRAM and DRAM? (1.5)

(i) Convert the following: (1.5)

a) $(2A6)_{16}=(?)_{10}$

b) $(1001.101)_2=(?)_{16}$

c) $(221)_{10}=(?)_8$

(j) Why do we use ASCII code? (1.5)

PART -2

Q2 (a) Discuss the working and operation of active pull up type TTL circuit. (8)

(b) Design and implement a Mod-5 synchronous counter using T-Flip Flop (7)

Q3 (a) Implement the following expression using a single 8:1 multiplexer. (7)
$Y(A,B,C,D)=\Sigma m(0,1,2,5,7,8,9,14,15)$

(b) Design and implement a 2-bit comparator using suitable logic gates. (5)

(c) What is the resolution in volts of a 10-bit D/A Converter whose full scale output is 5V ? (3)

Q4 (a) What are different types of shift registers? Explain universal shift register in detail. (5)

(b) Design a binary to Gray Code converter (5)

(c) Convert S-R Flip Flop to J-K Flip Flop (5)

Q5 (a) Design a combinational circuit for a common cathode display BCD to 7 segment code converter. (8)

(b) With a neat circuit diagram explain the operation of a Counter type A/D converter (7)

Q6 (a) Explain the following terms: (5)

i) Figure of merit

ii) Fan out

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iii) Propagation delay
iv) Tristate logic
v) Noise margin

(b) With the help of truth table, Explain the working of J-K Master-slave flip flop. (5)

(c) Discuss the various specifications of a DAC Converter? (5)

Q7 (a) Minimize the expression using K-map and realize using minimum number of gates: (7)

$$F(A,B,C,D) = \Sigma m\ (0,1,2,3,5,7,8,9,11,14)$$

(b) Write a short note on PLA and PAL . Also state the differences. (8)

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