YMCA UNIVERSITY OF SCIENCE & TECHNOLOGY, FARIDABAD

B.TECH EXAMINATION (Under CBS)

ADVANCED COMPUTER ARCHITECTURE (CE-401)

Time: 3 hrs M. Marks: 60

Note: Part-1 is compulsory. Attempt any four questions out of six from part-2.

PART-1

Q. No. 1(a) Differentiate between computer organization and computer architecture.

(b) Why 2's complement addition is used for subtraction?

(c) What are the vertical and horizontal microinstructions?

(d) How system attributes influenced the performance factors?

(e) Define computational granularity and computation latency.

(f) Explain the write-through and write-back polices used in cache memory.

(g) What are the various memory replacement policies?

h) What is a scalar processor?

(i) Draw the pipeline execution of VLIW architecture with degree (m=3)

(j) What is the SIMD and MIMD Flyn's computers classification? [10x2=20]

PART-2

Q. No. 2(a) Write the R/M code to execute the statements A := B + C, where A,B and C ar normalized, short floating point numbers (.F) resident in memory with bas address #D . [3+7=10

(b) Develop the detailed instruction timing for the code in problem 2(a) using we mapped machine.

Q. No. 3(a) Explain the inclusion, coherence and locality of reference property associate with memory hierarchy design. [5]

(b) What are multiprocessors and multicomputer? Explain in details [5

Q. No.4(a)A wafer has diameter of 21 cm and costs $5,000 for a particular production run. Compute the cost per die for die area = 2.3 sq.cm and for 1 sq.cm if ρD =1 defect/sq.cm. [5]

(b) What is grain scheduling? Compare control versus data flow mechanisms. [5]

Q. No.5(a) Explain the Hellerman's and streckers's models associated with processor-memory interaction. [5]

(b) A 40-MHz processor was used to execute a benchmark program with following instruction mix and clock cycle count:

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control Transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program. [5]

Q. No. 6(a) Perform a data dependence analysis on each of the following program fragments. Show the dependence graphs among the statements with justification. [5]

P1: C=D * E; P2: M=G+C;

P3: A=B+C; P4: C=L+M; P5: F=G/E

(b) Explain and compare the architecture of RISC and CISC processors.

Q. No. 7(a) Consider a cache consisting of 256 blocks of 16 words each, for a total of 4. words, and assume that the main memory is addressable by a 16 bit address and it consists of 4k blocks. How many bits are there in each of the TAG, BLOCK/SET and WORD fields for different mapping techniques [5]

(b) Write in brief about. [5]

(i) Vector processors (ii) Symbolic processors