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Roll No. .... Total Pages : 3

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Mar. 2022

B.Tech. (EIOT) - III SEMESTER

Digital Electronics (EEN-301)

Time : 90 Minutes] [Max. Marks : 25

Instructions :

1. *It is compulsory to answer all the questions (1 mark each) of Part-A in short.*
2. *Answer any three questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART-A

1. (a) Implement the NOR gate using the NAND gate only. (1)

(b) What is a demultiplexer? (1)

(c) Convert $(111.10)_2$ into equivalent Hexadecimal code. (1)

(d) Find $(125)_8 / (25)_{10} = (.......)_{10}$. (1)

(e) Differentiate between 'T' and 'D' Flip-flop. (1)

(f) What are asynchronous counters? (1)

(g) What do you mean by quantization for A/D converters? (1)

(h) What is the purpose of using PLD? (1)

(i) Write the truth table of Full adder. (1)

(j) How Ring counter is different from Jhonson counter? (1)

PART-B

2. Minimize the following function using Quine Mclusky method
$f(A, B, C, D) = \Sigma m(0, 2, 5, 11, 13) + \Sigma d(1, 6, 14)$. (5)

3. (a) What is the error detection and correction codes? How these are helpful in error detection and correction explain with the help of an example. (3)

(b) Differentiate between serial carry and carry look-ahead adders with suitable diagrams. (2)

4. Design a Mod-10 counter using flip-flops. (5)

5. (a) Perform the following :

(i) $(12.5)_{10} \rightarrow (\quad)_{16}$.

(ii) $(87.16)_{8} \rightarrow (\quad)_{2}$.

(iii) $(101110)_{2} \rightarrow (\quad)_{\text{Gray code}}$. (3)

(b) Implement half adder using 4:1 multiplexer. (2)

6. (a) Define resolution, sensitivity and accuracy of A/D converter. (3)

(b) Differentiate between PLA and PAL. (2)