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B.Tech. (EL) VIth Semester Examination
DIGITAL SYSTEM DESIGN
(E-302)

Time : 3 Hours] [Max. Marks : 60

Instructions :

(i) Part-A is compulsory and attempt four Questions from Part-B.

(ii) Assume relevant data/figure if found missing.

PART–A

1. (a) What are the capabilities of VHDL? Explain the role of VHDL in simulation and synthesis. (2)

(b) Differentiate between concurrent and sequential statement. (2)

(c) What are predefined Attribute? (2)

(d) What is package declaration? Explain. (2)

(e) Compare the array data type and record data type in VHDL. (2)

(f) What are data objects? Explain. (2)

(g) Explain the case statement with an example. (2)

(h) Discuss the inertial delay and transport delay in VHDL. (2)

(i) What is subprogram overloading? Discuss. (2)

(j) Write a VHDL code for 3 to 8 decoder. (2)

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PART–B

2. (a) Explain the three different styles of modelling used in VHDL. (5)

(b) Define and discuss with suitable examples operator overloading in VHDL. (5)

3. (a) Write a VHDL code for full adder and 4 : 1 Multiplexer. (5)

(b) Write a VHDL code for BCD to seven segment decoder in behaviour model. (5)

4. (a) Write a VHDL code for 4 bit serial in serial out register using the data flow model. (5)

(b) What is process statement? Write a VHDL code using the process statement. (5)

5. (a) What is generic statement? Why generic is used? Discuss with writing a VHDL code using generic. (5)

(b) What are different operators used in VHDL? Discus with giving the examples. (5)

6. (a) Explain the component declaration and component instantiation in structural modelling with examples. (5)

(b) Design a BCD to excess-3 code converter using the PLA. (5)

7. Write short note on the following :

(a) ROM. (5)

(b) FPGA. (5)
