ANALYTICAL STUDY OF MOS DEVICE FOR LEAKAGE REDUCTION IN LOW POWER CIRCUIT

THESIS

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DECLARATION

I hereby declare that this thesis entitled **"ANALYTICAL STUDY OF MOS DEVICE FOR LEAKAGE REDUCTION IN LOW POWER CIRCUIT"** by **PRASHANT KUMAR** being submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under **FACULTY OF ENGINEERING & TECHNOLOGY**, is a bonafide record of my original work carried out under joint guidance and supervision of **DR.MUNISH VASHISHATH, PROFESSOR (ELECTRONICS ENGINEERING), J. C. BOSE UNIVERSITY OF SCIENCE & TECHNOLOGY, YMCA, FARIDABAD** and **DR. P. K. BANSAL, FORMER PRINCIPAL, MIMIT MALOUT, PUNJAB** and has not been presented elsewhere.

I further declare that the thesis does not contain any part of any work which has been submitted for the award of any degree, either in this university or in any other university.

(Prashant Kumar)

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CERTIFICATE

This is to certify that the thesis entitled, **"ANALYTICAL STUDY OF MOS DEVICE FOR LEAKAGE REDUCTION IN LOW POWER CIRCUIT"** by **PRASHANT KUMAR**, being submitted in fulfillment of the requirement for the Degree of Doctor of Philosophy in **ELECTRONICS ENGINEERING** under Faculty of Engineering & Technology, J. C. Bose University of Science & Technology, YMCA, Faridabad, during the academic year 2021-22, is a bonafide record of work carried out under our joint guidance and supervision.

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ABSTRACT

The transistor is the elementary unit of all the electronic systems. The advancements in the performance of these systems have changed the world. In the recent years, the development of small, computationally efficient and portable system is mainly due to the miniaturization of semiconductor devices which, in turn, are heavily dependent on the improvement in the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) technology. The invention of MOSFET gave the quantum leap to the semiconductor components. In order to upgrade, this device has to be regularly scaled to small dimensions. The enhanced speed of operation, less size and lower power consumptions from predecessor are two other key parameters for next-generation semiconductor devices. With continuous scaling, the dimension of MOSFET has reached into nano-meter regime.

The performances of a scaled MOSFET degrade considerably due to the unpredictable electrical behaviour which is known as Short Channel Effects (SCEs). These effects arise mainly due to weakened control of gate over the channel. The Short Channel Effects leads to increase sub-threshold leakage current which affects the device characteristics. These short channel effects have become obstacle for further scaling of the devices while maintaining a good performance. Hence, it is required to improve the MOSFET technology by identifying the innovative approach to meet the expected performance with the upcoming scaling. It is very challenging to get the acceptable gate control over the channel with the planar MOSFET structures. Many novel device structures have been presented in literature to address the challenge of Short Channel Effects (SCEs). The Silicon-on-Insulator (SOI) technology has been utilized as the CMOS technology in the last decade due to the advantages of speed, packing density, excellent resistance to radiation and most importantly the immunity to Short Channel Effects. In addition to the effective suppression of short channel effects, SOI MOSFET gives excellent current drive capability and these structures are compatible with conventional CMOS processes. SOI device composed of a buried oxide layer on which a silicon layer is deposited in which source and drain are formed. SOI structure is dielectrically isolated to each other and from substrate layer. A higher packing density can be achieved in SOI devices due to inbuilt isolation from neighbouring transistors in SOI devices. The

presence of buried oxide layer makes SOI free from the latch-up phenomenon. Hence for predefined power consumption, a highly dense and faster circuit can be fabricated using SOI devices process.

The continued investigation for an alternative MOSFET to have better electrical characteristics led to the introduction of new materials and concepts to overcome the Short Channel Effects (SCEs). The usage of high-k materials as gate dielectric provides the advantages of reduced parasitic capacitances and low off current. HfO_2 as high-k material was used for analysis in the present work due to its better properties compared to other high-k materials. Due to the advantages offered by high-k materials, HfO_2 is used as dielectric materials for every MOSFET structure reported in the present research work by replacing/stacking with SiO_2.

The planner MOSFET structures having single gate at very small dimension are incapable to have good control of gate over the channel. Hence the multi-gate approach is good option for further scaling of the planner MOSFET. The design of such multi-gate structure may be complex but enhance the performance of the device by reducing the Short Channel Effects. The multi-gate structure including Double Gate, Triple Gate and Cylindrical Gate All Around Structures provide better control of channel and suppression of Short Channel Effects. Among all of these Cylindrical Gate All Around MOSFET structure offers the best performance. In this structure, the channel is completely surrounded by the gate. This structure provides better gate control and enhances the current driving capability of the device.

With MOSFET device technology reaching under 10nm, the formation of ultra-thin junction requires costly and sophisticated fabrication process. Hence, a device where junction and individual source/drain regions formation is not required will prove to be a better solution to the complex problem of scaling and fabrication. The device which has the same material from source to drain is called Junctionless Field Effect Transistor (JLFET). The operation of the device depends upon the work function difference between the gate metal and silicon. The device has CMOS functionality with the attributes of no junction. The JLFET was found to have less leakage current than conventional MOSFET structures. This device has same type and concentration of doping throughout the device active region. The device shows efficient results in suppressing the short channel effects. In the present research work the analytical

modeling of the JLFET has been carried out by solving the Poisson's Equation using Parabolic Approximation Technique. This analytical model is verified with the simulation results obtained from the Device Simulator Atlas from Silvaco.

The dual-material/triple material gates on MOSFET structure offers an alternative way of simultaneous short channel effects suppression and improved device performance by careful control of the material work-function.

The present work includes a superior device in which all the device improvement approaches like Gate Engineering, Channel Engineering, Gate Work-Function Engineering and Device Engineering have been applied. The "Stacked Dielectric Triple Material Cylindrical Gate All Around Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET)" structure have been presented on the basis of above device improvement approaches. The stacked dielectric structure minimizes the gate leakage and improves the carrier transportation efficiency in the channel. Triple materials gate composed of metal gates made up of three different metals having different work-function which results in the suppression of short channel effects. The Cylindrical Gate All Around structure provides very good gate control over the channel. The JLFET offers a simple structure which again provides better short channel effects immunity and negligible off current. The SD-TM-CGAA-JLFET structure was simulated and analytically modelled for the sub-threshold current which is the prime objective of this research work.

The suitability of SD-TM-CGAA-JLFET for circuit applications is analyzed with the help of the CMOS inverter circuit and various characteristics of the inverter were analysed. The excellent agreement is found between the analytical and simulated results. The static power dissipation of CMOS inverter with SD-TM-CGAA-JLFET structure as NMOS and PMOS was found to be 5 times less than the static power of CMOS inverter designed using SOI-based Double gate Junctionless transistor of comparable dimension. From the analysis, it is found that SD-TM-CGAA-JLFET device will be a better alternative for the nanoscale MOSFET device.

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μ	Mobility
C_{oxide}	Oxide capacitance
E	Electric Field
E_g	Energy Band gap
g_m	Transconductance
g_m/I_d	Transconductance to Drain Current Ratio
I_{sub}	Sub-threshold Current
I_{ds}	Drain to Source Current
$J_C(r,z)$	Total Current Density
K	Boltzmann Constant
L	Channel Length
M_1, M_2, M_3	Gate Materials
N_a	Acceptor Concentration
$N_C(r,z)$	Carrier Concentration
N_d	Donor Concentration
n_i	Intrinsic Carrier Concentration
ϕ_{fp}	Fermi Potential
Ψ_S	Surface Potential
Ψ_{OXIDE}	Potential drop across the gate oxide
Ψ_0	Center Potential
ϕ_{M1}	Work Function for Metal 1
ϕ_{M2}	Work Function for Metal 2
ϕ_{M3}	Work Function for Metal 3
Ψ_{min}	Minimum Surface Potential
q	Electronic Charge
T	Temperature
t_{HfO2}	Thickness of Hafnium Oxide
t_{SiO2}	Thickness of Silicon Oxide
t_{oxide}	Thickness of Oxide Layer
t_{si}	Silicon Film thickness
V_{bi}	Built in Potential
V_{ds}	Drain-Source Voltage
V_f	Flat-band Voltage

V_{gs}	Gate-Source Voltage
V_{th}	Threshold Voltage
ε_{SiO2}	Permittivity of Silicon Oxide
L_1	Channel Length under metal M_1
L_2	Channel Length under metal M_2
L_3	Channel Length under metal M_3
V_{th}	Threshold Voltage
V_{DD}	Positive Supply Voltage
$Pdynamic$	Dynamic Power Dissipation
fck	Clock Frequency
PSC	Short Circuit Power Dissipation
k	Dielectric Constant
2D	Two Dimensional
I_{on}	On-current
I_{off}	Off-current
Vt_{sat}	Saturation Threshold Voltage
Vt_{lin}	Linear Threshold Voltage
SS	Sub-threshold Slope

CHAPTER-I

INTRODUCTION

1.1 PREAMBLE

The discovery of the transistor and subsequently the monolithic integrated circuit (IC) has created a revolution in the field of the electronics industry. Semiconductor technology has grown at a very fast pace in the last 70 years. The first semiconductor transistor was invented in 1947 at Bell Laboratory by W. Shockley, J. Bardeen and W. Brattain [1]. It completely replaced the vacuums tubes from the entire electronics product. After the invention of the transistor, there is no looking back for the semiconductor electronics industry. The circuits where semiconductors devices are applied range from a very simple system to a very complex system having constraints of power, area, etc. The electronics industries have come up in the past to design and create semiconductor device-based circuits as small as basic gates and as complex as processors. The advancement in the fabrication technology with every generation of semiconductor devices, are producing smaller, faster as well as low-power integrated chips. This ultra-small design of integrated circuits requires advanced fabrication technology and capable fabrication equipment. With the advancements in computer technology for automated tools, a better understanding of electronics system design and applications software along with this improved process technology makes it possible to integrate billions of transistors on a single semiconductor wafer with device dimensions below 10 nanometres recently [2].

Moore's law states that the transistors in integrated circuits will get doubled every 18 months [3]. Continuous reduction in feature size has established the increase in device density on IC as per Moore's law for almost half-decade. The density improvement not only results in a reduction in the system design area but also improves processing speed and memory capacity in an exponential manner [3]. However, in deep sub-micron technologies, it enhances the sub-threshold current which causes more power consumption and subsequently reduced battery life. The continuous process of downscaling the semiconductor device dimensions is the main stimulant for the growth of integrated circuits and advancement in allied technology like robotics,

information communication technology, biotechnology, sensors, etc with superior performance and small size at a much-reduced cost.

The bipolar technology which was introduced in 1947 [4] was initially used for integrated circuits. Due to high power dissipation and limited level of integration over an IC, causes the semiconductor industry has to look for alternate semiconductor devices. Metal Oxide Field Effect Transistor (MOSFET) was initially conceptualized in the 1930s, but the first working MOSFET device was created in the 1960s [4]. The unique properties of MOSFETs make them a significant partner in the evolutionary progress of the semiconductor industry. The field of microelectronics today is dominated by MOSFET. The MOSFET or MOS transistor is the most commonly used semiconductor electronic device in the present era. In 1963 [4], with the advent of low power design technique, CMOS (Complementary MOS) where both NMOS and PMOS were fabricated on the same semiconductor substrate, the era of semiconductor technology changed forever. CMOS devices have better features, viz. high noise immunity, negligible standby power dissipation, significantly higher packing density, relatively faster circuit speed, lower energy wastage compared to NMOS and TTL (Transistor-Transistor Logic) [5].

As the number of semiconductor devices on integrated circuits increases, the size of each transistor and power supply is decreased or scaled. This scaling results in a decrease in power consumption, higher current drive and faster circuits leading to improved performance [5]. However, the scaling of MOSFET dimensions not only reduces the separation between the drain and source electrode but also decreases the control of the gate electrode. This reduction of the control of the gate electrode results in some undesirable effects called Short Channel Effects (SCEs). These effects include an adjustment in threshold voltage (V_{th}), reduced subthreshold swing, lowering of the potential barrier and increased leakage current [6]. These effects also cause large power dissipation and reduction in the device performance.

With the steady improvement in device fabrication technology, MOSFET in the recent past has reached its scaling limit. The requirements to further scale these MOSFETs have introduced several inventive techniques composing of the use of new channel materials, new device structures and new gate oxide materials. The proposed materials by various researchers [4-6], devices and technology include the usage of

High-k materials, Silicon over Insulator (SOI), Dual/double/multi-gate device structures, Gate all-around devices (GAA) and recently Junctionless MOSFETs [7] among many others. The Junctionless MOSFETs promised to have better-scaling properties as compared to the multiple-gate MOSFETs.

1.2. MOSFETS

Advanced integrated circuits with reduced feature sizes are created every coming year. These semiconductor devices are not only cost-effective but also more reliable than their predecessor. The semiconductor industrial advancement in the past mainly depends on the success of integrated circuits made up of silicon-based devices known as Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This semiconductor device is utilized as a switch as well as an amplifier.

MOSFET is a four-terminal device. A large number of MOSFETs and their interconnection can be created on the surface of the single integrated circuit due to the planner nature of this device. The integration of MOSFETs in Integrated Circuits (ICs) have been implemented through many generations of integration like MSI (Medium Scale Integration) includes 100-1000 transistors on an IC, LSI (Large Scale Integration) having 10^3-10^4 transistors on an IC, VLSI (Very Large Scale Integration) having more than 10^5 transistors on an IC and ULSI (Ultra Large Scale Integration) where more than one million transistors are mounted on an IC [5].

MOSFET was designed with the idea of an insulated gate i.e. the gate leakage current should be minimum. MOSFET was created with the insulated gate so that no leakage current flows to or from the gate. In silicon MOSFETs, reliable and high-quality insulators can be grown easily in the form of Silicon Dioxide (SiO_2). SiO_2 acts as an insulator that makes firm bonding with the silicon substrate. The SiO_2 not only works as an insulator in the MOSFET but also facilitates selective diffusion and pattern transfer during the fabrication of the device. Due to these benefits, silicon-based technology prevailed for MOSFET [8].

MOSFET is a unipolar device that controls the drain current by applying gate voltage. During MOSFET operation, the gate voltage is applied to create the channel that facilitates the charge carriers to flow from source to drain. Over the years many new

concepts for semiconductor materials have been applied in MOSFETs for various applications but the high-quality oxide formation still makes the Silicon-based MOSFETs the preferred choice.

Enhancement type MOSFETs and Depletion type MOSFETs technology exist in MOSFETs. MOSFETs based on the charge carrier which participates in the charge conduction process are classified as N-channel MOSFET (nMOS) and P-channel MOSFET (pMOS). MOSFET consists of the drain, source, gate and substrate electrode. The source is normally connected to the substrate of MOSFET.

1.2.1 Construction of the MOSFET

Figure 1.1 depicts the construction of the enhancement type n-channel MOSFET. The substrate of the MOSFET is made with the lightly doped p-type semiconductor material. The two heavily n-doped regions are created to form source and drain regions having metallic contacts. Isolation between the gate electrode and channel (the region between source and drain) is created using Silicon dioxide (SiO_2). The conductivity of the channel is modulated by gate bias.

The enhancement type and depletion type MOSFETs are the same from a construction point of view. However, a prefabricated channel exists in depletion type MOSFET.

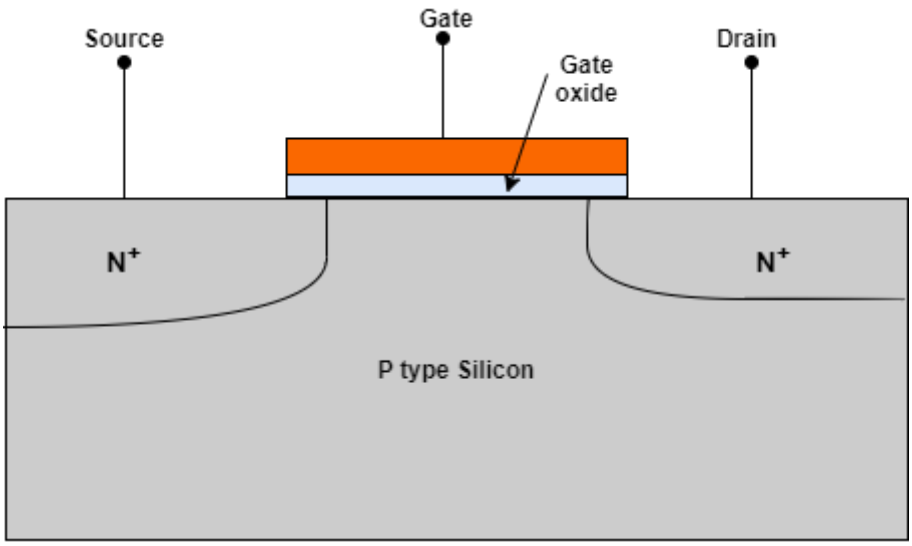

Figure 1.1 Basic construction of n-channel MOSFET

The nMOS have charge carriers as electrons in the channel and the pMOS have charge carrier holes in the channel.

1.2.2 MOSFET Operation

In MOSFET, when the appropriate voltage is applied at the gate terminal, a conducting channel is created which connects the drain and source using the minority charge carriers of the substrate.

In the absence of voltage on the gate terminal, the minority charge carriers are not able to accumulate under the gate region and the formation of the channel or the conducting path between the source and drain region does not take place which results in absence of drain current. When the positive voltage (in the case of nMOS), which is more than the threshold voltage is applied at the gate terminal, the electrons under the gate region start to accumulate under the gate region and a conducting channel gets created between the source and drain. The applied positive voltage on the gate terminal attracts the minority charge carriers (for substrate) i.e. electrons to form the n-type channel and also repels the majority charge carriers i.e. holes of the p-type substrate to deep inside the substrate.

When the appropriate voltage between source and drain is applied the drain current starts to flow in between the source and drain through this channel. When the voltage at the gate terminal is enhanced, more electrons get accumulated under the gate and holes move deeper inside the substrate, which results in the creation of a strong channel between source and drain. The strong channel is capable of conducting a large amount of drain current between drain and source. The device in which this process of gate voltage to create or to enhance the channel occurs is known as enhancement type MOSFET. The flow of the drain current can be controlled by the applied voltage at the gate terminal. Depending upon the applied voltage over the different terminals of MOSFET, the operation of MOSFET can be classified into three modes:

1.2.2.1 Cut-off mode

When the gate to source voltage (V_{gs}) is below the threshold voltage (V_{th}) (minimum voltage required for turning on the MOSFET), the MOS device is said to be operating in the cut-off region. Hence when $V_{gs} < V_{th}$, no current flows between the source and drain through the channel. The MOSFET in cut-off mode is shown in Figure 1.2

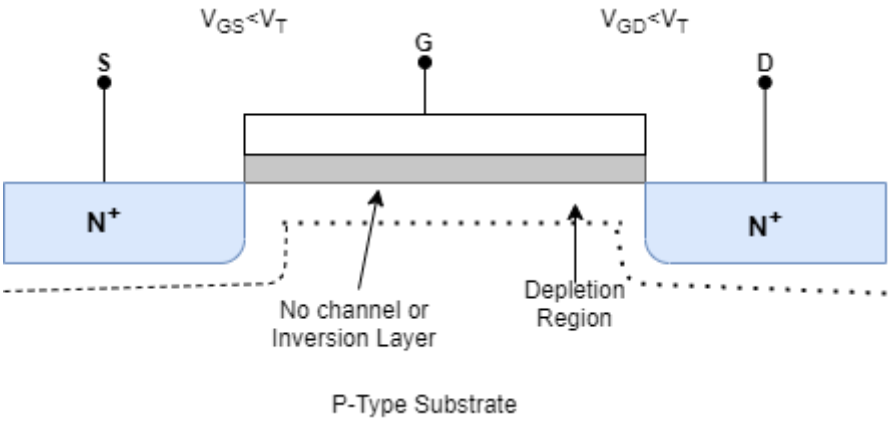

Figure 1.2: MOSFET cut-off mode operation [9].

1.2.2.2 Triode region or linear mode

When $V_{gs} > V_{th}$, $V_{gd} > V_{th}$, with $V_{ds} > 0$, the MOS device is said to operate in triode or linear mode. In this mode, the voltage applied at the gate terminal is more than the threshold voltage, but the drain to source voltage is less than the difference of gate to source voltage and threshold voltage (drain gate to drain voltage is less than threshold voltage)

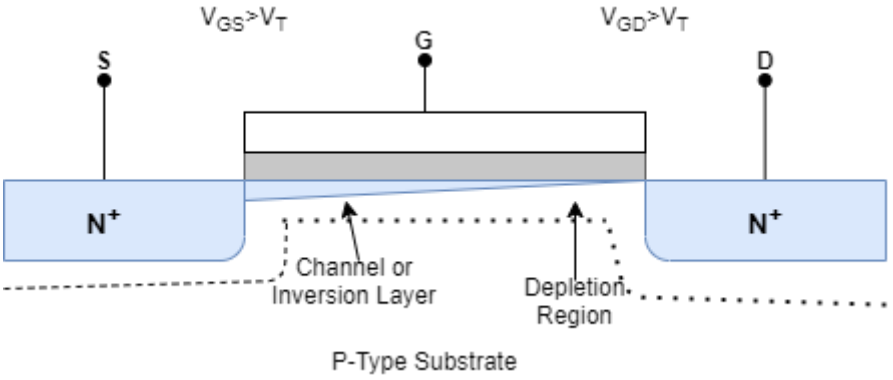

Figure 1.3: MOSFET linear mode operation [9].

This mode as shown in Figure 1.3 is also known as a linear or ohmic mode. In this mode, the drain current varies linearly with gate voltage and MOSFET behaves like a resistor in this mode.

1.2.2.3 Saturation mode

When $V_{gs} > V_{th}$, $V_{gd} < V_{th}$ ($V_{ds} > 0$), the MOS device is said to operate in saturation mode. In this mode, the gate to source voltage is higher in comparison to the threshold voltage and drain to source voltage is also greater than the gate to source and threshold voltage difference (or gate to drain is less than threshold voltage). The formation of a channel in saturation mode is maximum. Hence, a large current flows through the channel between the source and drain. In this mode, the drain current is almost constant and independent of drain voltage but only depends upon gate voltage.

The linear mode operation of the MOS device is useful for digital circuits and saturation mode is useful for analog circuits [9].

1.2.3 Distinguished Features of MOSFET

The distinguishing features of MOSFET with respect to other semiconductor devices are

1. Surface conduction.

2. Symmetrical doping in source and drain regions.

3. Channel barrier height controlled by the insulated gate.

4. Gate current is zero

5. Two physical mechanisms for current: Diffusion (in weak inversion mode / subthreshold conduction mode) and Drift (dominates in strong inversion)

6. Negligible second breakdown voltage [5].

1.3 ITRS ROADMAP FOR SEMICONDUCTORS

International Technology Roadmap for semiconductors or ITRS [10] was conceptualized by various experts of the semiconductors field to specify the device design parameters for the future generation semiconductor devices. It also predicts the challenges that the device scaling industry might face with the future generation of devices. ITRS specifies the parameters by keeping high performance and power consumption issues in focus. Since the digital and memory-based IC production is a major portion of the semiconductor industries so the consideration for ITRS was always low power, high-speed performance and area requirements for the future generation of devices.

The approaches for attaining these targets are quite different i.e. the high-speed performance usually result in high off current or increased power consumption, low power approach maintain longer operating status of portable devices by the mean of reducing switching activities or the operating speed.

The ITRS ensures that research and development be continued in this area to maintain the historical scaling for future projections. ITRS is not updated from 2017 and International Roadmap for Devices and Systems (IRDS) [2] had replaced it to make predictions about the future development in the field of electronics systems and semiconductor devices.

1.4 TECHNOLOGY TRENDS IN POWER DISSIPATION

In the recent past, most of the research in the semiconductors field is devoted to reducing the power dissipation of circuits. The omnipresent portable electronic devices have limited battery life but they require a longer operational lifetime. The semiconductor IC manufacturers are looking for new technologies and new circuit approaches to improve power performance without compromising on speed, area and reliability. In non-portables electronics systems too, the reduction of power consumption is an important concern due to the cost involved in cooling mechanism and system reliability. In order to obtain the high performance of the system, the low power operation is a major challenge in modern semiconductor integrated circuits. Many approaches like sub-threshold logic circuits where the semiconductor devices

are driven at the power supply voltage below threshold voltage are used. Here low power consumption is obtained at the cost of the performance of the circuit. In sub-threshold circuits, the speed of operation reduces due to the increase in delay. The current is having an exponential dependency on gate voltage, temperature and threshold voltage in the sub-threshold region. However, the current has a linear dependence on the W/L (width to length of the device) ratio. Hence, the device size has much less effect on the device current than it would have been in the strong operating region [11]. The sub-threshold region's operation of the device results in an improvement in the characteristics like Voltage Transfer Characteristics (VTC) and noise margin.

It can be easily predicted that in the absence of low-powered operations, the portable devices either have a very short operation lifetime or require very heavy battery space. The cost of the system does increase in the absence of low power operations due to advanced packaging and cooling mechanism. The reliability issues are also faced in the non-low power systems as these systems dissipate power in terms of heat and this heat raises the temperature of the system. The high temperature tends to increase the possibility of silicon failure mechanism.

1.5 POWER DISSIPATION IN CMOS CIRCUITS

CMOS circuits design approach composed of both pMOS and nMOS on the same silicon wafer which is generally a preferred low power choice for the systems. However, the major sources of power dissipation can be classified into three categories for CMOS circuits: Dynamic Power Dissipation, Short Circuit Power Dissipation and Static Leakage Power Dissipation.

In the initial stages of IC's era, dynamic power consumption was dominant and the remaining two power consumptions were almost negligible. The advent of short channel devices has caused the static leakages power to become the major component of power dissipation along with the other two mechanisms also playing a significant part [9]. A brief overview of different components of power dissipation in circuits is as under

1.5.1 Dynamic Power Dissipation

When the transistor switches from one logic to another logic, the power is required for the charging and discharging of load capacitances. This power consumption is termed dynamic power dissipation. The dynamic power dissipation for a CMOS inverter may be understood by assuming a CMOS inverter having load capacitance as C and having supply voltage as V_{DD}. Considering one cycle which involves rising and falling transition of the output, the charge Q= C*V_{DD} is consumed for low to high transition. The same charge is passed to the ground in the high to low transition of the output. By assuming the frequency of the input signal as f_S, and the time period for the operation as T, the dynamic power is given by the equation 1.1:

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt \qquad (1.1)$$

Solving equation (1.1), we get

$$P_{dynamic} = CV_{DD}^2 f_s \qquad (1.2)$$

The equation (1.2) can also be written as

$$P_{dynamic} = \alpha\, CV_{DD}^2 f_{ck} \qquad (1.3)$$

Where α is the activity factor for the node transition and f_{ck} is clock frequency.

1.5.2 Short Circuit Power Dissipation

During the switching of the CMOS transistor circuit, a momentary phase is reached when both the transistors, viz. NMOS and PMOS turn on and a short circuit path for the current exists between the high and low power supply. This results in the glitch of short circuit current. Considering I_m as the average short circuit current, the short circuit power dissipation is specified by equation (1.4).

$$P_{SC} = I_m * V_{DD} \qquad (1.4)$$

The value of I_m for the symmetrical CMOS inverter is given by equation (1.5) as [8]

$$I_m = \frac{\beta}{12} (V_{DD} - 2V_{th})^3 \frac{t_{rf}}{t_p} \quad (1.5)$$

Here V_{th} is the threshold voltage of both the MOSFETs, β is the current gain of MOSFET, t_{rf} is the rising and falling time period of the input signal and t_p as the pulse time period.

1.5.3 Static Leakage Power Dissipation

It is the power dissipation by the leakage current components present in the device when the transistor is in the off state. Considering n transistors in the circuits each having I_{off} as the off-state leakage current. The total static leakage power of the circuit is given by equation 1.6.

$$P_{static} = V_{DD} \sum_{i=1}^{n} I_{off_i} \quad (1.6)$$

1.5.3.1 Static Leakage Current

Figure 1.4 depicts the various leakage current components which are present in MOS devices.

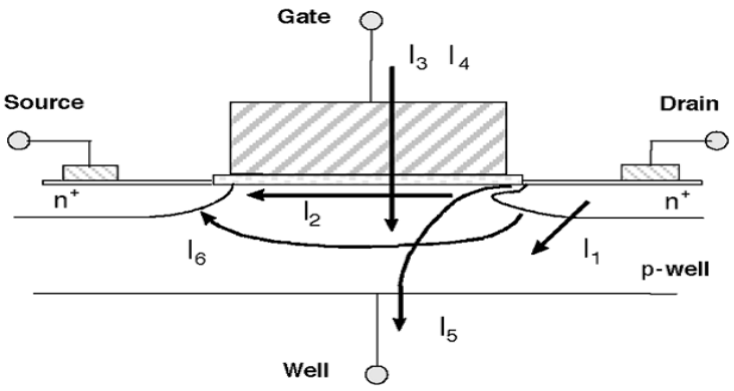

Figure 1.4: MOS device leakage currents [12]

I_1 represents the leakage current in a reverse-biased p-n junction

I_2 represents the subthreshold leakage current

I_3 represents the gate-oxide leakage current

I_4 represents the hot-carrier injection current

I_5 signifies the Gate Induced Drain Leakage (GIDL) current

I_6 signifies the punch-through current.

The off-state leakage currents are mainly contributed by I_2, I_5 and I_6, whereas I_1 and I_3 take place in both OFF and ON states [12].

i) Reverse biased p-n junction Current (I_1)

The diode which is present between source/drain to the substrate will be normally reverse-biased which causes reverse current I_1. This current I_1 can be attributed to the drift/diffusion of minority carriers near the depletion region edge and the electron-hole pair generation in the depletion region.

ii) Sub-threshold Leakage Current (I_2)

When the gate voltage is below V_{th} then the MOS device should be in an off state ideally. However, a small amount of current that flows between the source and drain, and is known as Sub-threshold Leakage Current **(I_2).** This state of the MOS device is also called a weak inversion. In this state, the concentration of minority carriers is negligible and a whole voltage drop is observed across the reverse-biased junction. This results in a very little change in the electrostatic potential at the surface of the semiconductor towards the channel which produces a very small electric field. The drift current component is very small due to the mitigation of mobile carriers and the longitudinal electric field [12]. The sub-threshold current is contributed mainly by the diffusion mechanism.

iii) Tunneling Gate Oxide Leakage Current (I_3)

The continuous scaling of gate oxide causes enhancement in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from the substrate to the gate and also from gate to substrate through the oxide layer. The tunneling involves Fowler–Nordheim (FN) tunneling and direct tunneling [13].

iv) Hot Carriers Injection Current (I_4)

The electric field is high near the Silicon–Silicon oxide interface (Si-SiO_2). Due to this the electrons or holes have enough energy to jump the interface and penetrate the oxide layer. This phenomenon is called hot-carrier injection. The holes injection from Si to SiO_2 is less prone than electrons [8] because the holes have higher effective mass.

v) Gate Induced Drain Leakage current (I_5)

The Gate Induced Drain Leakage (GIDL) occurs when the drain is subjected to higher voltages by keeping the gate at ground potential. This results in the creation of a depletion region under the overlap of drain and gate. The tunneling of the electrons from the valence band to the conduction band creates the electron-hole pair in the region. These pairs are collected by substrate and drain. The band to band tunneling under the overlapped drain and gate region causes the GIDL current (I_5). The GIDL current is directly proportional to drain voltage and inversely proportional to gate voltage [7].

vi) Punch through current (I_6)

The nearness of drain and source terminal of MOSFET in short channel devices cause the extension of the depletion region into the channel. The distance between the depletion region boundaries reduces with a reduction in channel length at constant doping. With the rise in V_{ds}, reverse bias across the junctions increases and it pushes the junctions further near to each other. With the significant increase in V_{ds}, merging of these two depletion regions occurs and this is known as punch-through. Due to punch through current, the performance of small size MOS transistors heavily depends upon drain bias. The other effect which is very similar to the punch-through is Drain-Induced Barrier Lowering (DIBL) [7].

1.6 DESIGNING FOR LOW POWER

The semiconductor technology has to be scaled down to meet the challenges of future circuits to improve the performance of the system and to reduce the cost of the system. The scaled circuits will have a denser packing of transistors working at high

frequency. This approach will usually result in more power dissipation. The factors like supply voltage V_{DD} hence are to be scaled in the same proportion to reduce power dissipation. This supply voltage scaling will impact the working of the transistor if the threshold voltage of the device is not scaled in the same proportion to maintain the appropriate gate current drive [6]. The factors like size of the transistor, supply voltage, threshold voltage, etc. have an enormous impact on the power dissipation.

1.7 POWER MINIMIZATION TECHNIQUES

Recently the semiconductor industry has adopted many approaches for facing the challenges of power reduction. Some of these approaches are as:

1.7.1 Supply Voltage Scaling

It is the most effective approach for the reduction of power dissipation. With every new generation of scaling, the IC fabrication processing mechanism has to be revamped. This power reduction approach often requires detailed consideration of issues like the signal-to-noise ratio and supported circuit integration for low voltage operation.

1.7.2 Reduction of Capacitance

The capacitance also plays a vital role in the power dissipation of the circuits. The capacitance can be reduced by using the latest design process approaches to make transistors with techniques like SOI (Silicon on Insulator). The implementation of these processes requires a compatible fabrication facility and time to research & development for the upcoming concerns.

1.7.3 Better Design Techniques Employment

This approach consists of research in the design perspective of the circuits for the reduction of power dissipation. A better arrangement of the various component of the circuit will result in a significant reduction of power dissipation.

1.7.4 Better Power Management Approaches

A better power management approach combining various approaches like device scaling, supply voltage scaling and a better choice of circuit architecture can provide the best solution for the power savings. All or some of these approaches can be effectively applied to obtain the optimal power-delay-area trade-off.

1.8 MOORE'S LAW

The scaling of the device dimension allows creating a high-performance system on the integrated circuit having minimum power consumption and occupying a very small area. Gordon Moore, co-founder of Intel, in 1965, had predicted about the scaling, that the number of transistors on a wafer in a given area will get doubled in every 18 months [3]. This law has been the motivating force behind the continuous reduction of device dimensions using scaling as shown in Figure 1.5.

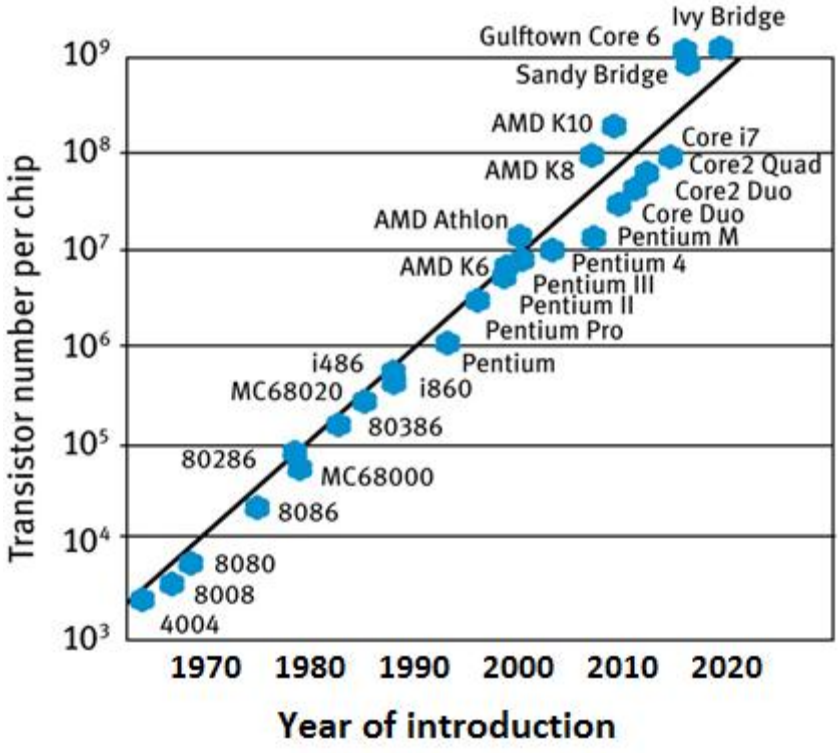

Figure 1.5: Moore's law

The scaling process has taken the CMOS devices in the sub-nano regime. The basic device structure still is the same but the gate lengths have been decreased from a few mm in the 1970s to less than 10nm recently in the fabrication unit [2]. The gate oxide thicknesses have also been reduced in the same proportion.

1.9 MOSFET SCALING

The semiconductor device technology is always aiming for the reduced size of the device. The process of reduction of the dimension of a MOSFET is known as scaling. Scaling maintains the same geometry as of the equivalent larger devices. It usually results in fast performance with more devices per unit area of the semiconductor. The channel length, width, doping density and oxide thickness are the major components on which the scaling is carried out. The scaling results in enhanced packaging density, operation speed and reduction in the cost of the IC [6]. Figure 1.6 shows the growing number of transistors on microprocessor ICs in the last 20 years.

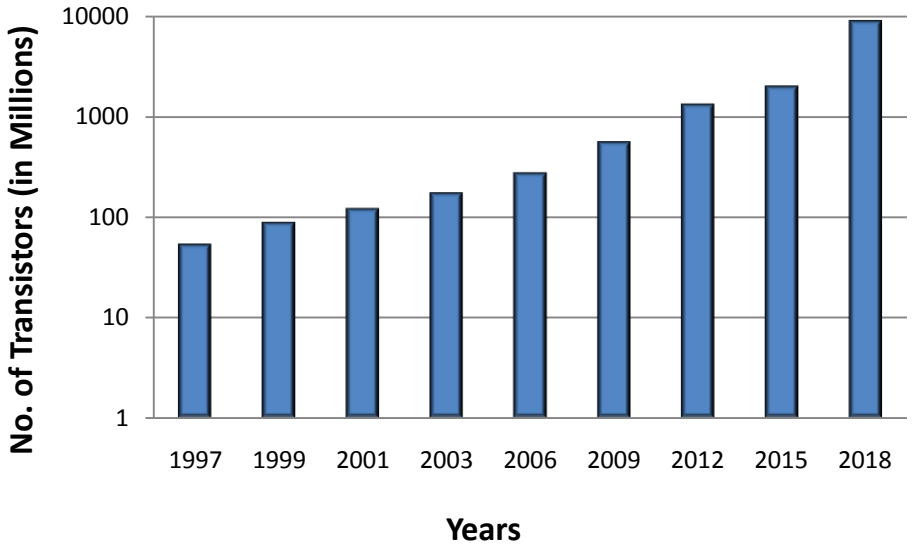

Figure 1.6: The increasing number of transistors per chip with device technology [10]

With the continuous scaling over the years, at present, the scaling of various dimensions has reached its optimum values and a further reduction in the oxide thickness will dent the insulator operations in MOSFETs. Hence, the appropriate mechanism is required to maintain a low gate leakage current besides device scaling.

1.9.1 Constant Field Scaling

Full scaling or constant field scaling is proposed by Dennard et al. [6]. In this scaling, a scaling factor ‘K’ is used to scale the dimension and voltage of the MOSFET, while sustaining the magnitude of the internal electric field in the horizontal and vertical direction as constant. This is achieved by scaling all the voltages in the same

proportion as device dimensions scaling. To maintain the constant electric field both V_{gs} (gate voltage) and V_{ds} (drain voltage) must be scaled by the same factor 'K' along with the t_{ox} (gate oxide thickness) by scaling the channel length by the same factor K. The substrate doping concentration is increased by a factor of 'K' to reduce the depletion width in the same proportion of channel length. The constant field scaling results in reducing the power-delay product of a MOSFET, the total power remains constant by keeping the area of the chip constant.

1.9.2 Constant Voltage Scaling

One of the limitations of constant field scaling is that the semiconductor device width cannot be scaled aggressively in the weak inversion region. The largest portion of the available supply voltage is consumed while switching the device. On the other hand, in constant voltage scaling, the potential of the devices remains unchanged while the scaling of the device dimensions is done by a factor '*K*'. This scaling results in an increase in the electric field and power dissipation. As the voltage remains constant in this scaling, the voltage compatibility is obtained with older circuit design methodologies [6]. The value of the threshold voltage will remain constant in this scaling but the power per device increases by a factor of 'K' which causes high power density per unit area. The substrate doping in this scaling also needs to be increased by a factor of 'K' to reduce the depletion width.

The constant voltage scaling results in an increase in an electric field with reduced dimensions. This phenomenon usually causes high leakage current, mobility degradation, low breakdown voltages and increased channel punch through, and hence, this type of scaling is generally not preferred.

1.9.3 Generalized Scaling

In the generalized scaling, the dimension of the device and the voltage of the device are scaled by different factors. This scaling results in low power dissipation and efficient speed of operation.

1.9.4 Modern Scaling

The threshold voltage and supply voltage are kept constant to maintain the balance between the off and on-current of the device. The high value of I_{on} and low value of I_{off} are more desirable to achieve high speed and low power for the semiconductor device. The threshold voltage is one of the key parameters to maintain the tradeoffs between speed and power. Modern scaling introduces the new doping profile like halo implants, new dielectric materials and strain engineering to increase mobility [14].

Table 1.1 shows the various types of scaling. The physical quantity before and after scaling is also mentioned in the Table.

Table 1.1: Various Types of Scaling [6]

Parameter Name	Before scaling	Constant Field Scaling	Constant Voltage Scaling	Generalized Scaling
Channel Length	L	1/K	1/K	1/K
Channel Width	W	1/K	1/K	1/K
Oxide Thickness	T_{OX}	1/K	$1/K^i$	1/K
Doping Concentration	N_A	K	K	K
Supply Voltage	V_{DD}	1/K	1	$1/K^i$
Threshold Voltage	V_T	1/K	1	$1/K^i$
Oxide Capacitance	C_{OX}	1/K	K	K

1.10. LIMITATIONS OF SCALING

The scaling of the MOSFET resulted in dimension reduction at a very rapid pace. A device having a channel length dimension comparable to the depth of source/drain junctions and drain/source depletion width at the drain and source junction now exists. However, it is difficult to control the channel potential by the gate, when the channel length of the MOS device decreases due to the influence of drain potential. This phenomenon results in non-ideal behaviour in the operation of MOSFET and is termed as SCEs or the short channel effects [5]. Many effects like tunnelling which occurs as the thickness of the gate dielectric are reduced, result in high off-state current and consequently limit CMOS scaling as significant consumption of power

takes place. The other short channel effects like DIBL (Drain Induced Barrier Lowering), CLM (Channel length modulation), mobility degradation, band-to-band tunnelling, GIDL (Gate Induced Drain Leakage) also occurs in the MOSFET device operations. These effects degrade the device performance and therefore need to be addressed carefully. CMOS design is severely affected due to these scaling limitations, which makes the conventional MOSFET unsuitable for use in the deep submicron regime. On the one end scaling improves the performance of the MOSFET device in terms of size, speed and power but on the other end, the downscaling of conventional MOSFET device causes short channel effects which result in performance degradation of the device. To further initiate the scaling, it requires new device structures which boost up the performance in nano regimes for the future generation of devices. The physical mechanisms like constraints on drift current in channel and variation in threshold voltage due to scaling contribute to short channel effects in MOSFETs [6].

The illustration of various short channel effects which affect the performance of MOSFET devices are as under

1.10.1. Drain Induced Barrier Lowering (DIBL)

The scaling is generally done in the manner where all the correlated parameters are scaled properly but when only the gate length is reduced without appropriately scaling the other dimensions during the scaling, the drain-induced barrier lowering effects occur. In the long channel MOSFET device, the channel is formed in the device under the influence of gate potential but when the applied potential is not sufficient, the conducting channel does not exist. The charge carriers in this condition will face the potential barrier that will block their flow. When sufficient gate voltage is applied then this potential barrier gets reduced and in the presence of a channel electric field, the charge carrier will flow from source to drain. In a small channel MOSFET, this barrier potential not only depends on the gate to source voltage but also on the drain to source voltage. If the drain voltage is increased the potential barrier in the channel gets reduced. This decrease in the potential barrier will ease the injection of more charge carriers into the channel resulting in an enhancement in drain current. This phenomenon where the drain to source voltage lowers the channel barrier potential is known as Drain Induced Barrier Lowering or DIBL. DIBL is a short channel effect

that was originally referred to as lowering of threshold voltage at high drain voltage [6]. DIBL can be reduced by increasing the doping concentration in the channel.

1.10.2 Velocity Saturation

Velocity saturation is another short channel effect. Due to the influence of an electric field, the charge carrier moves in the channel with electron drift velocity which varies linearly with electric field intensity. However, under the high electric field component, the drift velocity saturates and does not vary linearly but increases slowly with the electric field. When the device dimension is scaled-down without lowering bias voltage, the electric field increases, hence it makes the velocity saturation a more common phenomenon. The velocity saturation results in the reduction of drain current and transconductance of the device [15]

1.10.3 Impact Ionization

The impact ionization is a short channel effect that occurs due to the high electric field in the short channel of the MOSFET device. This phenomenon is mostly observed in NMOS devices. In this mechanism, hot carriers (electrons) generate a secondary electron-hole pair on the drain side. The electrons so generated causes the drain current to increase, the hole generated in the process causes the substrate current of the device as shown in Figure 1.7.

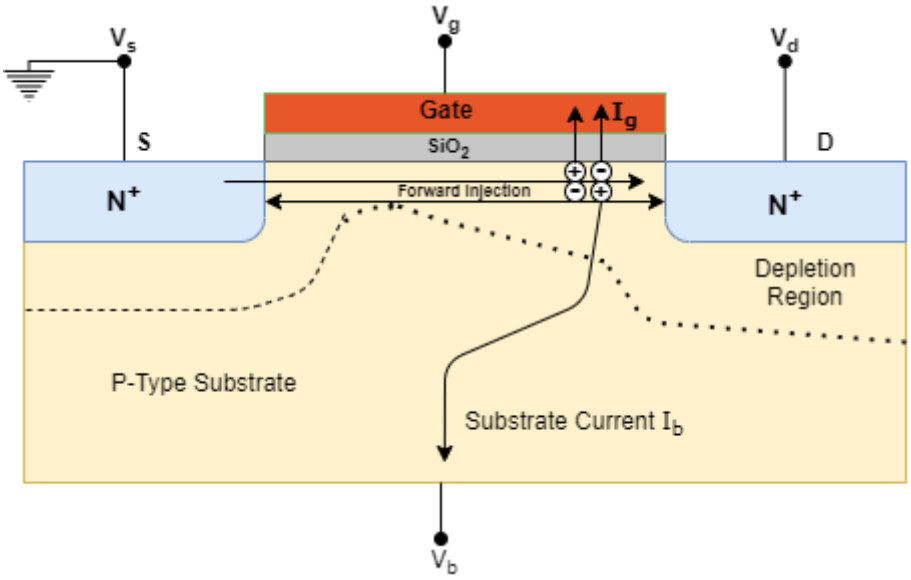

Figure 1.7: Impact Ionization [16]

1.10.4. Channel Length Modulation

In short channel devices at the reverse-biased drain substrate junction, the depletion region width starts to increase with the increase in drain voltage. This results in a reduction in the effective channel length and subsequently the drain current increases. The channel length modulation effect is prominent in the devices having a small channel length and comparatively low doping in the substrate. By increasing the doping of the substrate and scaling of the device reduces the effect of channel length modulation. In the extreme scenario punch-through occurs when the channel length due to channel length modulation reduces to zero. The consequence of punch-through is the enhancement in drain current with drain-source voltage. The increase in output conductance and reduction in the maximum operating voltage occurs due to punch-through [1]. The drain current I_D will vary due to the channel length modulation factorΔL_G. Figure 1.8 shows the channel length modulation.

$$I_D = I_{Dsat}/(1 - \Delta L_G/L_G) \qquad (1.7)$$

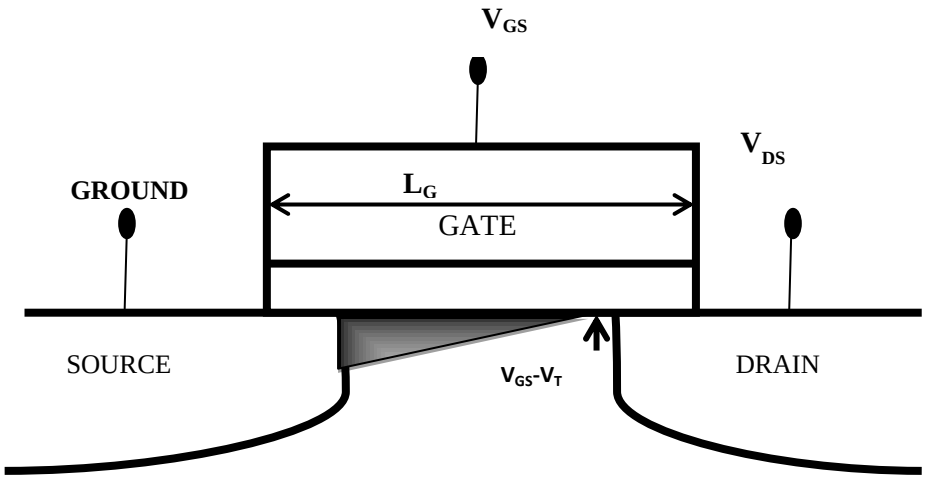

Figure 1.8: Channel Length Modulation [1]

1.10.5. Surface/Channel Scattering

In the small channel device, the effective channel length further reduces due to the extension of the depletion region into the channel. It increases the longitudinal component of the electric field. The surface mobility becomes dependent on the field.

As the charge carrier travelled through the channel near the surface, the channel scattering occurs due to the increased collision rate because of the accelerated electrons under the influence of the horizontal field. This results in a reduction in average surface mobility as compared to bulk mobility [17].

1.1.6. Hot Carrier Effect

In MOSFET devices, when the channel length is scaled without scaling the drain-source voltage, the electric field applied on charge carriers inside the channel increases more towards the drain region. The charge carriers moving from source to drain region accelerated with enough kinetic energy to cause the impact ionization. Some of these highly energized charged particles cross the Si-SiO_2 interface and reach in the oxide layer. These energized electrons are called hot electrons as they are not in thermal equilibrium with the lattice of the device. This effect increases the threshold voltage.

The electrons enter into the SiO_2 by tunnelling also. Direct tunnelling occurs in the thin oxide. For the high value of oxide thickness, Fowler–Nordheim field induces tunnelling of carriers which is possible due to the increase in the voltage across the oxide [18]. These energetic carriers damage the silicon oxide interface and a few of them are trapped in the oxide. The damaged oxide interface decreases the lifetime of the device. It is also known as hot-electron aging. The presence of a sufficient oxide charge changes the threshold voltage. This can affect the gate control and reliability of the device [18].

The hot carrier injection mechanisms can be classified into three categories as depicted in Figure 1.9. (a) The charge carrier created because of impact ionization can increase exponentially and constitute a large leakage current. (b) The highly energized charge can create conduction current (c) The highly energized electrons can penetrate to SiO_2 layer affecting the device characteristics like drain current, threshold voltage, etc. [18]

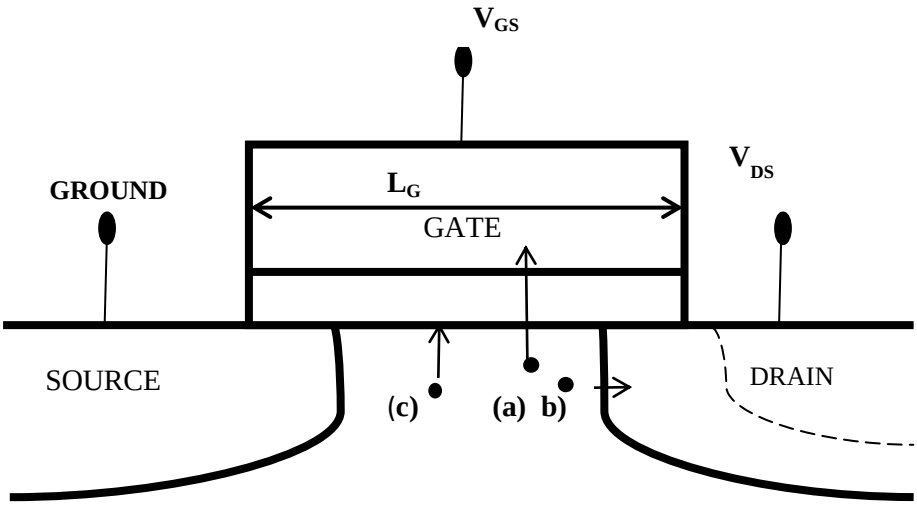

Figure 1.9: Hot carrier effects in MOSFETs

1.10.7 Source /Drain Parasitic Resistance/Capacitances

In the shallow junction devices, the source and drain resistances become an obstacle for further downscaling of MOSFET. The drain and source junctions of the MOS device have parasitic capacitances and resistances. These parasitic components degrade the switching speed and current driving capability of a MOSFET.

1.10.8 Mobility Degradation

Mobility of charge carriers is one important parameter as the drain current depends upon it. The mobility degradation in the MOSFET occurs due to both lateral and vertical electric fields. Due to the downscaling, the channel length is decreased and it results in a high electric field in the lateral direction. Hence the mobility starts to depend upon the electric field and results in velocity saturation and resultantly in current saturation. The vertical component of the field also increases with the reduction in the thickness of gate oxide. This increased vertical electric field causes the scattering of charge of a carrier near the Si-SiO_2 interface. Due to this surface scattering the surface mobility decreases and it also results in current saturation.

1.10.9 Fringing Field Effects

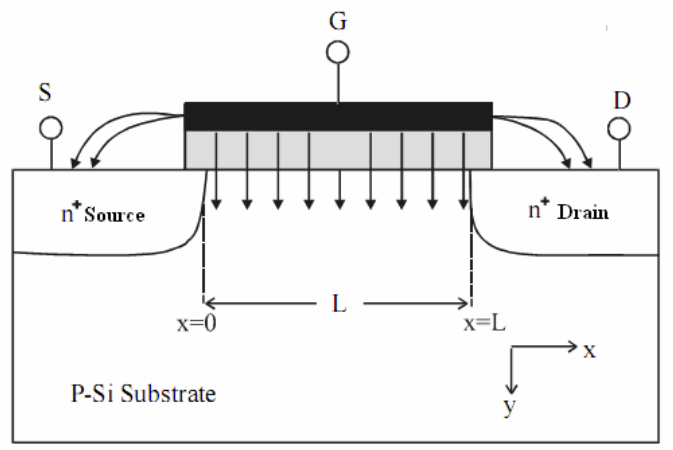

Figure 1.10: MOSFET cross-sectional view indicating fringing lines [6]

When the device length and width are reduced, the gate overlaps the source and drain regions. This overlapping causes electric field lines to become dense at the sidewall regions of the channel. These fringing field lines effectively increase the charge at the edges of the channel and affect the characteristics of the device. This phenomenon is called a fringing field effect. Figure 1.10 shows the fringing field lines.

1.10.10 Sub-threshold Conduction

When the device conducts at the gate voltage which is less than the threshold voltage, this mechanism is known as subthreshold conduction. In sub-threshold conduction only a small amount of current flows. This current is known as sub-threshold current. This sub-threshold current is the current which is flowing in the device during off state. Hence it causes to increase in the leakage current and static power dissipation. In practical devices, the sub-threshold current is negligible but non-zero. This current decreases exponentially when the gate voltage drops below the threshold voltage. These current components' characteristics become significant for the devices having channel lengths below 50nm [7].

1.10.11 Threshold Voltage Roll-off

When the channel length is reduced, the value of the threshold voltage also reduces it is called threshold voltage roll-off. The threshold voltage of MOSFET cannot be

scaled aggressively with channel length. The leakage current depends inversely on the threshold voltage. The increase in leakage current boosts up the static power dissipation. Hence, it degrades the device's performance. Designers will have to compromise between speed and power due to threshold voltage roll-off [15].

1.11 REDUCTION OF SHORT CHANNEL EFFECTS

The device engineers are looking for new methods to reduce the SCEs so that the packaging density of the device can be increased. This section gives various novel engineering methods which can improve the electrical performance of traditional devices.

1.11.1 Gate Dielectric Engineering

The scaling has continued for the last few decades to reduce the size and power dissipation and improve the performance of semiconductor-based ICs. For better gate control over the channel, the oxide thickness should be decreased in the same ratio as the channel length. SiO_2 has been the primary gate insulator for MOSFET for many years. The thinner gate oxide provides large oxide capacitances. Hence, it increases the drain current and also has control over the threshold voltage roll-off effect [15]. If gate oxide is very thin, then gate leakage current increase becomes the serious limiting factor for better performance. One possible solution is to use higher permittivity dielectric material compared to SiO_2. These high permittivity materials give more physical thickness along with a smaller effective oxide thickness (EOT) [11].

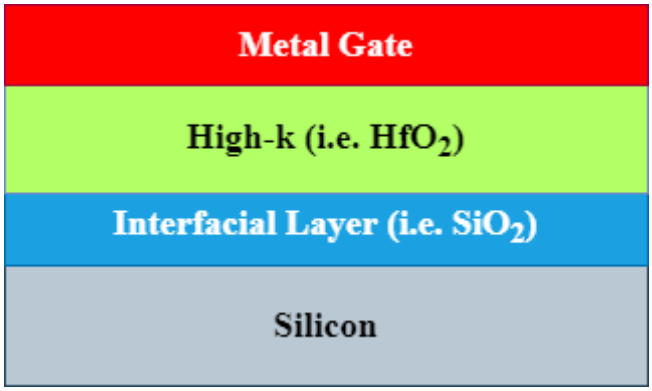

Figure 1.11: Gate stack architecture

High-k dielectrics as gate oxide material generate interface trap charges and reduce carrier mobility at the interface [19]. These dielectrics may result in the enhanced fringing field towards the drain/source which increases the control of the channel by the gate. It was experimented that an interfacial oxide layer should be present in the mid of silicon substrate and high-K material to maintain good interface quality.

The gate stack architecture shown in Figure 1.11 reduces the fringing field because the insertion of the interfacial layer reduces the high-k layer thickness to produce the same EOT. The EOT is given by equation 1.8 [4].

$$EOT = t_{SiO_2} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{High-K}} t_{High-K} \qquad (1.8)$$

In literature various materials which acts as high-k dielectric exists such as Al_2O_3 [Aluminium Oxide] (k~10), HfO_2 [Hafnium Oxide]/ZrO_2 [Zirconium dioxide] (k~25), La_2O_3 [Lanthanum oxide] (k~27) and TiO_2 [Titanium dioxide] (k~50) [20].

1.11.2 Channel Doping

The short channel effect like punch-through can be reduced by using enhanced substrate doping. Higher doping concentration usually increases junction capacitance and reduces channel mobility, which results in a reduction in threshold voltage control. The impact ionization can be reduced by using LDD (Lightly Doped Drain) structure [21]. Non-uniform doping and Halo doping are carried out in the channel to decrease the threshold voltage dependence on the channel length.

Asymmetric channel doping suppresses the depletion region thickness close to drain and source. This will increase the transconductance and result in the reduction in SCEs [21]. For n-MOSFET, the heavily doped p-type region is created near to drain and source regions. Asymmetrical or symmetrical doping can be done near the drain and source but non-uniform doping produces reverse short channel effects. This causes an increase in threshold voltage with a reduction in gate length. Figure 1.12 shows the conventional MOSFET, MOSFET with Asymmetric Halo Doping and MOSFET with Symmetric Halo Doping.

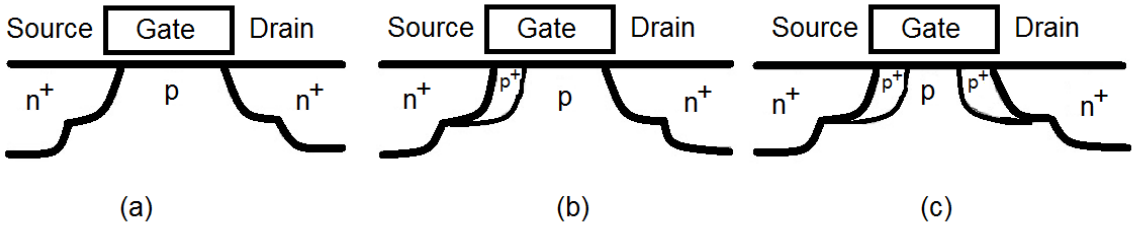

Figure 1.12 (a) Conventional MOSFET, (b) Asymmetric halo doping, (c) Symmetric halo doping [21].

1.11.3 Gate Metal Engineering

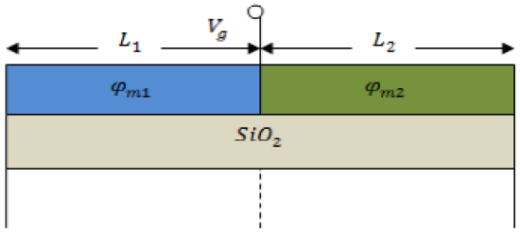

Figure 1.13: Multi-material gate structure

Single metal gates (SMG) used over the year, have constraints for further scaling. Gate metal engineering was first introduced by Long et al. [22]. In gate metal engineering, the gate is made from two different materials. This kind of gate structure is shown in Figure 1.13.

When the gate is made using two different materials it is called a Dual Material Gate (DMG). The metal near to source side has high work functions compared to the metal used near to drain. The two gates are called the control gate and screen gate. The control gate exists near the source and the screen gate exists near the drain. The channel has a peak electric field due to the variation in the work function difference; it increases the electric field close to the source side. This increased electric field reduces the variation in potential near to drain side and mitigates the effects of channel length modulation. In the source region, the increased electric field causes a high, carrier velocity, which decreases the hot carrier effects. The enhanced carrier transport velocity further increases the drain current and transconductance. To further

reinforce the immunity against SCEs, different multi-gate structures were proposed by various researchers. [23-25].

1.12 ALTERNATIVE MOSFET DEVICE STRUCTURES

For the last 50 years, MOSFET devices are the dominant technology in integrated circuit manufacturing but the primary issue with MOSFET is the existence of SCEs at reduced channel length. To make the best use of scaling many innovative device structures of MOSFET have been proposed by various researchers. Some of these structures are as

1.12.1 Silicon over Insulator (SOI)

SCEs can be minimized by using Silicon-on-insulator (SOI) technology. The top layer of MOSFET is useful for electrons transport, and most of the bulk volume of the device only generates parasitic effects. In SOI technology, MOSFET is created in a shallow layer of silicon semiconductor placed over the insulator called "Buried Oxide". The SOI MOSFET provides high packaging density with respect to conventional bulk MOSFET. It is due to the absence of wells and availability of buried oxide (SiO_2) layer which decreases the parasitic drain/source to substrate capacitance and reduces latch-up. The SOI device results in better speed and low power dissipation [26]. A sharp subthreshold slope and reduced leakage current are also achieved, which results in better device performance as compared to bulk MOSFETs. SOI MOSFET is of two types namely I) Partially Depleted Devices ii) Fully Depleted Devices.

1.12.1.1 Partially depleted (PD) devices

When the silicon film is thicker than the depletion width, the device is called partially depleted SOI because the depletion of the channel is partial during the normal operation of the device. The body is not completely depleted under normal bias conditions as shown in Figure 1.14 (a).

1.12.1.2 Fully depleted (FD) devices

If silicon film is thinner than the depletion width, then the channel region under the inverting layer is fully depleted. The Body is completely depleted under normal bias conditions as shown in Figure 1.14(b). The main advantage of SOI technology is a reduction in SCEs, kink effect, lower threshold voltage, body effect and elimination of latch-up. The floating body causes self-heating. The application of SOI MOSFET is in military and space applications.

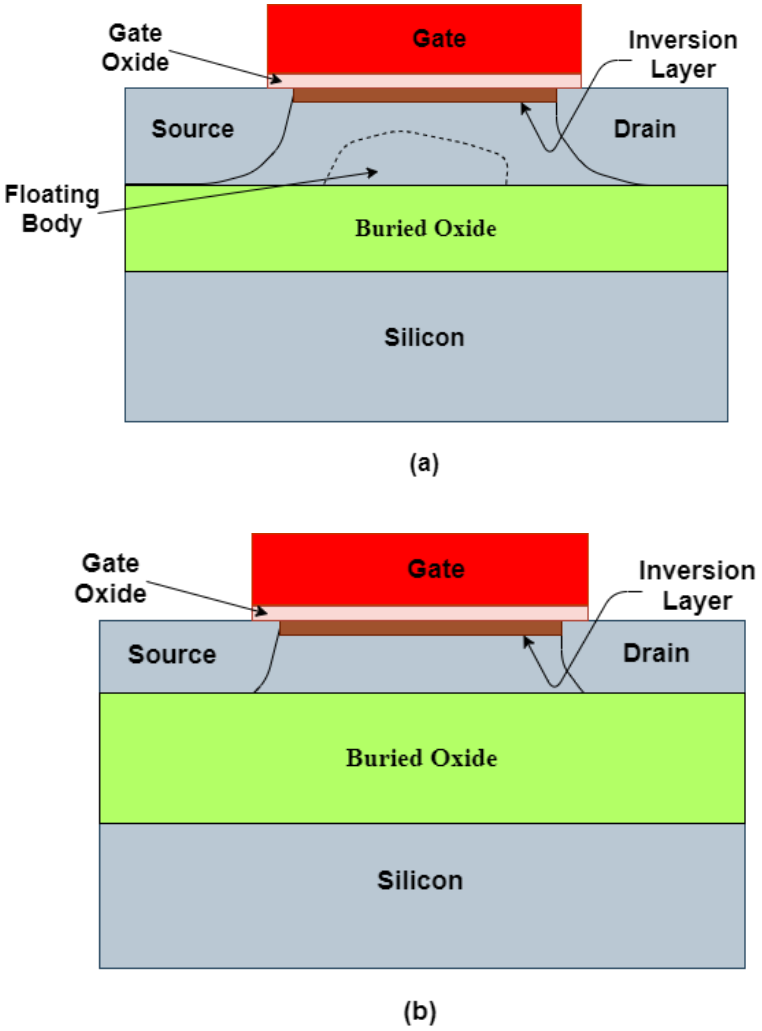

Figure 1.14 (a) PD SOI, (b) FD SOI transistor

However, it is found that for short channel length even an SOI device is not able to suppress the SCEs efficiently thereby the performance of the devices degrades. As the device size is reduced, the influence of the Drain Induced Barrier Lowering (DIBL) increases. One of the drawbacks of DIBL is that the electric flux from the drain side

affects the channel potential resulting in degradation in device characteristics. The other effects of reduction of the thickness of the oxide layer are observed in an increase in parasitic capacitance [27].

When the oxide layer thickness is reduced, it increases parasitic capacitances. The thermal conductivity of buried oxide is less than the silicon which restrains the cooling of the device and causes self-heating in SOI devices. Hence, most of the SOI structure operates at higher temperatures. Various researchers [27-28] claimed that a single gate SOI device will fail to offer improved device characteristics in the ultra-short channel length.

1.12.2 MULTIGATE MOSFET

With the failure of conventional MOSFET at lower technology nodes multiple structures were proposed by many researchers. The continuous effort has been made to have good control over SCEs and enhance the current drive capability of the MOSFET. A proposed concept of multiple gates SOI MOSFET technology offers many advantages in this regards [29]. The multigate MOSFET gives a high "ON" current and low leakage current which improves the device performance. The drain field reduces much more effectively by using multigate MOSFET. It was observed that the effective channel length of a MOSFET should be 5-10 times more than the natural length of the channel (the channel length controlled by the drain bias) [29]. Many works of literature report that the current driving capability of multi-gate is the number of gates times the current driving capability of a single gate [29-30].

1.12.2.1 Double Gate MOSFET

The double gate devices structures have very good scaling ability in the nanometer range. The two gates i.e. front gate and back gate bring better inversion of the volume in the channel region. It results in increased transconductance and better drain current [29]. In a Double-Gate MOSFET (DG), the bottom gate helps in controlling the channel potential in an efficient manner leading to suppressed short channel effects by improving the device performance as compared to single gate MOSFET. The inverted charge present in the channel of the double gate is twice the charge present in the inverted channel of the single gate MOSFET [29].

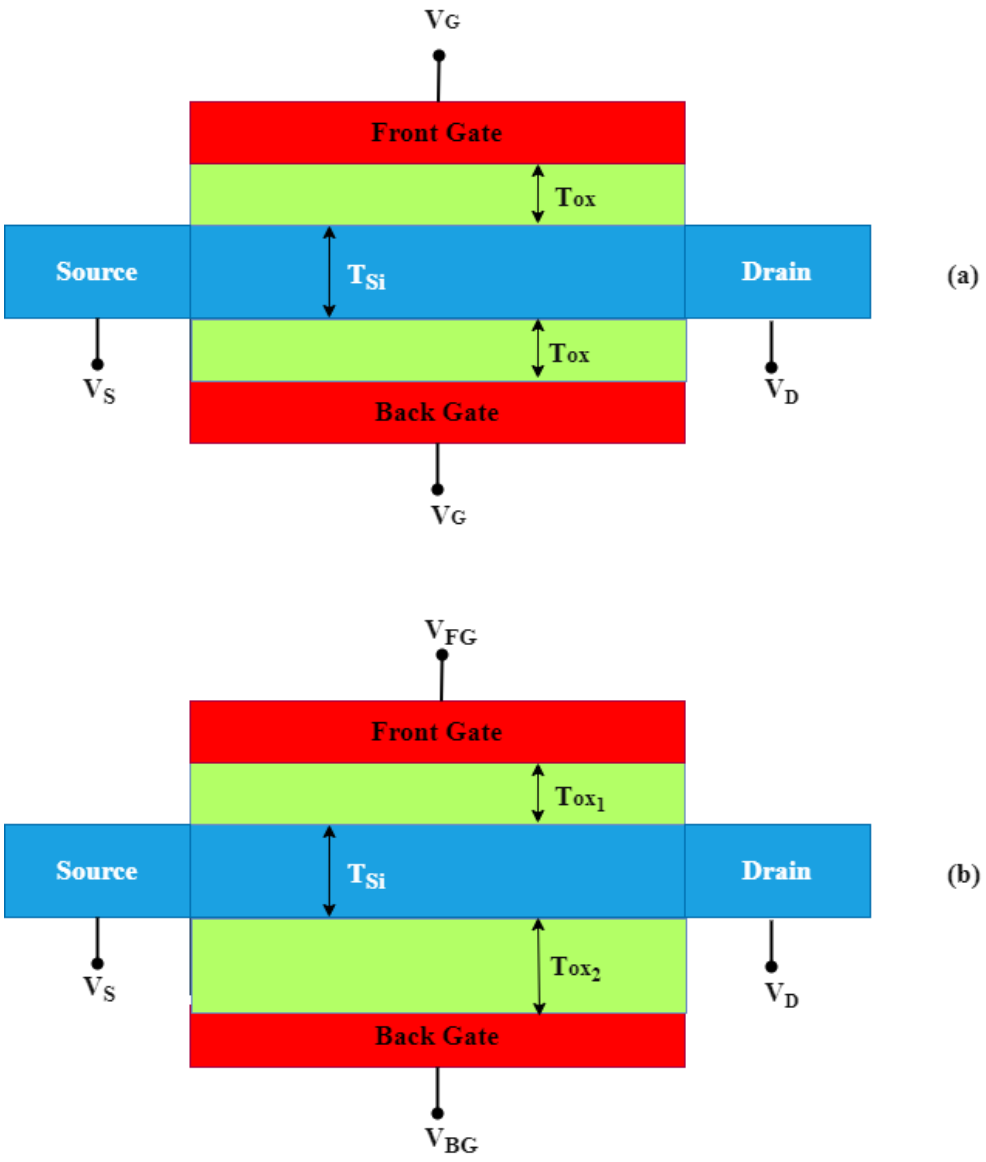

Figure 1.15: (a) Symmetric Double Gate MOSFET (b) Asymmetric Double Gate MOSFET

The major constraints in making the double-gate MOSFET are the alignments of two gates. Hence many researchers exert that triple gate design is comparatively easier as compared to double-gate MOSFET [31]. There are two structures possible for Double Gate MOSFET - symmetric Double gate MOSFET and Asymmetric Double gate MOSFET as shown in Figure 1.15 (a) and 1.15 (b) respectively.

In asymmetrical DG MOSFET, separate biasing is given to the front and back gate and the thickness of the two oxides is also different whereas in the symmetrical Double Gate MOSFET, both oxides have the same thickness and both the gates are

tied together with common bias. The Double Gate MOSFET current is almost twice the single gate MOSFET. The junction capacitance and random dopant fluctuation are gets decreased in DG MOSFET. The channel mobility is also found to be higher in symmetrical MOSFET [31]. Hence, it demonstrates higher performance with respect to bulk MOSFET.

1.12.3 Junctionless Field Effect Transistors (JLT)

The Junctionless Field Effect Transistors (JLFET) or JLT have heavily doped silicon film and a gate to modulate the carrier concentration in the channel to control the resistivity of the channel. The source and drain are heavily doped to have better ohmic contacts. Since the doping and material from source to drain through the channel is the same hence the presence of junction is eliminated. The structure of the JLT device is shown in Figure 1.16.

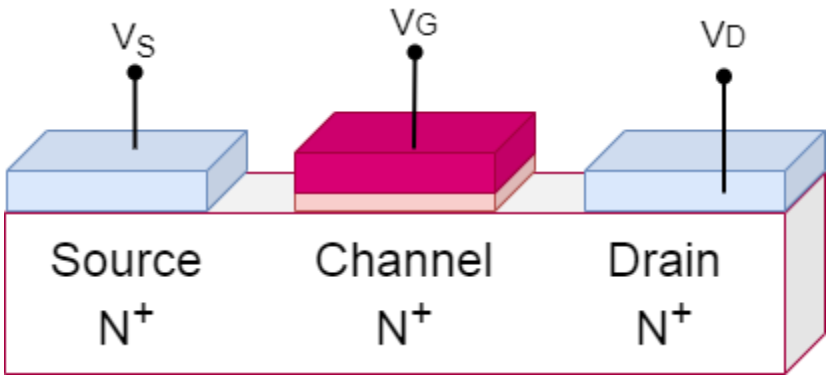

Figure 1.16: Structure of Junctionless Field-Effect Transistor

In JLFET, the work function difference between the metal gate and semiconductor is such that the electrons would flow from the semiconductor interface to metal. The gate electrode work function creates volume depletion of the channel region to switch off the device. In these devices when a positive voltage is applied at the gate, the depletion layer starts to reduce and expose the undepleted region in the middle of the channel. It allows majority charge carriers to flow from source to drain. The gate voltage at which, this undepleted region in the middle of the channel vanishes due to the merging of the depleted region is called threshold voltage.

By making the gate more positive the width of the depletion region reduces and hence exposing more undepleted regions for the charge carrier to move on. The charge conduction that takes place throughout the device reduces the possibility of trapping the charge carrier near the surface, so it makes the device less affected by many SCEs like the surface scattering and reduction mobility of charge carrier near the surface [32]. The JLTs have many advantages associated due to their working principle and simple fabrication process as compared to conventional MOSFETs.

1.12.4 Other Alternative Device Structures

The era of semiconductor devices research is everlasting. Many researchers over the years have proposed multiple devices [21, 23, and 29] which differ from the predecessor in term of structure, materials or technology. Many of these devices are currently available in existing integrated circuits and some of them are still under investigation. The device like surround gate MOSFET, in which the gate is made all around the device to have better control over the channel are the promising devices and continuous research is carried out on this front.

The FinFET structure in which a self-aligned double gate is efficiently used, have a channel created in vertical fin made up of semiconductors. This structure shows very good characteristics against SCEs.

The device structure like tunnel FETs, 2D FETs, nanowire FETs and nanotube FETs are also promising devices for the future generation of devices.

1.13 TECHNOLOGY COMPUTER-AIDED DESIGN (TCAD) UTILIZATION

TACD is a potent tool for improving design productivity, decreasing design costs and for getting better device designs. The computation tools are cost-effective solutions as compared to establishing a good and capable foundry unit. The TCAD tools are capable of predicting the various electrical characteristics of device design in a cost and time-effective manner. The modern TCAD tools are capable of predicting physical characteristics like doping distribution and oxide thickness with high accuracy during the process modeling of the fabrication process. For the specific

device structure, the exact characteristics can be predicted without carrying out any physical process.

TCAD tools support various models related to the fabrication simulation process, these models are selected depending upon the requirement of the simulation environment. The other application of the TCAD tool is that it assists to appreciate the working of the device and replicating the physical conditions applied to the device and their impact thereon. The quantities which are difficult to obtain experimentally are readily available while using the TCAD tools. Hence, it can be said that TCAD tools simulations help in analyzing the behavior of any semiconductor device/circuits without moving into the complex and costly process of fabrication and characterization, which reduces time to market.

Silvaco's TCAD tool is one such TCAD tool used for semiconductor device simulators. Silvaco's tools design flow [33] starts with a meshing in-process simulator, Athena. The Atlas package is used to simulate the electrical characteristics of semiconductor devices. The various models are utilized to numerically simulate the electrical behavior of a device in an individual capacity or in the circuit. The parameters like current, voltage, field, charges, etc. are calculated based on the modelling equation applicable to the specific device for a particular model and carrier conduction mechanism. The Tonyplot tool is used to plot and view the characteristics output from the various simulation.

1.14 DEVICE MODELLING

The device modelling of a semiconductor device is done to explain the behavioural characteristics of the devices. The models are thus prepared to represent the device behaviour in all the operational regions as Capacitance voltage (CV) characteristics, current-voltage (I-V) characteristics and transport process. These models can be divided into two broad categories of physical device models and equivalent circuit models.

The physical model of a semiconductor device predicts the transport mechanism and terminal behaviour of the device. It includes the parameters like device structure, materials properties, doping profile and transport equations for the charge carriers.

The present-day scaled devices are modelled in 2 or 3-dimensional aspects to exactly predict the behaviour of the device. These complex equations for the new device can only be solved by numerical methods using the device simulators. These device simulators are very exhaustive and consume many resources of the computational facility. Hence, these approaches are not preferred in circuit simulation where multiple devices exist.

The equivalent circuit model depicts the electrical characteristics of the semiconductor device in the circuit. These models are obtained from an empirical approach or the analytical function. These models are dependent on the frequency of the applied signal, temperature and the DC bias applied to the circuit. The three basic types of circuit models that exist in generals are the AC model, transient model and DC model. These models are differentiated in terms of the response of the circuit which varies with time.

1.14.1 MOSFET Device Modelling

The different kinds of MOS devices that control the flow of charge carriers in the channels of the scaled devices are made using various techniques and there are new to designer engineers. Modelling of these devices is carried out to predict the operation of the circuits where these devices are employed. The new physical device models are also required to be included in device compact models, which are used in circuit modelling. The accurate model in terms of current and thermal characteristics, if available for a novel semiconductor device will ensure its usage in the circuit. The devices in which the volume conduction occurs have different modelling principles compared to bulk MOSFET.

1.14.2 Analytical Models

The model equations which are derived from device physics represent the analytical model of the semiconductor device. These analytical models can be classified into two categories as a surface potential model and a semi-empirical analytical model [34]. The surface potential models are continuous in all the operational regions. These models can accurately determine current but the equation used to represent the model are often complex and required many iterations to compute surface potential under a

specific bias. In semi-empirical models, various approximations are applied in the equations depending upon the mechanism which will dominate. These models are preferred to represent first-order device behaviour. Semi-empirical models describe the electrical behaviour and relation between physical mechanism and device structure. However, these models are technology-specific and take time to develop due to the presence of a complex equation [34].

1.15 RESEARCH OBJECTIVE

The various objectives planned are as follows:

- To simulate the scaled model of the bulk MOS device to lower technology nodes and enhance its performance by applying the Gate engineering process.
- To implement and simulate the reported low leakage Double Gate Silicon On Insulator (DG-SOI) MOSFET device and apply Gate engineering for its performance enhancement.
- To validate the analytical modeling of Junctionless Field Effect Transistor (JLFET) for different characteristics.
- To implement the superior MOSFET device structure based on JLFET for a very low leakage current.
- To analyze the inverter circuit implemented with this superior MOSFET device.

1.16 RESEARCH METHODOLOGY

The followings steps were performed to achieve the above-mentioned objectives

Step 1: Literature survey was divided into four parts. In the first part, the gate engineering approaches, the second part deal with dielectric engineering approaches and the third part deal with the channel engineering approach used by various researchers for MOSFET structures to improve various device characteristics were studied. In the fourth part, alternate MOSFET structures with better electrical characteristics have been reviewed.

Step 2: The scaled bulk MOSFET was implemented virtually using SILVACO TCAD software.

Step 3: Device engineered MOSFET to reduce leakage components were simulated and optimized.

Step 4: Alternate MOSFET structures such as Junctionless FET were simulated and comparative analysis with earlier implemented MOSFETs was carried out.

Step 5: The analytical modelling of JLFET was carried out for validation of simulated results.

Step 6: Implementation and modelling of superior JLFET based MOSFET device structure were carried out.

Step 7: Finally this superior JLFET based MOSFET device was implemented in the inverter circuit and analyzed for suitability and various electrical characteristics.

1.17 THESIS ORGANISATION

This thesis includes six chapters and these chapters are summarized as:

Chapter 1: Introduction

This chapter includes the introduction of the fundamental concepts related to MOSFET, technology trends in power dissipation, fundamentals of scaling and its effects on MOSFET, the mechanisms to reduce the scaling effects, alternate device structures. It also includes an introduction to device modelling.

Chapter 2: Literature Review

This chapter reviews the short-channel effects in small dimension MOSFETs. The methods applied by different researchers to control the short channel effects are included in this chapter. The works of literature related to alternate MOSFET structures such as multi-gate MOSFETs, SOI, Junctionless MOSFET structures are also reviewed in this chapter.

Chapter 3: Analysis of Double Gate SOI MOSFET

This chapter demonstrates the implementation of bulk MOSFET and other devices/gate-engineered MOSFETs device structures for the suppression of various SCEs and compares various characteristics with different gate engineering approaches.

Chapter 4: Analytical Modelling and Simulation of Junctionless Transistor

This chapter includes the modeling and simulation of JLFETs. The comparison among various implementations is also carried out in this chapter. The analytical model validation is also carried out in this chapter.

Chapter 5: Analytical Modeling of Subthreshold Current for SD-TM-CGAA-JLFET DEVICE for Low Power CMOS Inverter

In this chapter, the novel SD-TM-CGAA-JLFET MOSFET device based on JLFET is modeled and simulated using SILVACO TCAD software. This chapter also includes the implementation of this novel MOSFET having superior electrical characteristics in the inverter circuits and its analysis for various electrical characteristics.

Chapter 6: Conclusion & Future Scope

This chapter concludes the various results obtained and further discusses the future scope associated with this research.

CHAPTER-II

LITERATURE REVIEW

2.1 INTRODUCTION

The forthcoming electronics products will be more capable in terms of computation, having less power dissipation and most importantly small-sized than their predecessor. By reducing the size of traditional MOSFETs, the performance of the device diminishes due to the presence of Short Channel Effects (SCEs) [16]. Novel structures like Multi-gate MOSFETs were found to be more efficient semiconductor device structures to enhance the performance in the nano-scale regime [16]. The ITRS [12] had observed the usefulness of MOSFETs with multi-gates and termed them as "Advanced Devices". The reduction in device size involves a reduction in separation between drain and source which decreases the capacitive control of the gate terminal over the channel. The presence of SCEs in scaled devices reduces the effectiveness of the MOSFETs [3]. The researchers are always looking for small-sized devices having the negligible presence of SCEs. The multi-gate MOSFETs have proved to be the most potent semiconductor devices with excellent performance. These multi-gate structures include double-gate (DG), triple-gate (TG), Quad-Gate (QG) and gate all around (GAA) MOSFETs which enhance the device performance in comparison to traditional single gate MOSFETs devices. In double-gate MOSFETs, two gates are present to control the channel current. The double gate device shows good performance in terms of SCEs in comparison to conventional MOSFETs [15].

The reduction of leakage current to reduce power dissipation is a very complex process for scaled devices. The Channel Engineering, Gate Engineering and Device Engineering techniques are applied to further boost up the device performance and device efficiency. Gate Engineering was introduced by Long et al. [31] by proposing a Dual Material Gate or (DMG) MOSFETs. In DMG the two dissimilar metals having distinct work functions are used to construct the gate. This approach results in suppression of the SCEs [22].

In conventional MOSFET, the value of the electric field is high towards the drain region and low towards the source region which can be attributed to the injection of hot electrons towards the drain. It usually results in the poor performance of the MOSFET. The leakage current can be reduced without decreasing the on-current of the device by reducing the magnitude of the electric field towards the region adjacent to the drain [22]. The device design approaches like halo implant [20] are usually done to reduce the hot carrier effects. The other design approaches like gate stack and gate engineering usually result in lower leakage currents and a decrease in SCEs [22].

The conventional MOSFET when scaled to a lower technology node not only difficult to process but fails on various parameters like short channel effects and static leakage currents [23]. To continue the scaling, Device Engineering is continuously carried out in which advanced device structures are modelled and verified for the leakage current as well as for various SCEs. The design approach like SOI, Tunnel FETs, Junctionless FETs and Nanowire Transistors [24] will continue to serve the purpose of scaling of devices.

The development of advanced semiconductor devices generally applies two approaches. The first approach is the numerical simulation of structure with TCAD [30] tools. The second approach includes an analytical modelling solution. The analytical modelling includes solution approaches using charge sharing or by solving Poisson's Equation. Many methods had been suggested in various works of literature [22-25] to develop solutions using Poisson's Equation. The methods include Fourier Series Expansion, Newton Raphson Method, Superposition Method, Parabolic Approximation Method and Green Function Approach [27].

2.2 GATE ENGINEERING

The Gate engineering technique approach [22] includes the modification of the gate design to the dual-material gate or tri-material gate. A gate of metal having a higher value of work-function is utilized towards the source region known as control gate and a low-value work-function metal gate is employed towards the drain region known as screen gate. The screen gate hinders the variation of the drain voltage [33]. This approach results in the potential profile of step nature because of the swift change in the electric field and consequently velocity of charge carriers at the crossing

point of two gates of different materials. This step profile improves transconductance and reduces the DIBL and sub-threshold leakage current [33]. Many diverse Gate Engineering structures have been being examined to date.

Reddy & Kumar [34] proposed the analytical modelling solution of the dual material double gate (DMDG) device. The DM-DG device incorporates the benefits of the dual-gate and dual metal gate approaches. The revised transconductance and electric field towards the drain region decrease reportedly by using the DM-DG structure. The main disadvantage with DM-DG structure is the threshold voltage strong dependence on the thickness of silicon film.

Ghosh et al. [35] developed an analytical model for DMG-CG MOSFET. This analytical model includes the drain conductance and transconductance parameter. The impact of technology parameter variations and work function differences has also been described. The authors reported that with the enhanced work-function of the gate towards the source region, the sub-threshold current was found to be decreasing. This indicates an enhancement in the performance of the device. The results depict that the DMG SGT device shows superior performance than SMG SGT MOSFET.

Chiang et al. [36] have developed a model using Poisson's equation for DMG MOSFETs by using Superposition Method. The Parabolic Approximation Method has been used by Saxena et al. [37] for the development of the analytical model for DMG MOSFETs. The surface potential modelling was carried out by Syamal et al. [38] by Newton Raphson Approach for DG MOSFETs.

Wang et al. [39] modelled surface potential by using a complex two-dimensional superposition method for short channel Triple Material Surrounding Gate (TMSG) MOSFETs. The method of Parabolic Approximation also is used in this work to model threshold voltage.

2.2.1 Threshold Voltage Characteristics

Xi Liu et al. [40] proposed a variable separation-based analytical model of FDDG MOSFET. The model was derived using complex mathematical equations and shows a better analysis of various short channel effects for short-channel MOSFETs.

Auth et al. [41] presented an analytical model for surrounding-gate MOSFETs. DIBL and subthreshold slope of the SG MOS structures are compared with DG-MOSFETs in this paper. The approach effectively shows the feasibility of the non-gate-engineered structures of SG-MOSFETs.

Wang et al. [42] proposed an analytical model for DG MOSFET using the concept of localized charge carriers. 2D Poisson Equation is solved by using the Parabolic Approximation Technique. The compact threshold model shows good correlations among device dimension and hot carriers induced device degradation.

Verma et al. [43] presented the physics-based mathematical model for Cylindrical Surrounding Double Gate Nanowire MOSFET. The superposition method is used to find out the potential, field and threshold voltage in this paper. In comparison to other conventional surrounding gate MOSFETs, CSDG MOSFET has better gate controllability over the channel. The effect of variation in channel length on different electrical characteristics has been also analyzed.

Wong et al. [44] developed a transconductance charge method for the calculation of thin oxide MOSFET's threshold voltage. This voltage is determined at gate voltage, using the highest value of the derivative of transconductance. This method is suitable only for thin oxide MOSFETs.

T.K. Chiang [45] has investigated fully depleted cylindrical surrounding gate MOSFETs for threshold voltage using a 2D Poisson Equation solved by Superposition Approach for 1D and 2D equations. The minimum surface potential approach is utilized for the development of a threshold voltage model. This research paper effectively depicts the relationship of threshold voltage roll-off with the thickness of gate oxide and silicon films.

M.A. Abdi et al. [46] presented a 2D threshold voltage model of DG MOSFET in the subthreshold region. The amelioration in oxide and channel materials gives birth to a new device known as Graded Channel Gate Stack (GCGS) DG MOSFET. The step potential profile along with the incorporation of a high-k oxide layer diminishes the SCEs in terms of reduction in roll-off of the threshold voltage.

K.P. Pradhan et al. [47] evaluated the threshold voltage using the proposed center potential model of a CGAA MOSFET using Poisson's Equation. The device constraints variation relationship with the threshold voltage is also presented in this paper. Furthermore, a comparative study between surface and center potential models has also been carried out to establish the accuracy of the center potential model for the calculation of threshold voltage.

Woo et al. [48] used the analytical model of thin-film SOI MOSFET for the threshold voltage. The 2D Poisson's Equation was solved with variable separation Infinite Series Method. The solution requires many analytical equations and is complex. The device characteristic was found to be strongly dependent upon the substrate bias.

N.B. Balamurgan et al. [49] investigated the cylindrical and rectangular surrounding gate MOSFET for the threshold voltage model. The variation in threshold voltage by different MOSFET device parameters like drain bias, gate oxide thickness and thickness of silicon film was analyzed for cylindrical and rectangular surrounding gate MOSFETs. The performance of the rectangular gate device was found to be influenced by the corner effect which causes premature inversion as well as the occurrence of SCEs. Cylindrical gate device is not affected by corner effects.

Himangi Sood et al. [50] presented the numerical modelling for cylindrical surrounding gate (CSG) MOSFETs for Gaussian doped and undoped states. The analytical model illustrates the dependency of threshold potential on gate voltage for undoped CSG. It was observed that the surface potential variation above the threshold voltage does not depend upon silicon thickness. These variations are altered by modifying the work function. The surface potential at the drain and source sides are used to represent drain current and capacitances. Taylor Series Expansion Approach was applied for the solution of surface potential equations. The threshold voltage relationship with projected range and stagger factor are also described in this research paper. The results show the supremacy of SG MOSFET in terms of unilateral and maximum stable power gain.

Kumar et al. [51] have analyzed the dual-material surrounding gate device with a novel numerical model for the threshold voltage. The model was able to predict

efficiently about threshold voltage roll-off for the short channelled device. This research paper also discusses the diminishing SCEs in the DM-SGTdevice structure.

P. Suveetha et al. [52] have presented a model for the TM-SG MOSFET. In TM-SG, the gate is made with three metals having varied work-function. The parabolic approximation approach is used for developing the threshold voltage model and surface potential model. The model demonstrates the effectiveness of device design in reducing the SCEs and improving the carrier transport efficiency.

M. Kumar et al. [53] developed the analytical model of DMG SGMOSFETs for the threshold voltage. The correlation between the reduction in channel length and threshold voltage roll-off is developed in the reported work. The effect on DMG SG MOSFET with varying device parameters is also discussed and analyzed.

G.K. Saramekala et al. [54] proposed a DMG recessed source/drain SOI MOSFET and developed an analytical model for the threshold voltage. The developed model assures overcoming SCEs in DIBL and HCE. The DMG produces a step profile in the potential which is responsible for the reduction in HCE and DIBL. The screen gate length effectively controls the DIBL. The SCEs were found to be reduced efficiently in DMG as compared to SMG.

Sarvesh Dubey et al. [55] present an analytical model of a TMCGAA MOSFET for threshold voltage by using Parabolic Approximation. 2D Poisson Equation in a cylindrical coordinate system is used to find out the center and surface potential. The center potential model was applied to find the threshold voltage and DIBL. This research paper also presents the impact of device parameter variation on the threshold voltage. It was observed that by increasing the screen gate length ratio, there is a decrease in the DIBL and hot carrier effect (HCE) but it also increases other SCEs. Hence, the optimum value of device parameters is selected for the appropriate value of the threshold voltage.

Naskar et al. [56] present an analytical model for DM-DG silicon on nothing (SON) MOSFET including carrier quantization. The inversion charge and potential have been found out using 2D Poisson and 1D Schrodinger Equations. This structure provides a step potential profile that leads to a decrease in SCEs. This structure also

enhances the screening effect which ameliorates the drain conductance and DIBL. It can also be scrutinized that DM-DG SON structures give a lower threshold voltage as compared to DG MOSFETs.

B. Jena et al. [57] proposed a novel device structure as Work-Functional Modulated Conical Surrounding Gate (WMC-SG) MOSFET by introducing a gate metal with an incessant deviation of work-function. The device is compared with basic conical SG MOSFET. The simulated result depicts that WMC MOSFET provides high on current and reduced DIBL in GAA MOSFET due to better electrostatic control. HCEs are also reduced due to the reduction in the field towards the drain. Furthermore, the investigation was done to scale silicon film and oxide thickness on WMC MOSFET.

P. Suveetha et al. [58] presented the threshold voltage model of a TM-SG MOSFET. The model shows the significance of the Gate Engineering Approach in MOSFETs. This research paper elaborates on the reduction of SCEs with Gate Engineering Structure as compared to conventional MOSFETs. The correlation among variation in threshold voltage with other MOSFET parameters i.e. gate length ratios, doping concentration, the thickness of oxide and thickness of silicon is also developed.

Cong et al. [59] employ Halo Doping in surrounding gate (HD-SG) MOSFET. The threshold voltage and subthreshold current are calculated using 2DPoisson's Equation over the cylindrical coordinates system of the above MOSFETs structure. This research paper depicts that the superposition technique shows higher accuracy than the parabolic approximation technique especially for the small oxide thickness compared to the dimension of the silicon channel. The characteristics of the threshold voltage can be further improved by considering low gate oxide thickness, the small value of channel radius and halo doping.

P.Suveetha [60] developed the analytical modelling of SH-TM-SG MOSFET. The sub-threshold current and threshold voltage was calculated by the parabolic approximation method. The roll-off of the threshold voltage is reduced that indicating the suppression of SCEs.

2.2.2 Sub-threshold Characteristics

Liu & Hsieh [61] analyzed the sub-threshold behaviour of a device using the analytical model. The model assumes that the voltage difference in the drain and the source terminals are small for the threshold voltage above the gate to source voltage. However, the above assumptions do not apply to triple material structures.

Bayani et al. [62] presented CSG MOSFET with different cross-sectional areas with germanium is used as channel material instead of silicon. The circular cross-section gives the highest I_{on}/I_{off} ratio and sub-threshold swing which means an enhancement in device performance. But the fabrication of such a device is difficult.

Vaddi et al. [63] proposed an analytical model of conventional DG MOSFET having gate-source under lap. This model presents an efficient result for the reduction of subthreshold leakage current.

Tiwari et al. [64] used the virtual cathode approach to propose the analytical model of TM-DG MOSFET for the sub-threshold characteristics. P.Suveetha et al. [65] have adopted a similar mechanism to find the sub-threshold parameters of TM-SG MOSFET.

Kumar et al. [66] developed mathematical models for DG-GAA MOSFETs to represent the subthreshold swing and leakage current. The subthreshold current is calculated using Pao-Sah's formula. Quantum carrier confinement effect mechanism is added in the model due to the introduction of quantum effects in the device. The subthreshold swing is modelled using the virtual cathode method. This research paper also reported that the alteration in sub-threshold characteristics is observed with device design parameters.

Sonam et al. [67] have used the superposition method approach to develop a model of sub-threshold swing and sub-threshold current for (JLDSG) MOSFET. The effects of variation in channel length, silicon & oxide film thickness have also been studied for this junctionless double surrounding gate structure. The results obtained from this device structure are properly matched with the simulation results. These results show

superior performance for conventional junctionless surrounding gate (JLSG) device MOSFET.

B. Jena et al. [68] systematically analyzed the performance of an undoped CGAA MOSFET with different process parameters. In traditional MOSFET, channel doping is high to provide more current but causes more variation in threshold voltage. Hence, the undoped behaviour of GAA MOSFET solves the above problems. The result reveals that ultra-thin body and higher metal gate work-function can decrease the SCEs and consequently increase the performance. The proper selection of silicon thickness and gate work function can give the optimum value of the threshold voltage.

Vadthiya et al. [69] developed a 2D numerical analysis and analytical model for sub-threshold current, transconductance and surface potential. The underlap DM-DG MOSFET was utilized to enhance the RF and analog characteristics of Double Gate MOSFET. A significant reduction in sub-threshold current has been observed when underlap length increases due to the better control of the gate over the channel. DMG structure improves the analog figure of merit such as TGF, output conductance and gains frequency product, and also proves the general suitability of the DMG MOSFET for RF/ analog applications.

Kumar et al. [70] presented an evanescent mode analysis with a high-k dielectric to develop an analytical model for Schottky barrier (SB) CGAA MOSFET. The superposition method is used to find threshold voltage (V_{th}) and sub-threshold slope (SS) in this paper.

T.K. Chiang et al. [71] presented the sub-threshold behaviour model for DM-SG MOSFETs. The DM-SG MOSFETs show an excellent performance than their counterpart SM-SGMOSFET by reducing HCE and SCEs. The device can achieve good sub-threshold behaviour with a thin gate oxide and a thin silicon body. The superposition approach is utilized to deduce the threshold voltage and surface potential. The sub-threshold current and swings are also determined for DM-SG MOSFETs in this research paper.

Gautam et al. [72] developed an analytical model using the impact of localized charges for CG-GAA MOSFET. This model uses a charge dependency modelling approach to calculate the sub-threshold current.

Chiang et al. [73] developed a tri-material gate-stack SOI MOSFET device structure and proposed a model for its analytical sub-threshold behaviour, threshold voltage, electric field and surface potential using Superposition Method Approach. In the sub-threshold region, it is observed that the large L_1/L_2 ratio, thin silicon body and thin gate stack oxide provide excellent characteristics of the device in the sub-threshold region.

Rajendran et al. [74] presented an analytical model for FD double-gate SOI MOSFETs to find out Transconductance to Drain Current Ratio (TDCR) and body factor (*n*) and its influence on electrical characteristics. This technique is suitable for VLSI circuits having low power consumption where weak and average inversion is used. The dependence of TDCR on temperature is also considered. The result reveals that DG SOI MOSFET has a higher TDCR and optimum body factor values than conventional and SOI MOSFET.

Balamurugan et al. [75] explained a transconductance model for dual metal surrounding gate MOSFET. The surface potential is calculated based on boundary conditions derived for that particular MOSFET. TDCR value of DM-SG MOSFETs does not decrease as in the case of DG MOSFETs at small channel lengths and large thickness of oxide and film thickness. Hence, the transconductance generation efficiency of DM-SG MOSFETs is better as compared to DG MOSFETs.

Ortiz Conde et al. [76] described a model based on front and back surface potential to find out the transconductance for asymmetric double-gate MOSFET using a single equation. This model applies to all bias conditions. This model cannot be applied to the surrounding gate MOSFET due to its symmetrical structure.

Santosh Gupta and S. Baishya [77] presented the suitability analysis of cylindrical gates all around MOSFET. By using CGAA MOSFET, further downscaling of conventional MOSFET is possible with immunity against SCEs. At lower gate length,

it has high transconductance and small output resistance which makes it suitable for analog applications and low power applications.

P.Suveetha et al. [78] recently reported a model for triple material surrounding gate MOSFETs. The electric field distribution profile in TMSG MOSFETs is attained by solving Poisson's Equation. It is observed from the results that the device exhibits higher performance when the control gate is longer than the remaining gate lengths. The proposed models discuss the sub-threshold properties of MOSFET and its dependence on the dimensions of the gate oxide and silicon. The comparative analysis shows the TM-SG MOSFETs have a high value of TDCR as compared to DG MOSFETs.

Sonam et al. [79] proposed a Dual Metal Insulated Shallow Extension (DMISE) technique to reduce the problem of gate-induced drain leakage (GIDL) in CGAAMOSFET. The proposed device reduces the gate leakage current by reducing the valance band to conduction band tunnelling. The DMISE MOSFET as compared to traditional GAA MOSFET shows a large value of transconductance and drain current. It also achieves the ideal value of sub-threshold slope and large $I_{on}/_{Ioff}$ ratio.

Kranti et al. [80] presented an analytical model to enhance the transconductance for a Vertical Surrounding Gate (VSG) MOSFET. VSG MOSFETs obtained more transconductance values than DG MOSFET at all sets of device parameters. The results show that a reduction in silicon film thickness (t_{si}) is essential to obtain a larger value of transconductance. This model does not apply to triple material surrounding gate devices.

2.3 GATE DIELECTRIC ENGINEERING

A gate insulator can also be made with a high-k or the high dielectric constant oxide to inhibit direct tunnelling leakage current which arises due to downscaling of device dimensions. The study shows that substituting $SiO_2$with high-k materials with the same effective oxide thickness (EOT) increases state control over the channel and the device performance. A high-k dielectric with a thin interfacial oxide layer can be utilized to reduce the density of interface trap charge. Hence, it reduces the gate-

leakage, enhances the channel electric field and also improves carrier transportation efficiency [81].

Wong et al. [82] analyzed the importance of oxide thickness for future generation CMOS devices. The channel length has to be reduced for further downscaling of MOSFET. The downscaling results in an increase in gate leakage which further causes an increase in off current. Due to the increase in off current, device performance degrades. The gate and channel engineering will be the only solution to control the current in the deca-nanometer devices. The effective oxide thickness (EOT) has to be scaled aggressively to minimize the off current efficiently. The metal gate & high-k interface is not directly scalable is the major issue in the implementation of the MOSFET device.

S.K. Mohapatra et al. [83] presented the analytical model for the DG-GS MOSFET device. This research paper also includes the Channel and Gate Engineering in the DG-GS MOSFET for the improvement of device characteristics. The comparison of several of the above structures like Single Metal (SM) DG-GS, Dual Metal (DM) DG-GS and DM-SH-GS-DG MOSFETs were also carried out for the characteristics like transconductance, intrinsic gain, early voltage and transconductance generation factor (TGF). It has been observed that DM-DG MOSFET with gate stack shows better characteristics performance than SM counterpart in the research paper.

Nirmal et al. [84] reviewed the multiple high-k dielectrics over the DMG MOSFET. The dielectric such as HfO_2 has higher electron velocity (about 31%) in comparison to SiO_2 which enhances the carrier transport efficiency. The device characteristics of the MOS device like transconductance generation factor (TGF), DIBL and I_{on}/I_{off} ratio were analyzed for this dielectric. The DIBL of the MOSFET having HfO_2 as dielectric material is lower by the factor of 61.5% as compared to the DIBL of the MOSFET having SiO_2 as a dielectric material. TGF shows an improvement of 35%. The authors have utilized the high-k MOSFET to design a CMOS inverter which shows a reduction in delay and power dissipation

Frank et al. [85] analyzed the utilization of dielectric with high-k which can help for further scaling of MOSFET. This concept is introduced in DG MOSFET and shows improved performance of the device against multiple device characteristics.

Yeo et al. [86] described the future material for gate dielectrics. Leakage from the gate is the major issue in scaled devices. The existing SiO_2 should be replaced by an alternate gate dielectric which can be used for future devices. In this research paper, the different gate dielectrics are compared based on tunnelling effective mass. It has been observed that high-k gate dielectrics are suitable for low standby power techniques.

Zhang et al. [87] modelled the roll-off of threshold voltage using a high-k and gate stack structure. The proposed model considers the impact of the fringing field on single and double stacked-layer insulators. The introduction of the ultra-thin low-k layer in the mid of the substrate and high-k was found to improve the SECs.

Aniruddh et al. [88] presented a gate stack structure in which dielectric is made with high-k material and vacuum. The work reported that this device architecture minimizes the effects of impact ionization, BTBT and electric field towards the drain. This results in a reduction in SCEs. Using Poisson's Equation, an analytical model was developed for the junctionless cylindrical surrounding gate (JL-CSG) MOSFET. A comparison was made between JL-CSG, gate stack JL-CSG and CSG. The proposed device shows improvement in current driving capability and reduction in hot carrier effect.

Yeap et al. [89] analyzed the effects of high-k dielectric on MOSFET's turn-off/on characteristics. It was observed that the characteristics were deteriorating which may be attributed to fringes field effects and subsequently lowering of the barrier. The potential barrier lowering causes lower threshold voltage and enhancement in standby power. By using the interfacial oxide layer, FIBL can be reduced completely for $k \leq 25$.

B.C. Mech & J. Kumar [90] highlighted the important aspects of the selection of gate dielectrics to minimize the SCEs. The comparative study of silicon oxide (SiO_2), hafnium oxide (HfO_2), titanium oxide (TiO_2), lanthanum oxide (La_2O_3) and aluminium oxide (Al_2O_3)as gate dielectrics for scaled devices was carried out. The results show that titanium oxide is the best gate dielectric among all. However, its dielectric constant is high which causes an increase in capacitance and degrade the performance in ac analysis.

R. Gautam et al. [91] proposed a vacuum as the gate dielectric in the Gate-All-Around MOSFET. The RF performance of the proposed MOSFET is evaluated against the traditional gate-all-around MOSFET. It has been observed that GAA with VGD is much better than SiO_2 dielectric in terms of hot carrier reliability due to the low drain field. It is also reported that it suffers from poor current and transconductance. To improve these parameters, Gate and Channel Engineering were used which results in an overall improvement in device performance.

D.M. Thomas et al. [92] analyzed the effects of high-k gate dielectric on the MOSFET. The simulations and analytical study of the DM-DG MOS device are carried out for the characteristics like transconductance and surface potential. The utilization of dielectric with high-k materials results in a decrease of EOT. These MOS devices depict an enhancement in the analog performance. In the sub-threshold regime, this device shows a remarkable improvement in current by 5%. This device is also reported a 3% enhancement in transconductance.

Sonam et al. [93] proposed modelling for Dual-Metal Hetero-Dielectric (DM-HD) Cylindrical Gate-All-Around (CGAA) MOSFET. This model was developed by taking the impact of GIDL effects on the device characteristics. The device structure which was designed to decrease the off-state leakage current has a gate dielectric as a vacuum dielectric towards the drain end and SiO_2 towards the source end. The DM-HD-CGAA MOSFET device was reported with a lower off-state leakage current in comparison to traditional CGAA MOSFET. Leakage current analysis was done at elevated temperatures.

Vandana Kumari et al. [94] analyzed the numerical modelling of dielectric pocket double-gate MOSFET. The model involves 1D and 2D solutions for the device. The impact of interface charges on gate leakage current for DP-DG MOSFET was discussed in the literature.

Nidhi Singh et al. [95] developed an analytical model for TM GSDGMOSFET using Poisson’s Equation. The impact of dielectric thickness on the potential barrier has been analyzed in the reported work. The model for TM GSDG MOSFET was designed by taking adequate boundary conditions

2.4 CHANNEL ENGINEERING

The channel engineering is carried out to vary the doping profile in the channel using halo implants or pocket implants. Halo implants are basically of two types: symmetrical and asymmetrical. The device performance is affected when the depletion layers near to drain and the source extends towards each other and have the length same as the channel length L in scaled devices. Increasing the doping in the substrate region results in the reduction of the width of depletion layers and SCEs. On the other side increase in the substrate, doping causes an increase in threshold voltage and lowers the carrier mobility [96]. By increasing doping near to source side can reduce the SCEs without reducing the carrier mobility. These devices are known as Lateral Asymmetric Channel Devices. The surface potential decreases due to the incorporation of pocket implants in the MOSFET. These halo profiles introduce an extra step function in addition to steps produced due to gate-engineered structures. The benefit of reduction in surface potential is the reduction of the threshold voltage roll-off and DIBL. The extra benefit of using dual halo devices is the large doping at the drain side inhibits the field penetration from the drain side to the source side. Hence, the dual halo further reduces the DIBL and gives better control over the channel.

Sarkar et al. [97] presented a device that integrates the benefit of both Gate and Channel Engineering methods. This device is known as a Double-Halo Dual Material Gate (DH-DMG) MOSFETs. The pseudo-2D analysis was utilized to build the analytical model for sub-threshold surface potential. The Gauss's Law was applied to an elementary rectangular box in the depletion region of the channel. The accurate estimation of sub-threshold surface potential considers the channel depletion layer with diverging depth in association with the inner fringing potential in the drain and source. The same procedure is adopted to calculate the threshold voltage and sub-threshold behaviour for DH-DMG and Single-Halo Dual Material Gate (SH-DMG MOSFETs). DH-DMG MOSFET results in a better reduction of the SCEs in the entire pocket implanted MOSFETs.

P.Suveetha et al. [98] analyzed threshold voltage and sub-threshold current for Single Halo Triple Material Surrounding Gate (SH-TM-SG) MOSFETs by an analytical model using Parabolic Approximation Approach. By introducing halo in TMSG, the

roll-off of the threshold voltage is reduced which indicates a reduction in SCEs. The effect of dual halo on TM-SG was not described in this research paper.

S Baishya et al. [99] presented the sub-threshold potential model for dual halo MOSFET. This model consists of the impact of space charge region width near the drain and source junctions on channel depletion layer width. The surface potential is calculated using Gauss's law.

Zanchetta et al. [100] introduced halo doping in MOSFET to control the SCEs. A quasi- 2D model was developed and results show that the halo implant concept reduces the off current of MOSFET which is a preferred choice for low power circuits.

N. Mohan Kumar et al. [101] have applied Gate Engineering Technique along with lateral asymmetric halo doping in MOSFET. The dual metal gate MOSFET having halo doping was investigated for DIBL, drain current, electric field, transconductance and surface potential. The leakage current and SCEs in the device decreases due to the Lateral Asymmetric Channel (LAC). In this method, the channel doping near to drain end is lower than the source end, and it results in the sub-threshold leakage current reduction. SCEs characteristics are better taken care of in single halo dual metal DG MOSFET in comparison to Single Halo DG MOSFETs. The reported work does not have elaborative analytical modelling of the device.

Harshit Aggarwal et al. [102] have reported the anomalous behaviour of halo implanted MOSFET in linear and saturation regions for transconductance. The transconductance curve shows a sharp change of slope in saturation. The reason for this behaviour has been found out for halo and uniformly doped transistors. The impact of oxide thickness variation on g_{m} is also analyzed. The g_{m} characteristics using the efficient SPICE model are also proposed.

Li Cong et al. [103] developed a model of threshold voltage, electric field, surface potential and sub-threshold current for halo-doped SG MOSFETs. The threshold voltage shows higher accuracy than the Parabolic Approximation Method. The variation with device parameters i.e. the thickness of the oxide layer, the concentration of dopants and thickness of silicon were also discussed. The

mathematical model was described by using the superposition technique that consists of 1D and 2D equations. The proposed model seems to be complex and tedious to find out the solution.

Reddy & Kumar [104] have proposed Asymmetrical Single Halo Doped Double-Gate MOSFET. This work presents the simulation studies of the threshold voltage roll-off, DIBL and sub-threshold slope. The results of the simulation indicate the ASH-DG MOSFET has superior performance compared to a traditional DG MOSFET. The step functions in the surface potential are due to the existence of a single halo near to source side which protects the source from the variations in drain bias. The analytical model of the structure was not described in this research paper.

Luan et al. [105] developed an analytical model for asymmetrical Halo Dual-Material Gate (DMG) Silicon-On-Insulator (SOI) MOSFET. The halo doping is done near to source region. 2D Poisson's equation is applied to estimate the channel potential. The drift-diffusion theory was utilized for understanding the sub-threshold behaviour of the MOSFET. The model has limitations for the multi-gate device.

T.K. Chiang [106] developed a numerical model of asymmetrical dual-material double-gate (ADM-DG) MOSFETs for sub-threshold swing and threshold voltage. The device parameters such as gate oxide, thin-film and a small length of screen gate are preferred to suppress the SCEs. The superposition approach is also used to solve the model equation in the reported work.

Zunchao [107-108] carried out the performance analysis of Symmetrical Halo-Doped Cylindrical Surrounding Gate MOSFETs. The analytical model of threshold voltage and surface potential was developed by using Parabolic Approximation Approach. The symmetrical halo doping profile illustrates higher performance in quenching roll-off of DIBL and threshold voltage in comparison with Uniformly Doped Surrounding Gate MOSFETs. The reported model has constraints below 50 nm channel length.

Harsupreet Kaur et al. [109] have analyzed graded channel surrounding gate (GC-SG) MOSFET and developed an analytical model for the same. The low doping at the drain end in comparison to the source side increases the mobility and decreases the

electric field. The drain current model also incorporates DIBL and channel length modulation (CLM) for GC-SG MOSFET.

Amitava Das Gupta et al. [110] reviewed the short channel effects in traditional bulk MOSFET and SOI MOSFET with symmetric halo implant. The threshold voltage for DMG-SOI MOSFETs is calculated using the variable separation technique by employing suitable boundary conditions.

S. Baishya et al. [111] developed an analytical model for sub-threshold drain current of pocket implanted halo MOSFET. The 2D Poisson's Equation was utilized in the reported work to estimate surface potential. The model includes complex mathematical equations and is not suitable for surrounding gate MOSFETs.

P K. Sahu and S. Panigrahy [112] have analyzed DG MOSFET for DIBL, threshold voltage, sub-threshold swing (SS) and device on/off current. To further reduce these parameters, halo doping is used. The optimum MOSFET characteristics and reduced SCEs can be obtained by scaling silicon and oxide thickness down with L. The halo implant technique decreases the SCEs and enhances the device performance. The graded channel DM-DG MOSFET gives optimal cut-off frequency at reduced drain currents [69].

2.5 DEVICE ENGINEERING

Bulk MOSFET has existed in integrated circuits for more than five decades with every advancement in applications and more functionality per chip. The device density is increased by following Moore's law. The recent architectures of integrated circuits require MOSFET of very low technology nodes i.e. in tens of nanometres. When the conventional bulk MOSFET is scaled to these dimensions, the short channel effects (SCE) start to occur and heavily affect the electrical characteristics of the MOSFETs. To overcome and diminish the effects due to these SCEs, many alternate device structures were introduced. Silicon-On-Insulator (SOI) and junctionless (JL) MOSFET are assumed to be the best replacement of bulk MOSFET in the nanometre regime.

2.5.1 Silicon on Insulator (SOI) MOSFET

SOI MOSFETs are said to be the most potent device for the scaling of bulk MOSFETs due to their immunity to SCEs, exceptionally less subthreshold leakage current and inflated I_{ON} to I_{OFF} ratio. Although the development processes for SOI MOSFETs started in the early eighties. IBM Research Division launched a new program focusing on SOI-based CMOS device design and related material research in 1989 [113]. The application of high-k as gate material and scaling the device to an appropriate dimension provides further improvement in the current [114]. The gate work-functions engineering and careful silicon channel doping make the SOI MOSFET a superior device. Extremely small MOSFET device dimension requires the scaling in threshold voltage for low voltage operation of the device [115].

K.K. Young et al. [116] developed a realistic 2D analytical model of short-channel FD SOI MOSFET for threshold voltage by utilizing 2D Poisson's Equation. The proposed model has included the vertical field and lateral field effects under Parabolic Potential Profile Approximation.

Shur et al. [117] proposed an innovative concept of split-gate structure. Later on, the Dual Material gate structure was based on this concept of applying different gate-bias in split-gate. However, this concept had the limitation of handling the fringing field capacitance between the two amalgamated metal gates which increases with the decrease of separation between the two gates. Some asymmetric structures were reported in [118-119] in which the channel field distribution was assumed to be continuous.

Wei Ma and Savas Kaya [120] analyzed a DG SOI MOSFET structure and measured the impact of device physics on the structure to compare the performances of the said structure with that of bulk MOSFET in terms of the output conductance, transconductance and drain-to-source current.

Mohan Kumar et al [121] analyzed a Gate Engineering Technique where a single gate is formed by merging the two metals of unlike work function. DMG nMOS is created by keeping the high work function metal towards the source and low work-function

metal towards the drain. This arrangement of gates increases the velocity of the electrons and gate transport efficiency.

Veerraghavan and Fossumet al. [122] developed a charge sharing model which predicted threshold voltage dependence. In this model, the surface potential was assumed to be constant and thus independent of drain potential. However, this model does not include the important issue of DIBL and also the front and the back gates have a coupling effect.

Samad Ghalandari et al. [123] reported a new structure for FD SOI MOSFET at 30-nm technology to improve the DIBL parameter as well as to enhance the self-heating effect. The structure has a varied thickness of the Buried Oxide (BOX) layer in the transistor to improve the DIBL parameter and self-heating effect. Due to changes in the thickness of silicon oxide from 0.1 micron to 30 nanometers, the maximum temperature of the channel was decreased which result in a reduction in the rise in thermal activity of the MOSFET.

DG SOI MOSFETs are significant device structures because of the reduced impact of SCEs and the fabrication processing steps similar to bulk CMOS. It is always in research for the performance augmentation of analog circuits. Although SOI features significant performance improvements over conventional bulk MOSFETs but SOI is not fully immune to SCEs. Hence, the other device structures were explored along with improving the SOI by applying Channel or Gate Engineering. Junctionless FET is one such reported structure.

2.5.2 Junctionless Field Effect Transistor

Gate-all-around devices were developed as the scaling of the other structures under 45nm increases SCEs and static leakage current. Hence more attention was provided to research multi-gate structures/ pi gate and gate-all-around MOSFET, to improve SCE and DIBL. With the scaling of devices, the fabrication steps like the creation of very thin junction and annealing result in complex and costly processing. Hence, the alternate strategy to create a semiconductor device that includes a single material uniformly doped channel from source to drain among others was developed. These single material uniformly doped channel devices are known as junctionless transistors

(JLT) as no junction between drain/ channel and source/channel exist, unlike conventional MOSFETs.

JLTs have electrostatically depleted channels in which the variation of the difference of work-function between channel and gate is used to turn on/off the device. JLTs are a unique kind of device due to the absence of abrupt doping in source/channel and channel/drain interfaces, unlike conventional MOSFETs.

Bulk planar JL-FETs are upcoming devices offering advantages over bulk MOSFET. Their doping profile is uniform throughout the body, but these devices have high doping concentrations. The absence of junctions makes the devices have insignificant SCEs. The off current of these devices is very low.

Various researches have been carried out to study the leakage current mechanism and other characteristics in MOSFETs.

J. P. Colinge [124] demonstrated that the MOS device is a variable resistor where the charge carrier density varies with the applied voltage on the gate terminal. The in-work-function difference between the gate material and semiconductor depletes the charge carriers to turn the device off. The high doping concentration of majority charge carriers assists in high current flow during the on-state.

N. Jaiswal et al. [125] developed a quasi-analytical model for short-channel JLT devices to study the effect of gate-source/drain underlap on the device. The reported work has channel potential represented in the five regions equivalent model in the sub-threshold regime of DG-JLT for the symmetric mode of operation. The model is verified by the numerical simulation using the TCAD tool.

Kathy Boucart et al. [126] have proposed the optimized performance model for DG-TEET. The reported work also includes the operation of DGTEET in greater detail and optimized device designing with the high-k dielectric material.

Qian Xie et al. [127] presented an analytical model by solving 2-D potential equations for DG-JLT. The various parameter of the device was validated by numerical simulation using TCAD tools. The literature reports that the SCEs in JLT

get reduced and the performance of the device increases with increased doping of the channel.

A. Gnudi et al. [128] proposed the analytical model for the electrical properties of JLT. The cylindrical device design is considered for modelling. The literature recognizes the variability of the device and parasitic resistance are the constraint for device characteristics.

C. W. Lee et al. [129] analyzed the deviation of electrical parameters with temperature for the conventional MOSFET and JL MOSFETs. The numerical simulations for the devices were also carried out. The reported work also shows that JLT devices achieve fully depletion-mode when the work-function of the gate materials is above 5.0eV.

K. P. Londhe et al. [130] developed a model for the double-gate junctionless transistor to model SCEs in JLT. The reported work also includes the design of the JLT device using Germanium to improve the various device parameters like GIDL and DIBL.

R. Rios et al. [131] compared the junctionless transistor and traditional tri-gate transistor at the shorter channel length. The various SCEs were found to be better suppressed for JLT devices in comparison to difficult to fabricate tri-gate MOSFET with the same kind of parameters.

N. Gupta et al. [132] presented the simulation studies to represent the difference in SCEs of JLT conventional MOSFETs. The simulation was carried out in the Silvaco's TCAD tool. The simulation demonstrated the supremacy of JLTs over conventional MOSFETs.

Y. Taur et al. [133] presented the comparison of JL MOSFETs and DG MOSFETs based on charge characteristics. The research paper includes the analytical model of JL MOSFET by utilizing 2D Poisson's Equation. The analytical model shows the effects of dopant concentration variation on the threshold voltage of junctionless MOSFETs.

Yongbo Chen et al. [134] analyzed the junctionless MOSFET by applying higher doping towards the drain end. This results in the improvement in transconductance,

operating frequency and gain, etc. The processing of the device becomes complex but the characteristics parameters improvements are beneficial for RF application of junctionless MOSFETs.

Suresh Gundapaneni et al., [135] demonstrated the bulk planar junctionless transistor in which the silicon-only device is created in place of a buried oxide-based device. The JLT devices are made with a high doping concentration in the channel region. The high doping in these devices forces the bands to overlap. Hence it causes Band to Band tunnelling (BTBT) among the drain and the channel. This BTBT causes an increase in off current. BP JLT devices have reduced the impact of BTBT and have a high on to off current ratio. The reported work also compared the BPJLT device against SOI JLT for various parameters like SS and DIBL.

It can be concluded that Junctionless FET offers exciting features as the scaled device and hence it will be the prominent structure for the replacement of bulk MOSFET.

2.6 TECHNICAL GAPS AS OBSERVED IN THE LITERATURE

From the different approaches applied to the devices to improve their characteristics which were discussed in the previous section, it was observed that Junctionless MOSFET is a prospective device due to the multiple advantages associated with it. It was also observed that many approaches which include gate engineering, gate dielectric engineering and channel engineering have been applied on various devices resulted in better performance in terms of immunity against short channel effects (SCE) at the cost of fabrication complexity. However not much research to improve the device characteristics by applying gate engineering (using multiple gates) along with gate dielectric engineering is available for Junctionless MOSFET devices. It shows the path of the research could be aligned on these aspects to improve the further immunity against SCE for the Junctionless MOSFET.

2.7 CONCLUSION

In the literature, there are many instances where selecting a high-k dielectric in place of SiO_2 has resulted in better device characteristics for different applications. Since the adhesive properties of the alternate high-k material are generally poor [136] so it

would be beneficial to use this alternative high-k dielectric along with a layer of SiO_2 to have better physical and thermal stability of the device. DGMOSFET has a reputation because of its resistance to SCEs and similarity to the bulk planner for processing. Hence, the research on DGMOSFET is quite critical. As emphasized in multiple works of literature [20, 70, 77, 81, 92, 104], the integration of high-k with DGMOSFETs will make them more applicable for low power and sub-threshold design. The obvious benefits for SOI MOSFET may also be considered for designing these MOSFETs. Moore's law is compelling the design engineers to shrink the device size further to fit in more devices per unit area. The scaling not only induces SCEs but also creates difficulty while fabricating the devices. As already discussed the junctionless transistors offer the advantages of simple processing steps close to CMOS processing and also proved to be highly immune to SCEs [128-130]. The integration of high-k along with JLT is expected to be a beneficial design for the future generation of scaled devices.

CHAPTER –III

ANALYSIS OF DOUBLE GATE SOI MOSFET

3.1 INTRODUCTION

The world has seen unprecedented growth in the use of integrated circuits in computing and all other allied engineering fields. This growth is directly related to advancement in the field of integrated circuits in terms of size (more semiconductor devices per unit area), power dissipation and computing performance. For fulfilling International Technology Roadmap for Semiconductor (ITRS) requirement for future generation devices, the researchers have stepped into the area of nano-technology and deep submicron region of operation [23]. The high demands for low-power integrated circuits have increased with the widespread use of portable hand-held devices that are powered by limited capacities batteries.

The integrated circuits had rigorously followed Moore's law from the last half of the decade which talks about doubling the device density in every one and half years. The ITRS which provides the direction to future devices and integrated circuits predicts that very soon the physical length of the device will be of few nm [10]. The researchers are working hard to implement this prediction into reality. The Integrated circuits with more than 9.2 billion transistors in a single chip are already reported [135] which is possible due to the aggressive scaling of semiconductor devices. The scaling as already discussed is the process used to implement the future generation of devices by reducing their dimensions. Hence the number of gates per unit chip area is constantly increased over the years since the inception of integrated circuits.

During the process of scaling not only the size of the device is reduced but modifications in structural and electrical characteristics are also carried out to enhance the performance of the scaled device. The main objective of scaling is to make the device smaller than the earlier generation of devices and make more devices in the given area of integrated circuits. Figure 3.1 below shows the instance of the scaling process of the MOSFET.

3.2 TECHNOLOGY COMPUTER-AIDED DESIGN (TCAD)

The integrated circuits and semiconductor devices are developed and optimized using computer simulations. Technology CAD simulation tools give the numerical solution of complex device model equations for different geometries of a semiconductor device. Numerical simulations are a widely used and approved approach for device research. The semiconductor industry depends heavily on various simulation tools to enhance research, reduce the time and costs involved in the device development as technology approaches in nano-scale.

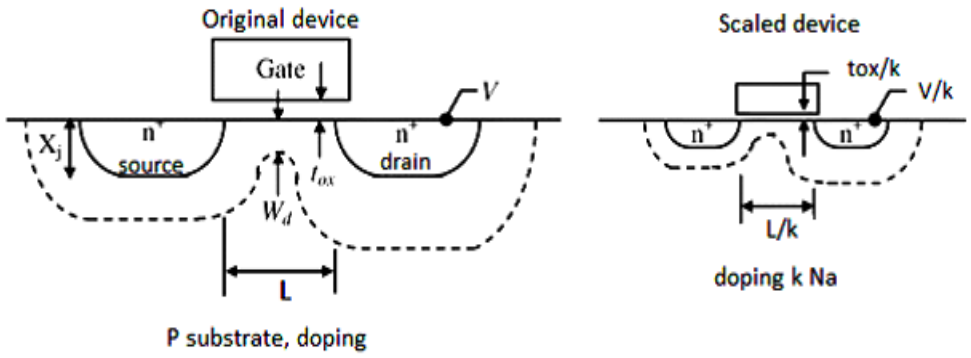

Figure 3.1: Scaling of MOSFET [113]

The semiconductor manufacturers utilized these tools for optimizing their integrated circuits process flows and their variation. TCAD tools can be divided into (i) Process Simulators (ii) Device Simulators.

3.2.1 Process Simulators

The various processing activities are simulated according to the governing model in process simulation which is carried out by process simulators. This simulation involves steps viz. deposition, etching, ion implantation, annealing and oxidation. The meshing which is the first step is done in a silicon wafer to create a basic element structure.

3.2.2 Device Simulators

The electrical characteristics of the semiconductor device are analyzed using device simulators. A mesh of a finite number of elements is created to analyze electrical field, potential and carrier concentration at these elements.

The device simulator provides the solution of Continuity and Poisson's Equation. After solving these equations, the electrical characteristics of the device are extracted. In the present work is a simulation is carried out using the Silvaco's TCAD package, where ATLAS works as a device simulator and is used to predict the electrical behavior of semiconductor devices. ATLAS works along with process simulator Athena tools and other TCAD packages as depicted in Figure 3.2 [33].

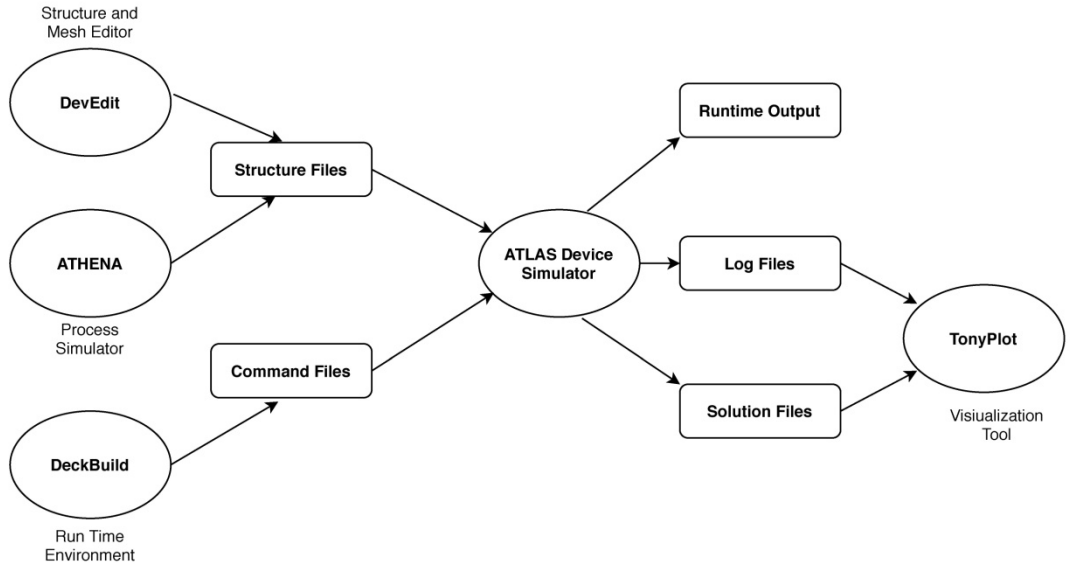

Figure 3.2: Flow of data in SILVACO TCAD TOOL [33]

ATHENA is a process simulator, which is used to make the structure of the semiconductor device. This structure acts as input to ATLAS. The outputs of the ATLAS may be taken to Mix-mode, a circuit simulator or UTMOST device characterization tool. The ATLAS accepts two types of inputs for simulation: i) command file ii) structure file.

The ATLAS tools produce output files as run time output, solution file and log file. The run time output gives the status of the current execution with errors and warnings.

The log file predicts the electrical behavior of the device. The solution file creates a device structure for parameters analysis. The log file and the solution files can be plotted and figured on TONY PLOT. It is also used to extract the data from the simulation result.

3.3 METHODOLOGY USED FOR SCALING

The devices on which the scaling is carried out for performance enhancement must undergo some experimental and theoretical analysis for the validity of expected objectives. The integrated circuit devices are established by process simulation where the physical processes are modeled to examine the effect of the environmental parameters on the devices.

The reported work describes the bulk MOSFETs having a channel length of 200 nm, 90 nm and 65 nm and 32nm using the numerical simulation for the extraction of MOSFET device parameters like V_t, Sub-threshold slope (SS), I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio using TCAD tools.

3.4 EFFECTS OF SCALING ON MOSFET

The scaling which is carried out to reduce the size of the semiconductor device is a complex process when the channel length runs in the nano regime. The scaled devices are not only difficult to process but also raise issues of short channel effects. These SCEs degrades the performance of the device.

3.4.1 Device Parameters under Analysis

The scaled MOSFET structures characteristics are defined using many device parameters such as sub-threshold slope, transconductance and threshold voltage. The electrical parameters which are analyzed in the present study include (i) Sub-threshold slope (ii) Threshold voltage (iii) On current (iv) Off current (v) On to off current ratio.

3.5 NUMERICAL SIMULATIONS OF BULK MOSFET STRUCTURES

ATHENA, the process simulator was utilized to obtain a numerical simulation of the MOSFET device at various technology nodes. NMOS devices at 200nm, 90nm, 65nm and 32nm were simulated by undergoing various virtual fabrication steps. The final structure after the simulation is obtained on Tony Plot Tool.

3.5.1 Planar NMOSFET Design at Different Node

Figure 3.3 shows the simulated structures of N-MOSFET with a gate length of 200nm, 90nm, 65nm and 32nm. MOSFET in all the structures is created by implanting boron having the doping density of $1e^{17}cm^{-3}$ and phosphorus to create n-type S/D regions with doping density in the range of $1e^{20}cm^{-3}$. The oxide thickness is kept at 2nm. The work function of the gate is 4.5eV.

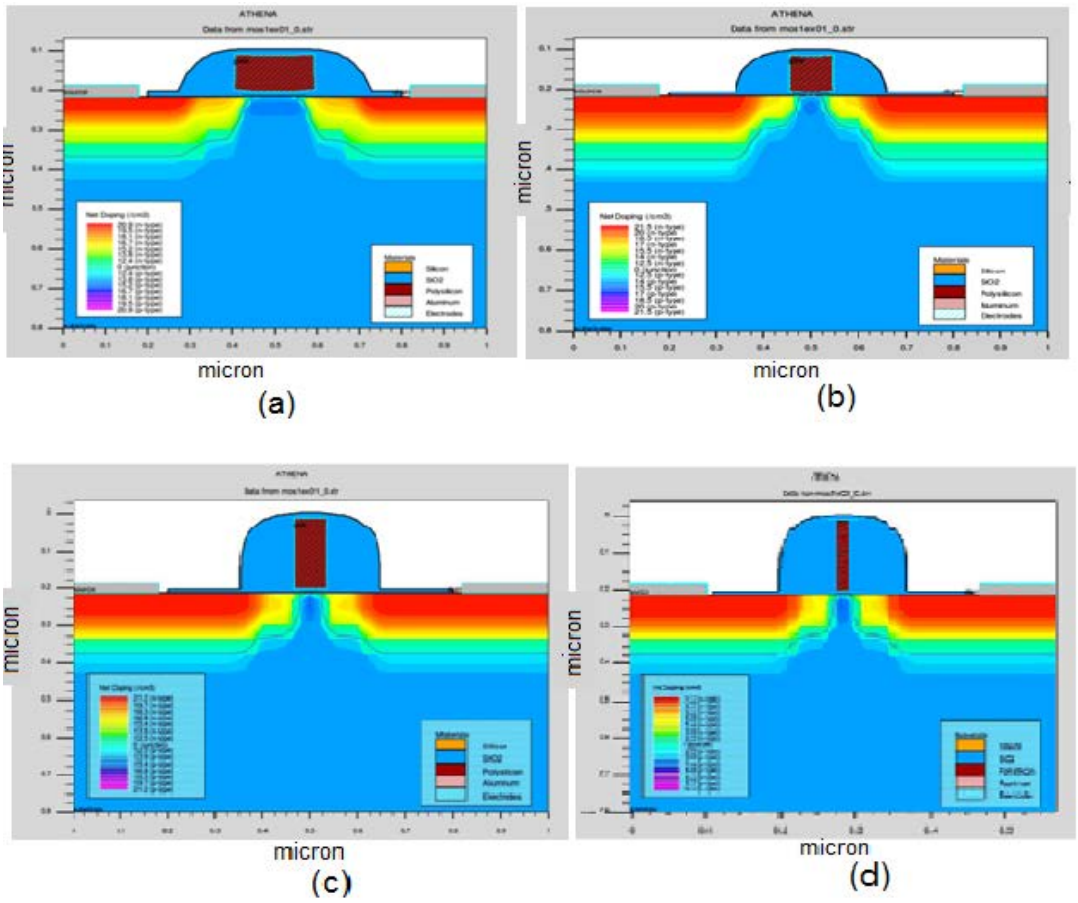

Figure 3.3: Simulated structures of NMOS at (a) 200nm (b) 90nm (c) 65nm and (d) 32nm

Figure 3.4 plots transfer characteristics for NMOS at 200nm, 90nm, 65nm and 32nm at V_{DS}=0.1 volt. Figure 3.5 plots transfer characteristics for 200 nm, 90 nm, 65nm and 32nm nodes. The Transfer characteristics are used to obtain the sub-threshold slope (SS). The values of the SS are 0.1021V/decade, 0.1272V/decade, 0.1534V/decade and 0.176 V/decade respectively for NMOS at 200nm, 90nm, 65nm and 32nm. The

calculated threshold voltages are 0.36V, 0.22 V, 0.2009 V and 0.188 V respectively for NMOS at 200nm, 90nm, 65nm and 32nm.

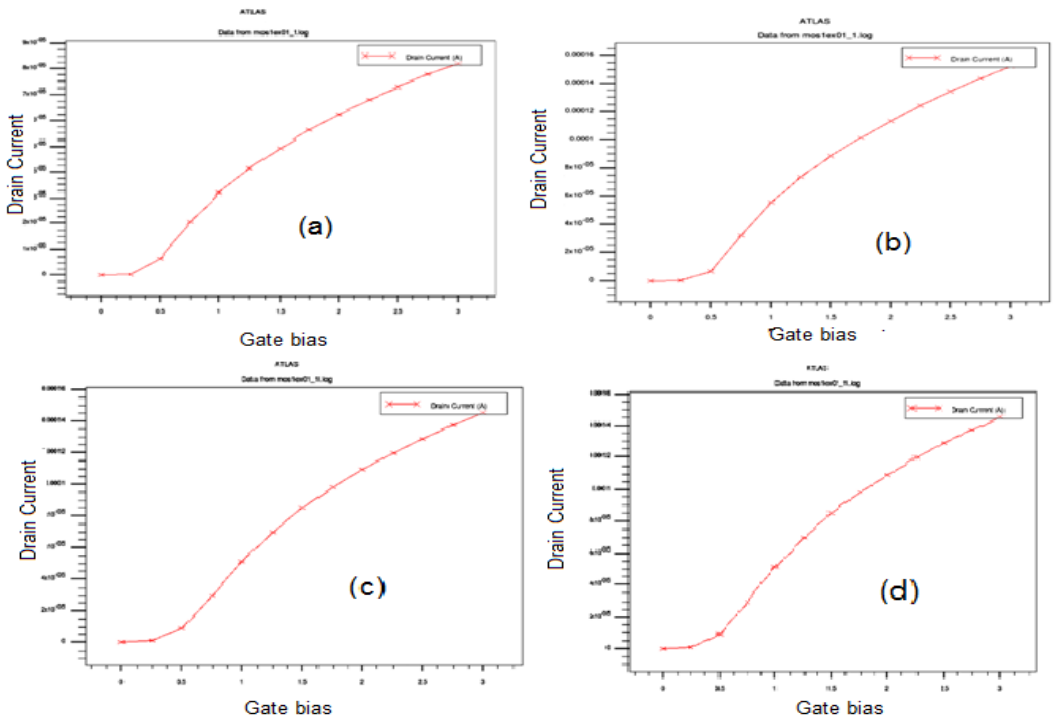

Figure 3.4: Transfer Characteristic of NMOS at (a) 200nm (b) 90nm (c) 65nm and (d) 32nm channel length

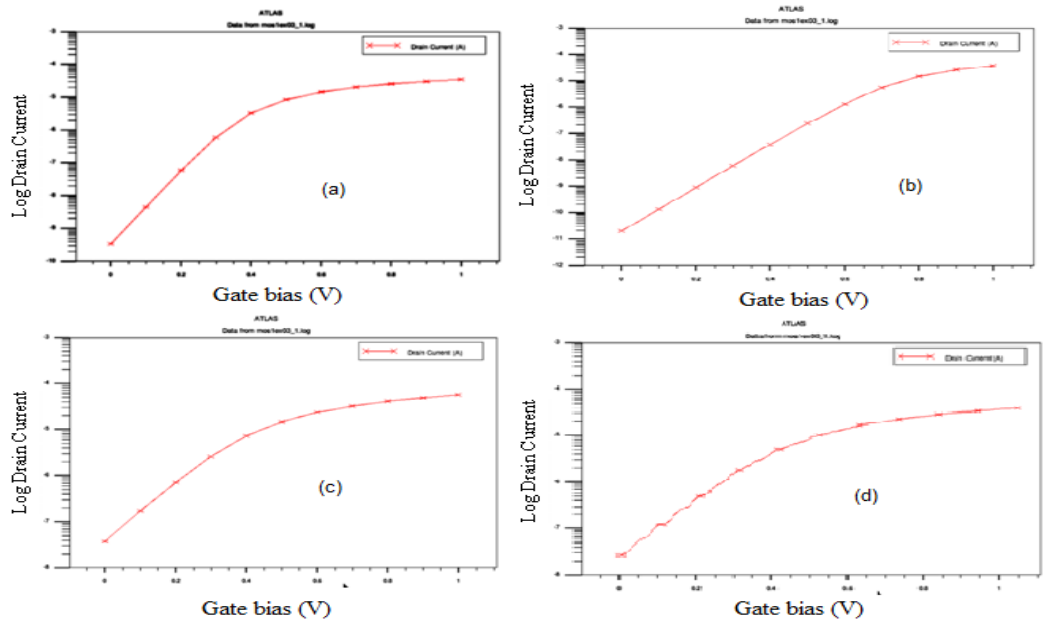

Figure 3.5: NMOSFET transfer characteristics (log) plots for (a) 200nm (b) 90nm (c) 65nm and (d) 32nm channel length

Table 3.1 shows various extracted parameters from the numerical simulations of N-MOSFETs on using Silvaco's TCAD for node technologies mentioned above.

Table 3.1**:** Extracted parameters of NMOSFET for different technology node

Parameters	**200 nm**	**90 nm**	**65nm**	**32 nm**
Sub-threshold Slope (v/decade)	0.1029	0.12731	0.151976	0.176
Threshold Voltage	0.36 V	0.22 V	0.2009 V	0.188 V
I_{ON}	$1.8e^{-04}$A	$1.76e^{-04}$A	$1.6e^{-04}$ A	$0.7812e^{-04}$ A
I_{OFF}	$1.946e^{-10}$A	$1.1958e^{-09}$A	$0.9e^{-07}$A	$1.1803e^{-06}$A
I_{ON}/I_{OFF}	924873	147167	1856	661.8

3.5.2 Variation in Different Parameters with Scaling.

i) Variation in threshold voltage with Channel length

With the reduction in channel length, the threshold voltage also reduces as observed in figure 3.6. The decrease in threshold voltage (V_{th}) with the decrease in channel length is called V_{th} roll-off. This decrease in threshold voltage may be attributed to the existence of SCE in the short channeled MOSFET device [29]

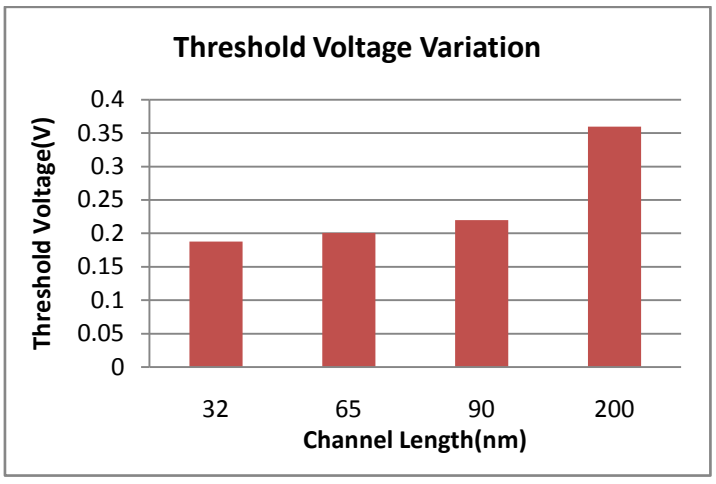

Figure 3.6: Threshold voltage variation with channel length

ii) Variation in Sub-threshold Slope with Channel length

The value of the sub-threshold slope reflects the speed of the MOSFET device. It shows how speedily a MOSFET can be turned off when the gate voltage decreases below the threshold voltage. It has been observed that with the decrease in channel length there is an increase in subthreshold current and sub-threshold slope. Figure 3.7 plots the subthreshold slope variation with different channel lengths.

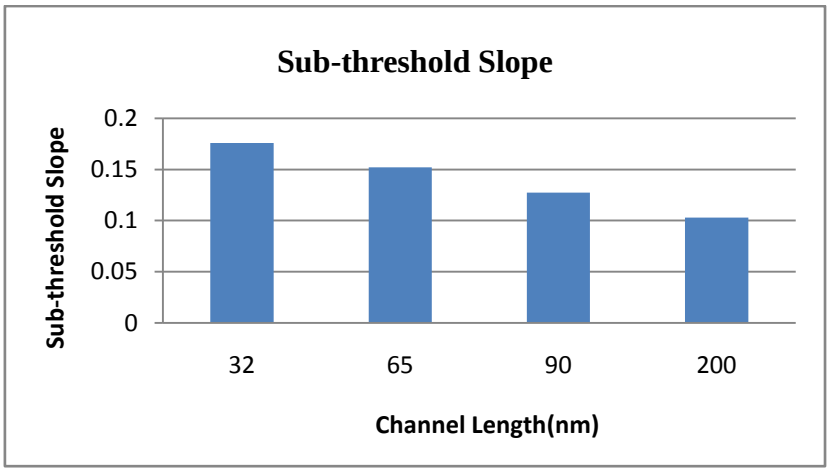

Figure 3.7: Sub-threshold slope variation for channel length

iii) Effect of Channel Length on I_{ON}/I_{OFF} Ratio

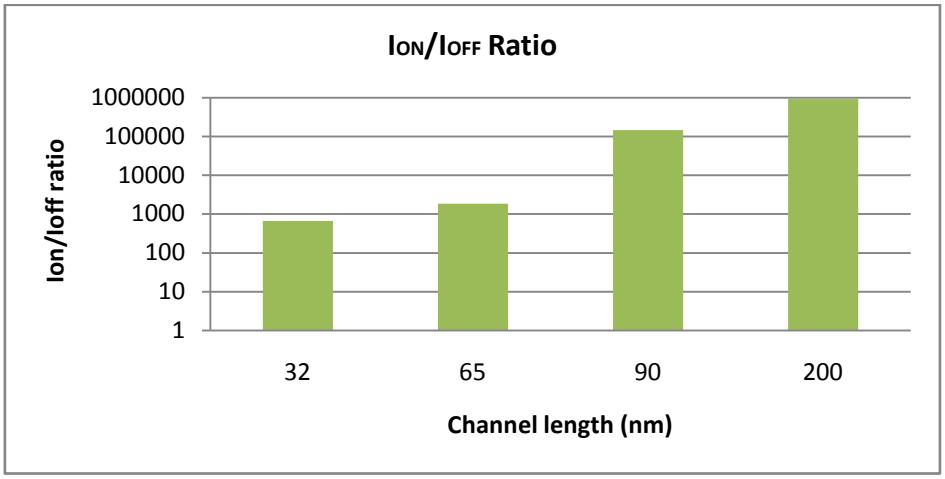

Figure 3.8: I_{ON}/I_{OFF} variation with different channel length

The I_{ON}/I_{OFF} ratio or on to off current ratio shows the effectiveness of the MOSFET when it is perfectly on and perfectly off. When I_{ON}/I_{OFF} is high it shows the device has a maximum on current and minimum leakage current. Table 3.1 depicts that I_{ON} is

almost the same. However, the value of I_{OFF} increases when the channel length is reduced. This fact can be attributed to SCEs. The leakage current component increases when the separation in drain and source decreases. Figure 3.8 shows the variation of I_{ON}/I_{OFF} with channel length.

3.6 CONCLUSION FROM SCALING

The study of scaling was carried out for various electrical characteristics and performance comparisons of N-MOS devices at various technologies using the SILVACO T-CAD tool using numerical simulation. When the channel length decreases the threshold voltage decreases, and I_{ON}/I_{OFF} ratio decreases but the sub-threshold slope (SS) increases. The MOSFETs are the key components of an IC. The aggressive scaling of the MOSFET is carried out over the years which mean the channel length is reduced with time. To make the integrated circuit future-ready, the dimensions of the MOSFETs have to be reduced. The above study shows all the factors going against the ideal characteristics of the MOSFETs with the decrease in channel length or when the scaling is carried out. Hence, it is very important to employ other techniques to improve the performance of the MOSFET at a lower technology node.

3.7 LIMITATIONS WITH DEVICE MINIATURIZATION AND ALTERNATE DEVICE DESIGN APPROACH

Contemporary electronics instruments have integrated circuits as the fundamental building block. The performance enhancement of these ICs is a continuous process. The continuous improvisations in scaling and the number of devices on an IC have given a tremendous boost in the computational ability to consumers at a minimal cost. Preserving the transistor performance with scaling down was the key to microelectronics technology evolution and its success. The scaling down process increases the circuit speed while reducing the cost drastically. Device miniaturization involves several complications including the fabrication and characterization of the miniaturized devices. With the shirking device dimension, the basic fabrication steps become difficult to be performed.

Scaling down a device leads to various short channel effects (SCEs). With the decrease in channel length, the gate loses control over the channel region as a result of enhanced sharing of charge by drain/source. This results in threshold voltage reduction. The salient short channel effects observed in a miniaturized device are the hot-carrier effect and DIBL along with threshold voltage roll-off. For the last few decades, the research efforts in the field of MOSFET mainly deal with finding novel methods of preventing short channel effects. Many solutions to reduce these SCEs were proposed by various researchers [51,100,137-139]. One of the efficient solutions is the reduction in the effective thickness of gate oxide by keeping physical thickness same various means. The next section of the work deals with this aspect of the solution for SCEs.

3.8 HIGH-k GATE MATERIALS

The down-scaling rules require a simultaneous decrease in thickness of gate-oxide and enhancing the doping in the substrate to eliminate the drain influence in the gate region. To provide current driving capability in MOSFET, a high C_{ox} (or small t_{ox}) is desirable [5]. A problem here is that the oxide thickness needs to be about 1nm. Even if an almost perfect oxide of 1nm thickness was technologically available, the electrons would tunnel through the 1-nm barrier [13]. The possibility of a large gate/substrate tunnel current exists due to the reduction in thickness of gate oxide to a few nanometres (10-20 Å) [13]. It will stop the further scaling of the oxide thickness with a channel length below 10 Å. If the gate oxide thickness is reduced below this value then the tunnelling current will reach over $100A/cm^2$ [13]. It will create a barrier in the working of highly efficient devices. With such a high gate-current, the problem with power dissipation would re-appear in another form.

The solution to the above concern exists in the usage of high-k materials to replace SiO_2 in the MOS technology. Better control over the channel region by the gate voltage can be obtained by increasing the permittivity rather than decreasing the thickness of the oxide. The dielectric materials with very high permittivity compared to silicon dioxide exists. The same field strength could be achieved with much thicker dielectric layers by using high-k dielectric materials. The thicker dielectric layer over the gate will decrease the device off current and will enhance the reliability of the gate dielectric [140].

Therefore, in the direction of attaining further scaling the researchers are working to attain performance improvement of the device by applying high-permittivity dielectric materials as gate oxide like hafnium oxide (HfO_2).

The capacitance of the high-k material gate for a MOSFET with thickness $t_{high\text{-}k}$ is

$$C_{ox} = \frac{\varepsilon_o A k_{high\ -k}}{t_{high\ -k}} \quad (3.1)$$

Where high-k dielectric material permittivity is represented as k_{high}, ε_o is the free space permittivity, t_{high} is the gate dielectric material thickness and area of the conducting plates is represented by A. From the above relationship for the same C_{ox}, the t_{ox} or effective oxide thickness is expressed as

$$t_{ox}\,(\text{Effective oxide thickness}) = \frac{k_{SiO_2}}{k_{high\ -k}} t_{high\ -k} \quad (3.2)$$

HfO_2 or Hafnium oxide is an inorganic compound having a relative permittivity of k ≈25. The band gap for HfO_2 is 6eV and it has low thermal expansion and high inversion temperature coefficient. The boiling point is 5400ºC and the melting point is 2758ºC. It has a molecular weight of 210.49 g/mol and a density of 9.7 g/cm^3 [84]. It is found in the form of a crystalline solid and has a dielectric constant of about 5-6 times higher than that of SiO_2 (k ≈3.9).

It can be calculated from the above equation (3.2) that to produce the same oxide capacitance as 1nm of SiO_2 a 6nm thickness of HfO_2 is required. Many other high-k materials like aluminium oxide (Al_2O_3), ZrO_2, etc are also analysed by various researchers. [81, 84].

The major disadvantage with high-k materials has always been the issue of much poorer adhesion properties of high-k films with silicon as compared to native silicon-silicon dioxide interface. These materials have an affinity to adhesion with low band gap. Due to which these materials become inefficient in reducing gate leakage. The excellent property offered by silicon dioxide outweighs the comparative disadvantage of low dielectric permittivity.

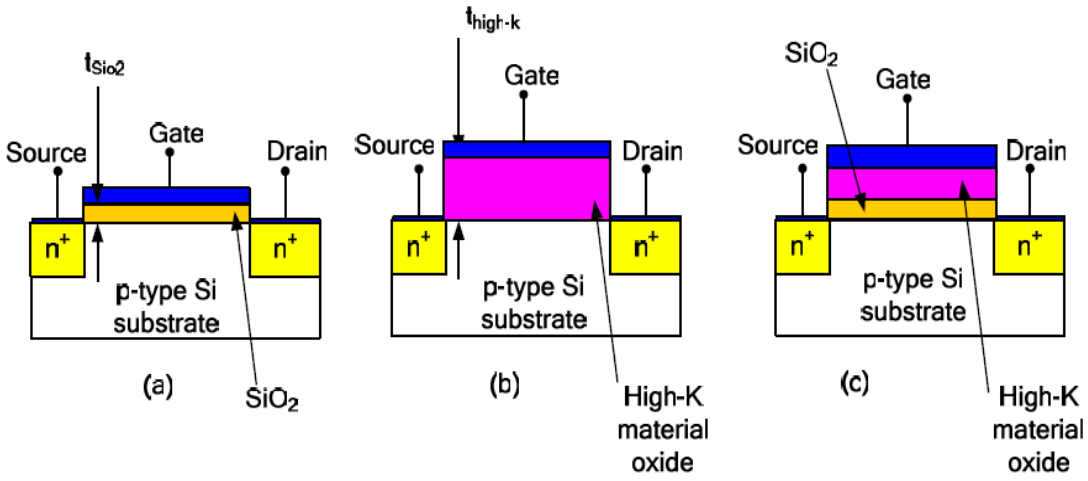

Figure 3.9: Cross-sectional structure of bulk NMOS having gate dielectric as (a) SiO_2 (b) High-k (c) Gate stack of High-k +SiO_2.

The materials with a very high permittivity of >50 exist. However, these are not chosen in the present work because of the 2-D associated effects and with very high permittivity the capacitance (CV/I) is negatively affected [136]. Due to these reasons, much of the research is constraint with high-k of permittivity in the range of 20. However, to reduce the hot-carrier effects advanced innovative techniques and novel architectures involving stack architecture in which high-k material is deposited over SiO_2 are now given extensive consideration [86]. Stack architecture is also reported to have improved carrier mobility [81]. The HfO_2 is the preferred choice as high-k dielectric material as the energy band gap of HfO_2 (6eV) is matched with SiO_2 (9eV) and HfO_2 is thermodynamically more stable on Si than any other high-k material for forming gate oxide stack structures.

3.9. NUMERICAL SIMULATION OF HIGH- K DIELECTRICS MOSFET

The numerical simulation of MOSFET at 32nm technology node is carried out using the Silvaco's TCAD tool. The structures considered for numerical simulations are having the gate oxide as SiO_2, HfO_2 and stack architecture of SiO_2 and HfO_2. These numerical simulations are done with the intention to analyse the characteristics of the device.

3.9.1 NMOSFET at 32 nanometres with SiO_2 as Dielectric Gate Material

Figure 3.10 shows the bulk MOSFET with 32nm with SiO_2 as a dielectric material

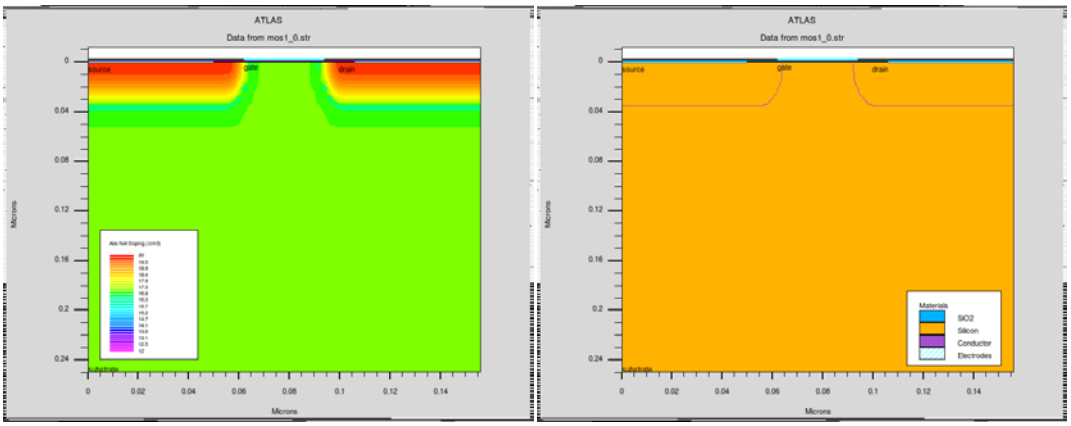

Figure 3.10: 32nm Bulk N-MOSFET a) Material view and b) Doping density view

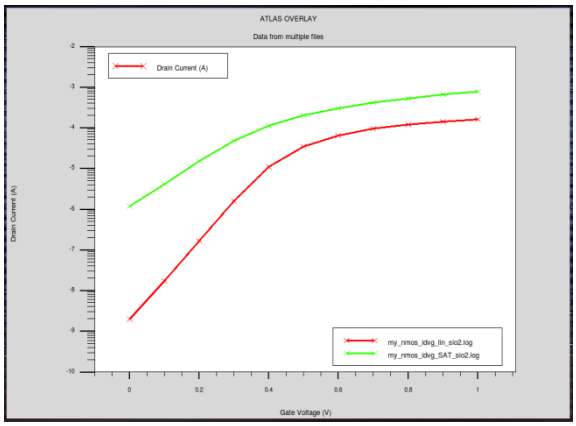

Figure 3.11: Transfer characteristics for bulk MOSFET with SiO_2 as the dielectric.

The transfer characteristics are shown in Figure 3.11, which is essential for the prediction of on/off current and sub-threshold characteristics of MOSFET. The saturation (high V_{DS}) characteristics are shown with a green line and linear (low V_{DS}) characteristics are shown with a red line.

3.9.2 NMOSFET at 32 nanometres with Multi-oxide (SiO_2+HfO_2) as Dielectric Gate Material

Figure 3.12 shows the bulk MOSFET with 32nm with multi-oxide (SiO_2+HfO_2) as dielectric material in stack architecture, to improve the adhesion of the high-k material (HfO_2) with the silicon substrate.

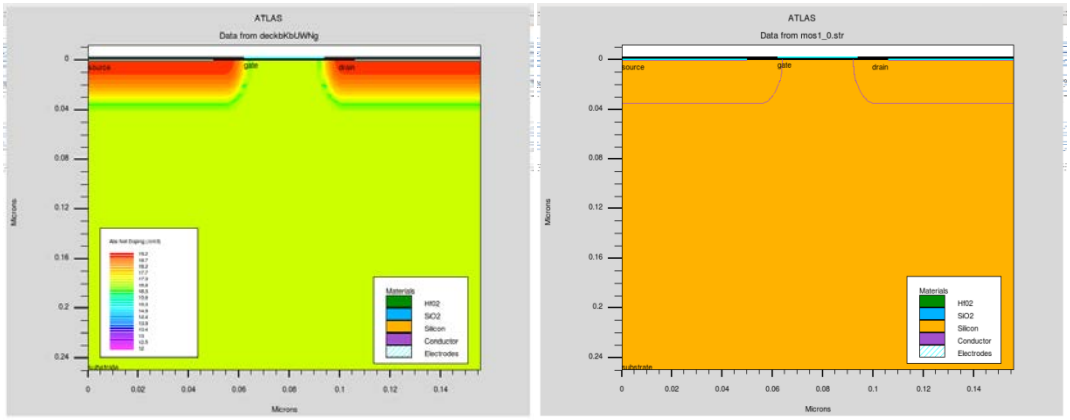

Figure 3.12: 32nm Bulk N-MOSFET a) Material view and b) Doping density view using multi oxide (SiO_2+HfO_2).

The closer architecture of the gate is shown in figure 3.13. The green layer (HfO_2) can be seen lying on the blue layer (SiO_2).

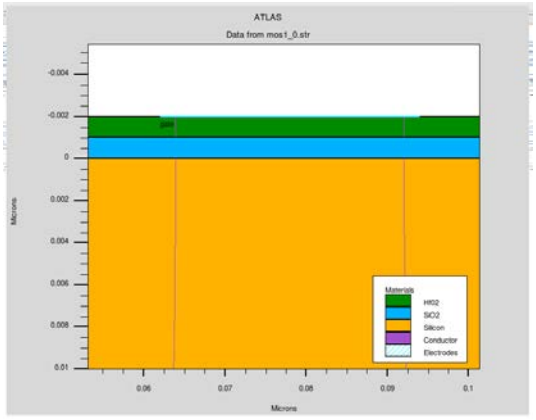

Figure 3.13: 32nm Bulk N-MOSFET with multi oxide stack architecture.

Again like the previous architecture, the transfer characteristics are shown in figure 3.14 which is essentials for the prediction of on and off current and sub-threshold

characteristics of MOSFET. The saturation (high V_{DS}) characteristics are shown with a green line and linear (low V_{DS}) characteristics are shown with a red line.

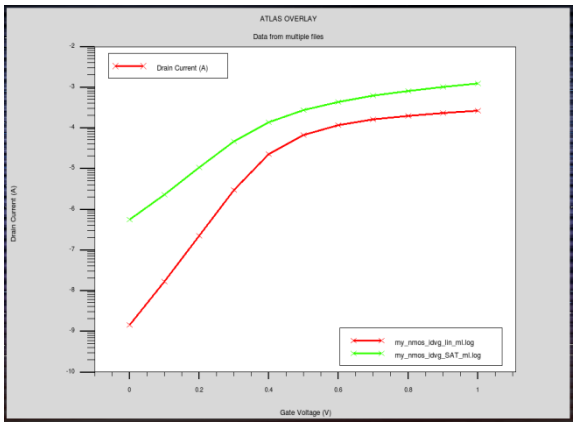

Figure 3.14: Transfer characteristics for bulk MOSFET with multi oxide as the dielectric

3.9.3 NMOSFET at 32 nanometres with High-k (HfO_2) as Dielectric Gate Material

Figure 3.15 shows the bulk MOSFET with 32nm with High-k (HfO_2) as dielectric material in the gate oxide. The utilization of HfO_2 offers an advantage in terms of keeping the same effective oxide thickness for the higher physical thick layer of HfO_2 to achieve the oxide capacitance as before.

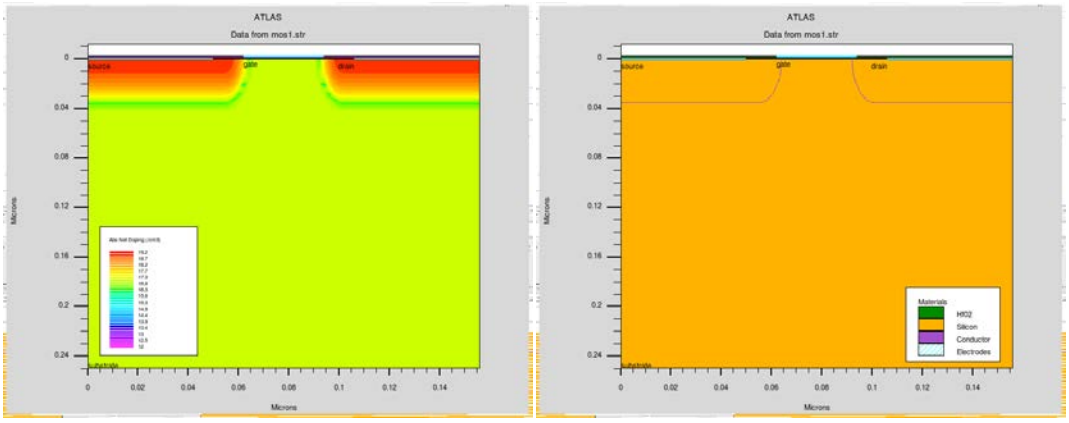

Figure 3.15: 32nm Bulk N-MOSFET a) Material view and b) Doping density view using high-k (HfO_2).

The transfer characteristics are shown in figure 3.16. The saturation (high V_{DS}) characteristics are shown with a green line and linear (low V_{DS}) characteristics are shown with a red line.

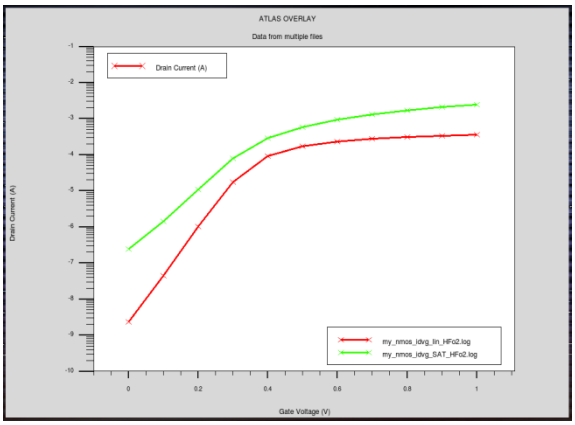

Figure 3.16: Transfer characteristics for bulk MOSFET with high-k as a dielectric.

3.9.4 Comparisons of 32 nm NMOSFET Characteristics with Different Oxide Material

The characteristics of drain current in saturation (high V_{DS}) on a logarithmic scale for different oxide materials is depicted in figure 3.17. The characteristics of SiO_2 as a dielectric for gate oxide are shown with a red line, the green line shows the characteristics of multi-oxide as a dielectric material for the gate oxide and the blue line shows the characteristics of HfO_2 as a dielectric material for the gate oxide.

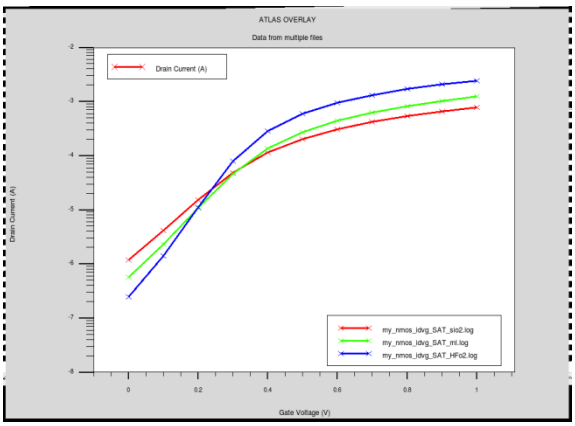

Figure 3.17: 32nm NMOS transfer characteristics with SiO_2, Multi oxide and HfO_2

Figure 3.17 depicts that the nMOSFET structure having HfO_2 as dielectric material (blue line) has the lowest value of the off current and highest value of on current. Afterward, the multi oxide has better on/off current properties than the device fabricated only with SiO_2. The sub-threshold slope of the device can also be deduced from the above figure and it can be seen that the device having HfO_2 as a gate dielectric has the minimum sub-threshold slope among all compared here. The detailed comparisons for the different dielectric materials obtained from numerical simulation are given in Table 3.2. The n-type materials have a Gaussian doping profile concentration of $1e^{20}$ cm^{-3} and a uniform doping concentration of $1e^{18}$ cm^{-3} was considered for the substrate.

Table 3.2: 32nm Bulk NMOS Characteristics with SiO_2, Multi oxide and HfO_2

Device	**Bulk NMOS with SiO_2**	**Bulk NMOS with Multi oxide**	**Bulk NMOS with HfO_2**
Vt_{sat} (V)	0.0655723	0.12889	0.22715
SS_{sat}(mV/decade)	0.176196	0.149	0.1122
I_{on}	0.000781229	0.00124	0.00244
I_{off}	1.18035 e^{-06}	5.688 e^{-07}	2.46 e^{-07}
I_{on}/I_{off}	661.862	2186.8	9925.8
Vt_{lin}	0.316061	0.320521	0.3212
SS_{lin}(V/decade)	0.101386	0.08839	0.07412
DIBL (V/V)	0.263672	0.2012	0.0999

3.9.5 Effect of High-k Material on Various Parameters

Table 3.2 shows the effects of high-k materials structure/ stack architecture. Some of the variations of characteristics parameters are analyzed as under

3.9.5.1 Effect of high-k material on DIBL

The value of the Drain Induced Barrier Lowering is calculated as

$$\text{DIBL} = \frac{V_{Th\,lin} - V_{Th\,sat}}{V_{sat} - V_{lin}} \qquad (3.3)$$

Here V_{thlin} is the threshold voltage in the linear region of operation (usually V_{DS}=0.05V) of V_{DS} and V_{thsat} is the threshold voltage in the saturated region of operation (usually at V_{DD}) of V_{DS}. Accordingly, the value of V_{sat} and V_{lin} is considered. Figure 3.18 depicts the variation of DIBL with high-k.

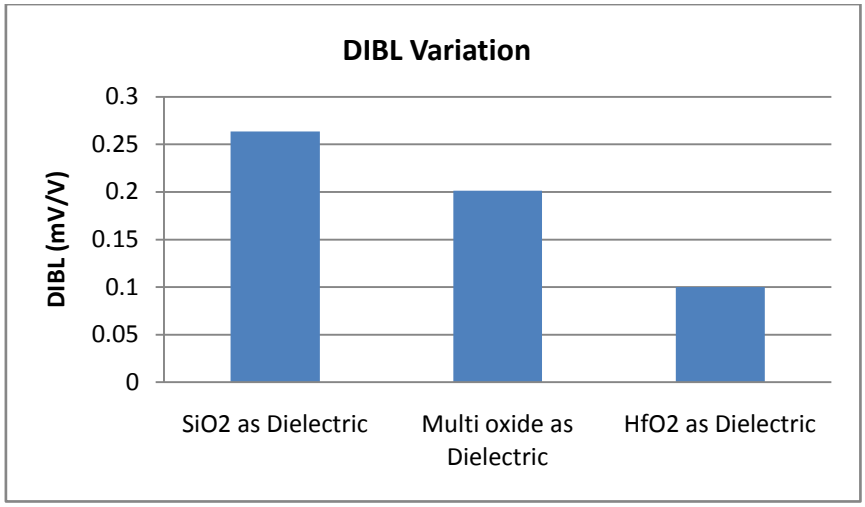

Figure 3.18: DIBL for 32nm bulk MOSFET with different dielectric materials

3.9.5.2 Effect of high-k material on the threshold voltage

The threshold voltage is calculated for enhancement mode NMOSFET when substrate bias is present as

$$V_{th} = V_{t_o} + \gamma \left(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{|2\emptyset_F|}\right) \quad (3.4)$$

Here $\gamma = \left(\frac{t_{ox}}{\epsilon_{ox}}\right)\sqrt{2q\varepsilon_{Si}N_A}$ (3.5)

Threshold voltage at zero substrate bias is represented as V_{to}, V_{SB} is the voltage between source and body substrate, $2\emptyset_F$ is the surface potential and γ is the body effect parameter. In equation 3.5, t_{ox} is oxide thickness; N_A is acceptor doping concentration and ϵ_{ox} is the permittivity of oxide. For a given MOSFET process, the threshold voltage depends on the thickness of the oxide along with the choice of oxide materials. The different oxide materials having different permittivity ought to vary the value of the threshold voltage. Figure 3.19 depicts the effects of the high-k material on the threshold voltage.

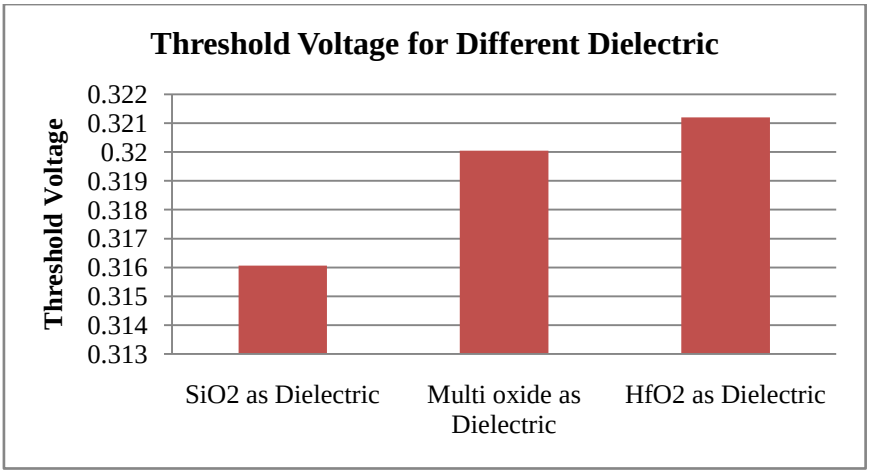

Figure 3.19: Threshold voltage variation on the application of high-k dielectric.

3.9.5.3 Effect of high-k material on the sub-threshold slope

The sub-threshold slope is a significant design parameter related to MOSFET, it is usually described how fast a device can turn off from the on-state. The sub-threshold slope is given by the expression

$$SS = 2.3\ \frac{kT}{q}\left(\frac{\partial \Psi_{min}}{\partial V_{gs}}\right)^{-1} \qquad (3.6)$$

Here Vgs represents the voltage between gate to source and $\partial \Psi_{min}$ denote minimal surface potential.

Alternatively, SS can also be represented as

$$SS = \left(\frac{kT}{q}\right) ln_{10}\left(1 + \left(\frac{C_D}{C_{ox}}\right)\right) \qquad (3.7)$$

Here electrons charge is represented as q, T is the temperature in kelvin, C_{ox} is the gate oxide capacitance and C_D is the depletion capacitance. As when $C_{ox} >> C_D$, the second term can be neglected. The SS depends on the first term only and has a value of 60 mV/decade [140]. Higher SS means a minimal change in drain current from the OFF state to the V_{th} which represents a higher OFF current at a specific V_{th}. The variation of the sub-threshold slope of the 32nm MOSFET for different dielectric materials is shown in figure 3.20.

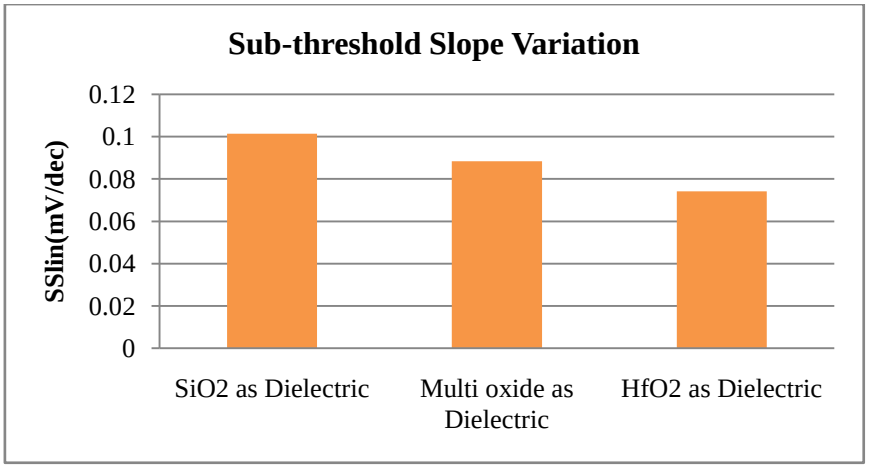

Figure 3.20: Variation of the sub-threshold slope with different dielectrics.

3.9.5.4 Effect of high-k material on I_{ON}/I_{OFF} current ratio

I_{ON}/I_{OFF} ratio is the characteristics parameter for the MOSFET device, it precisely tells how high the on current will be and how low the leakage current will be in the device. The I_{ON}/I_{OFF} ratio is dependent on the gate controlling the channel. With the increase of gate control by using high-k materials, the value of I_{ON}/I_{OFF} increases. The variation of I_{ON}/I_{OFF} with different dielectric materials for 32nm NMOSFET is as shown in figure 3.21. It can be seen that MOSFET with SiO_2 dielectric has a smaller value of I_{ON}/I_{OFF} ratio as compared to MOSFET with high-k dielectric materials which can be attributed to the fact that strong depletion of a channel occurs with higher barrier potential in high-k devices [141].

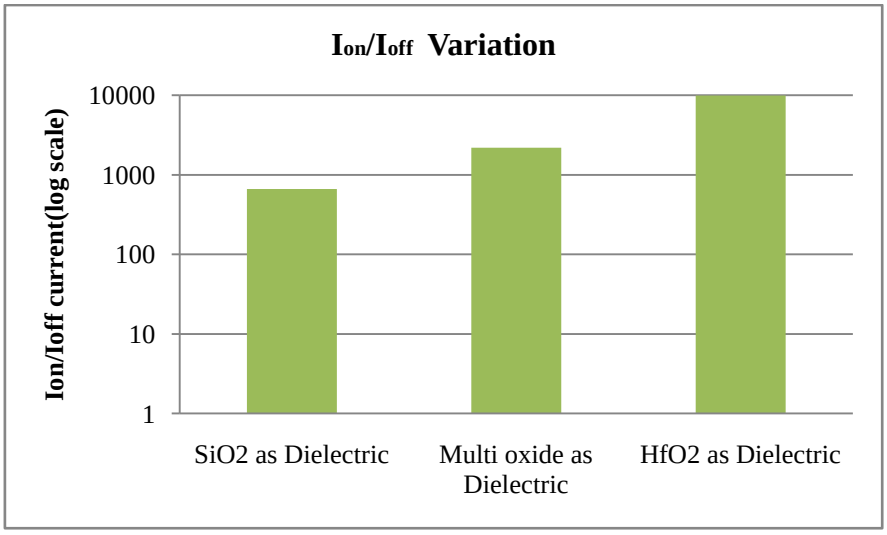

Figure 3.21: Variation of I_{ON}/I_{OFF} with different dielectric materials

3.10 MULTIPLE GATE MOSFET

The essential process of scaling results in an increase in SCEs. These SCEs as discussed above can be controlled by various device designing approaches. One such approach is utilizing multiple gates across the channel. This approach not only has better suppression of SCEs but also improves the current driving ability of the MOSFET [139]. Multiple gate MOSFETs structures are potent devices due to their capability in suppressing SCE without requiring high channel doping concentrations. In these structures, the thin body of the device restrains the SCEs efficiently. Hence, a lightly doped silicon layer may be used. This lightly doped silicon will minimize the effects which arise due to high doping like low carrier mobility and variation of threshold voltage because of the variation of statistical doping [142].

These devices have multiple gates so that they effectively control the channel from multiple sides. The multiple-gate architecture offers good controllability but also results in a complex and costly fabrication process. Hence, the simplest multiple gate design approaches i.e. double gate architecture is considered in the present work for investigation of characteristics of the bulk MOSFET.

3.11 DOUBLE GATE MOSFET

A double-gate structure is a special case of multiple-gate architecture where the two metals gates are created to have better control over the channel. These structures have carrier conduction in two shallow channels which are parallel to each other.

The DG MOSFET is proposed to be the ideal device structure for scaling by various researchers [46,143]. The device has a very thin layer of silicon as a channel along with two gates on each side of the channel. The electrical connections exist between the two gates. The drain field lines effects are minimized in these structures as shown in figure 3.22 for DG-SOI structures. The two gate structures screen the drain potential effects on the source [138]. The effects of channel length and impact of drain voltage on threshold voltage are very less as compared to conventional bulk MOSFET [144].

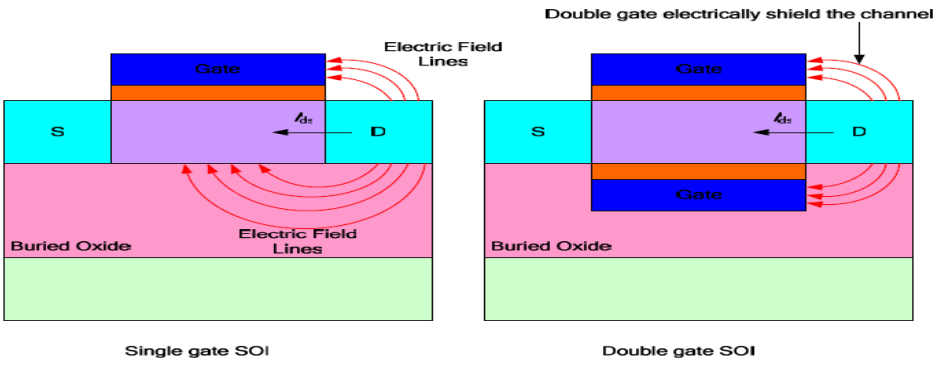

Figure 3.22: Drain field lines impact on SOI structure with (a) Single gate (b) Double gate.

The band-to-band tunnelling is also less significant as the high doping of the channel/body is not required. The utilization of the ultrathin body reduces the metal contact junction perimeter which causes low junction capacitance [148].

3.11.1 Advantage of Double Gate MOSFET

The double-gate MOSFET offers advantages over conventional bulk MOSFETs like

i) High drive current

ii) Good immunity to SCE

iii) Lower junction capacitance

iv) Better sub-threshold slope

v) Requirement of light doping

vi) High scalability

3.11.2 Demerits of Double Gate MOSFET

The two gates of DG MOSFET should be aligned properly but this proper alignment requires a complex process. The DG structures were also found to have high series resistance of drain and source, to minimize this series resistance the concept raised drain and source architecture is used [145]. The DG MOSFET requires some extra

processing steps hence in comparison to conventional bulk MOSFET, the DG MOSFET is complex and costly to fabricate.

3.12 SOI MOSFET

Silicon-on-insulator (SOI) is a semiconductor device in which the active silicon area is made above the insulating substrate. This insulating substrate is generally made up of an oxide layer called buried oxide or the BOX. A layer of silicon dioxide can be created by implanting oxygen into the silicon. SOI devices have better characteristics like low power dissipation due to the reduction of leakage currents, low parasitic capacitance, elimination of the requirement of wells and reduction of latch-up in comparison to bulk devices. It also suppresses the majority of SCEs which occurs in bulk MOSFET. The depletion region is not able to go beyond the BOX region, which results in a reduction in the leakage current and parasitic capacitances. SOI devices have fabrication compatibility with bulk technology.

Based on the thickness of the silicon channel SOI can be classified as partially depleted (PD) SOI and fully depleted (FD) SOI. In the case of PD-SOI, the depletion region does not extend to the whole silicon film. In the case of FD-SOI, the thickness of the silicon region is less than the depletion region of the device [27].

3.12.1 Advantages of SOI MOSFET

i) In an SOI device, the presence of SiO_2 in the buried (BOX) layer considerably reduces the capacitances between the substrate and source/drain region. It increases the speed of operation of semiconductor devices [146].

ii) SOI devices due to the availability of the oxide layer are isolated from each other in the lateral direction.

iii) The near-ideal device isolation achieved using SOI technology makes closer packaging of the SOI devices possible as compared to the bulk ones.

iv) Latch-up occurs when parasitic thyristor turns on in conventional CMOS circuits. The SOI MOSFETs are immune to latch-up due to the BOX layer. The p-n junctions

between the S/D junctions and the substrate are insulated preventing the formation of such parasitic thyristor.

v) Due to the BOX layer under the diffused regions, the only sidewalls of the diffused regions are available for the formation of the p-n junction. This subsequently reduces the p-n junction leakage current.

vi) The SOI MOSFET has a very thin body layer and shallow source/drain regions. As a result, the gate gains better control over the channel potential profile thereby significantly reducing the various short channel effects [147].

vii) Due to the presence of radioactive elements in semiconductor materials, α particles are produced in minute amounts. The innovative SOI devices provide excellent immunity to radiation caused by radioactive particles.

viii) Thin silicon films eliminate sub-surface leakage currents flowing through the substrate regions which are not under gate control in conventional bulk MOSFET. In SOI MOSFETs, with thin silicon film and BOX gate have better control over the channel reducing sub-surface leakages.

3.12.2 Disadvantages of Simple SOI Structure

Even though SOI shows superior performance in terms of higher speed, lower power dissipation, low values of parasitic capacitance over its bulk counterpart. But SOI is not completely free from SCEs which arises with SOI devices in the nano-regime. The other disadvantages of the SOI structure can be summarized as:

i) Floating body effects in partially depleted SOI MOSFETs results in ‘Kink’ effect in DC circuits and drain-current overshoot in switching circuits.

ii) Dynamic floating body effects and parasitic bipolar effects become significant with ultra low dimensional SOI structure and these effects are quite difficult to mitigate [147].

iii) High drain voltage forward biases the body-source junction and increases the off-current.

iv) Ultra-thin films are required to realize fully depleted devices. Many critical design adjustments are needed to be done for growing such thin films which are very difficult to be realized.

v) The superior quality of the buried oxide-silicon interface is required to reduce interface scattering and other effects.

vi) Due to the presence of thermally insulated SiO_2 layer of SOI structure creates the problem of self-heating effect. This self-heating can affect device performance and reliability. [146].

SOI structure is more immune against different SCEs compared to short-channel conventional MOSFETs but it is not fully free from the adverse effects of SCEs. Hence there are ample scopes for further performance improvement.

3.13 DOUBLE GATE SOI (DG-SOI) STRUCTURE

Earlier studies have revealed that applying a double gate in the device structure provides better control of channel charge resulting in enhanced mobility and reduced short channel effects. In DG SOI MOSFETs, both the gates are linked together creating a volume inversion in the silicon film. Hence, achieves an almost ideal sub-threshold slope for sufficiently low channel doping. Another significant benefit of DG MOSFET is the ability to adjust the device threshold voltage by choosing a suitable work function metal gate. Due to the presence of two gates, DG-MOSFET has better current drive capability; however, when gates are independently biased DG-MOSFET can provide increased logic functionality. DG SOI MOSFET transistors can exist in planar configuration or FinFET 3D configuration. In planar configuration, the current flows parallel to the surface. The channel and gates are vertical in the case of the FinFET structure. The DG-SOI FinFET device is created on the BOX layer and the silicon film along with two polysilicon gates exist on other sides of the channel. DG structure is generated by making the top gate inactive [figure 3.23(a)]. This is done by making thicker gate insulation on the top side of the channel. DG SOI MOSFET transistors have been analyzed for various performance characteristics in this work. The structure of DG-SOI MOSFET is shown in figure 3.23.

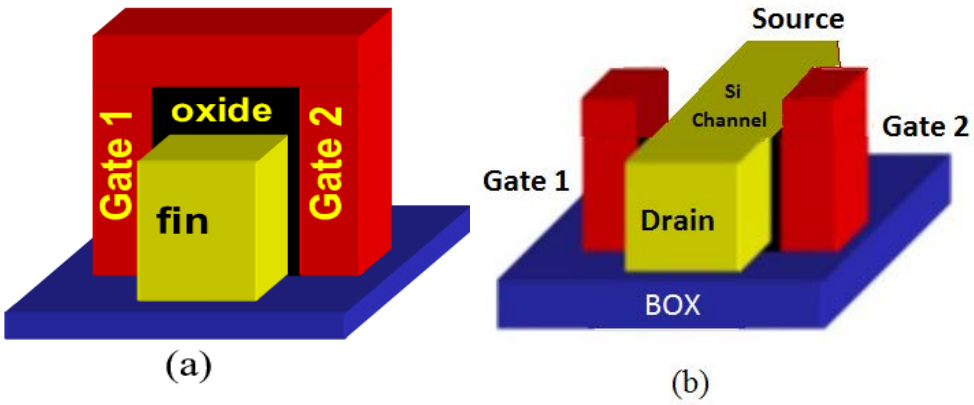

Figure 3.23: DG-SOI MOSFET with (a) Inactive top gate (b) Two gates

The dual-gate has two modes of operation. In the first mode, both the gates are connected and move simultaneously providing better short channel scalability due to tighter control of the gate over the channel and superior sub-threshold swing. Again, the dual-gate device can be operated with two gates independent of each other. This provides an option for controlling the front-gate threshold voltage with back gate bias. However, the two independent gates introduce an additional gate-to-gate capacitance [148].

3.14 PERFORMANCE IMPROVEMENTS IN DG-SOI MOSFETS

To improve the performance in conventional DG-SOI MOSFET for the parameters such as off current, on current, trans-conductance, DIBL and threshold voltage, many gate and channel engineering approaches are adopted. In this work, an approach of using high-k dielectric is introduced in the DG-SOI MOSFETs to suppress the leakage current and the Short Channel Effects.

The gate dielectric materials are required mainly for having good insulating properties and high capacitance value. The gate dielectric materials should be able to prevent the diffusion of dopants. It should have good thermal stability and very good interface adhesion with the substrate. However, the utilization of high-k materials improves the control of the gate and results in the reduction of SCEs along with all of the above qualities [149].

The performance of the DG-SOI MOSFETs device can be further enhanced by introducing high-k dielectric gate materials. With the increasing value of dielectric,

the value of DIBL is found to be decreasing exponentially which indicates suppression of SCE [150]. The transconductance of the devices was also observed to be improved with high-k dielectric material utilization. The numerical simulations of the 32 nm double gate with high-k and multi oxide stack architecture are shown next for the evidence of the suppression of SCE.

3.14.1 DG-SOI NMOSFET at 32 nanometres with SiO_2 as Dielectric Gate Material

Figure 3.24 shows the N-type DG-SOI MOSFET at 32nm having SiO_2 as a dielectric material. The physical thickness of oxide is taken as 2nm.

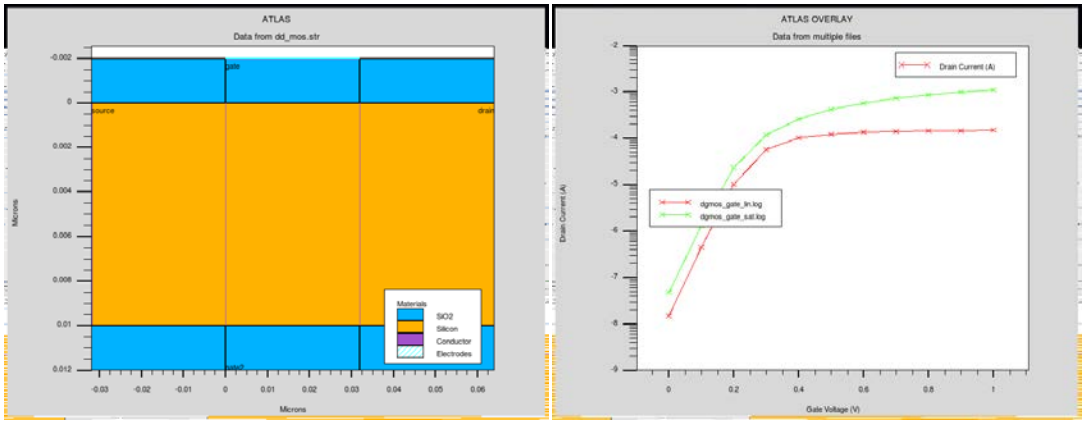

Figure 3.24: 32nm N-type DG-SOI MOSFET having SiO_2 dielectric a) Material view (b) Transfer characteristics

The transfer characteristics are shown in figure 3.24 (b) which is essential for the prediction of on/ off current and sub-threshold characteristics of the device. The saturation (high V_{DS}) characteristics are shown with a green line and linear (low V_{DS}) characteristics are shown with a red line.

3.14.2 DG-SOI NMOSFET at 32 nanometres with Multi oxide (SiO_2+HfO_2) as Dielectric Gate Material

Figure 3.25 shows the N-type DG-SOI MOSFET at 32nm having Multi oxide (SiO_2+HfO_2) as the dielectric material. The physical thickness of oxide is taken as 2nm (1nm for SiO_2 and 1nm for HfO_2)

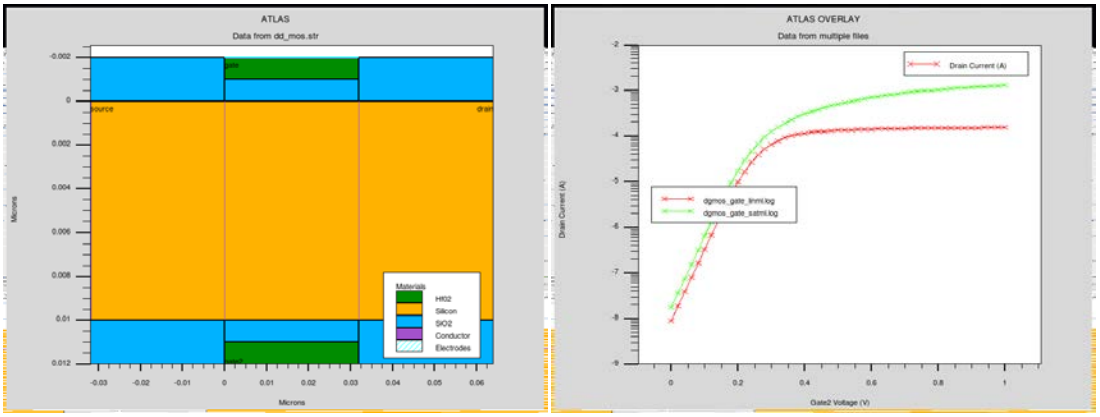

Figure 3.25: 32nm N-type DG-SOI MOSFET having multi oxide (SiO_2+HfO_2) dielectric a) Material view (b) Transfer characteristics

The transfer characteristics for 32nm N-type DG-SOI MOSFET having Multi oxide (SiO_2+HfO_2) as a dielectric are shown in figure 3.25 (b). The saturation (high V_{DS}) characteristics are shown with a green line and linear (low V_{DS}) characteristics are shown with a red line.

3.14.3 DG-SOI NMOSFET at 32 nanometres with HfO_2 as Dielectric Gate Material

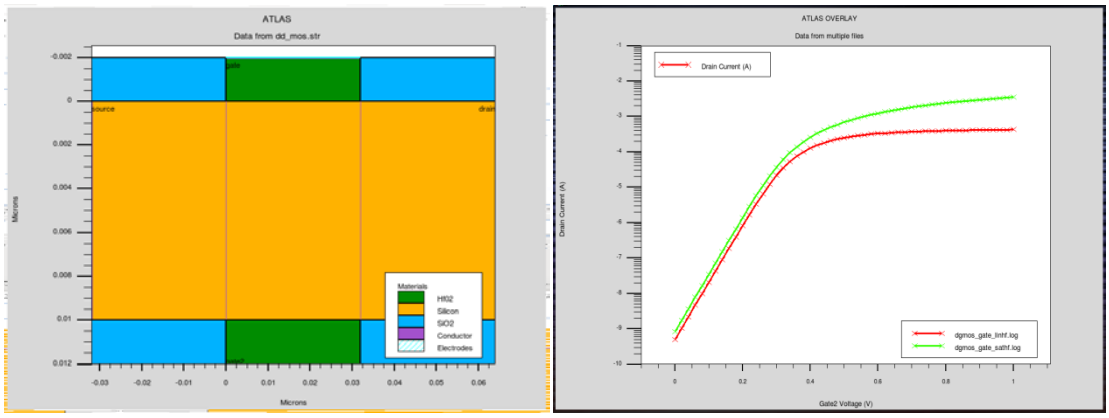

Figure 3.26: 32nm N-type DG-SOI MOSFET having HfO_2 dielectric a) Material view (b) Transfer characteristics

Figure 3.26 shows the N-type DG-SOI MOSFET at 32nm having HfO_2 as the dielectric material. The physical thickness of oxide is taken as 2nm. The transfer characteristics for 32nm N-type DG-SOI MOSFET having HfO_2 as dielectric are

shown in figure 3.26 (b). The saturation (high V_{DS}) characteristics are shown with a green line and linear (low V_{DS}) characteristics are shown with a red line.

3.14.4 Comparisons of 32 nm N-type DG MOSFET Characteristics with Different Oxide Material

Figure 3.27 depicts the characteristics of drain current in saturation (high V_{DS}) on a logarithmic scale for different oxide materials. The characteristics of SiO_2 as a dielectric for gate oxide are shown with a red line, the green line shows the characteristics of multi-oxide as a dielectric material for the gate oxide and the blue line shows the characteristics of HfO_2 as a dielectric material for the gate oxide.

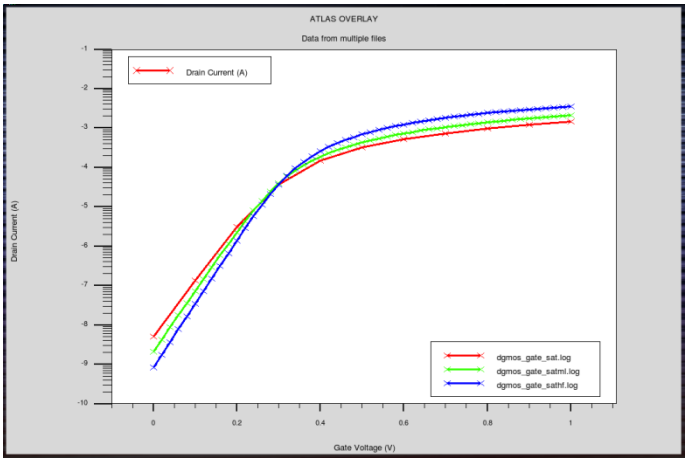

Figure 3.27: 32nm N-type DG-SOI MOSFET transfer characteristics with SiO_2, multi oxide and HfO_2

It can be seen from figure 3.27 that the N-type DG-SOI MOSFET architecture having HfO_2 (oxide permittivity=21) as dielectric material (blue line) has the lowest value of the off current and highest value of on current, afterward, the multi oxide has better on/off current properties than a device made only with SiO_2. The sub-threshold slope of the device can also be deduced from the above figure and it can be seen that the device having HfO_2 as a gate dielectric has the minimum sub-threshold slope among all compared here. The detailed comparisons for the different dielectric materials obtained from numerical simulation are given in Table 3.3. The n-type materials have a Gaussian doping profile concentration of $1e^{20}cm^{-3}$ and a uniform doping concentration of $1e^{18}\ cm^{-3}$ was considered for the substrate. The work-function of both

the gates was taken as 4.56eV. The linear and saturation voltages are taken as 0.05V and 1V respectively.

Table 3.3: 32nm N-type DG-SOI MOSFET Characteristics with Different Oxide

Device	DG with SiO2	DG with Multi oxide	DG with HfO2
Vt_{sat}	0.198961	0.21783	0.2195
SS_{sat}	0.06979	0.06457	0.061479
I_{on}	0.0014455	0.00210674	0.00355436
I_{off}	5.03399 e-9	2.08 e-9	8.2436 e-10
I_{on}/I_{off}	287160	1.009 e+6	4.309 e+6
Vt_{lin}	0.2208	0.2372	0.237081
SS_{lin}	0.06832	0.06421	0.0615757
DIBL	0.02299	0.02048	0.018588

3.14.5 Effect of High-k Material on Various Parameters for N-type DG-SOI MOSFET

Table 3.3 shows the effects of high-k materials/ high-k materials in stack architecture for N-type DG-SOI MOSFET at 32nm. Some of the variations of characteristics parameters are analyzed as under

3.14.5.1 Effect of high-k material on DIBL in N-type DG-SOI MOSFET

The Drain Induced Barrier Lowering or DIBL is given by equation 3.3.

$$\text{DIBL} = \frac{V_{Th\,lin} - V_{Th\,sat}}{V_{sat} - V_{lin}}$$

Here V_{sat} and V_{lin} are considered as 1.0 V and 0.05 V respectively. The V_{thlin} is the threshold voltage measured at V_{lin} and V_{thsat} is the threshold voltage measured at V_{sat}. Figure 3.28 shows the effect of high-k on DIBL for N-type DG-SOI MOSFET.

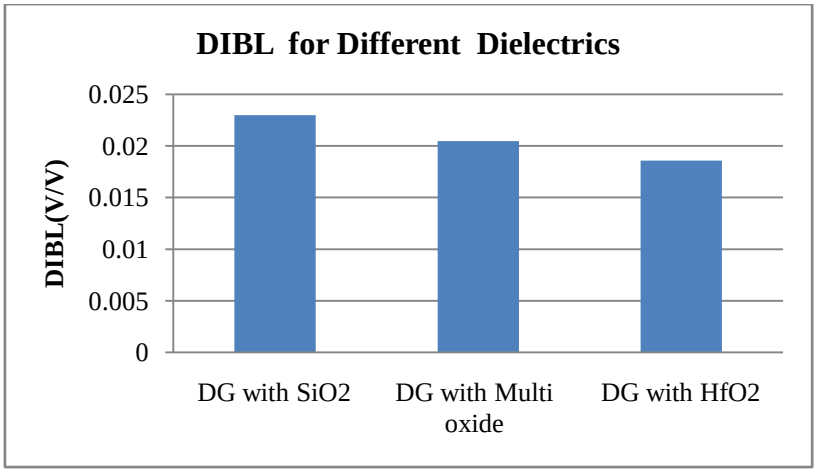

Figure 3.28: DIBL for 32nm N-type DG-SOI MOSFET with different dielectric materials

3.14.5.2 Effect of high-k material on threshold voltage in N-type DG-SOI MOSFET

The threshold voltage is given by equations 3.4 and 3.5.

$$V_{th} = V_{t_o} + \gamma \left(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{|2\emptyset_F|}\right)$$

Here $\gamma = \left(\frac{t_{ox}}{\epsilon_{ox}}\right)\sqrt{2q\varepsilon_{Si}N_A}$

Threshold voltage at zero substrate bias is represented as V_{t_o}, $2\emptyset_F$ is the surface potential, V_{SB} is a voltage between source and body substrate and γ is body effect parameter. t_{ox} is oxide thickness, N_A is acceptor doping concentration and ϵ_{ox} is the permittivity of oxide. Hence, for the given MOSFET process the threshold voltage depends on the thickness of oxide along with the choice of oxide materials. The different oxide materials having different permittivity ought to vary the value of the threshold voltage. Figure 3.29 depicts the effects of the high-k material on the threshold voltage.

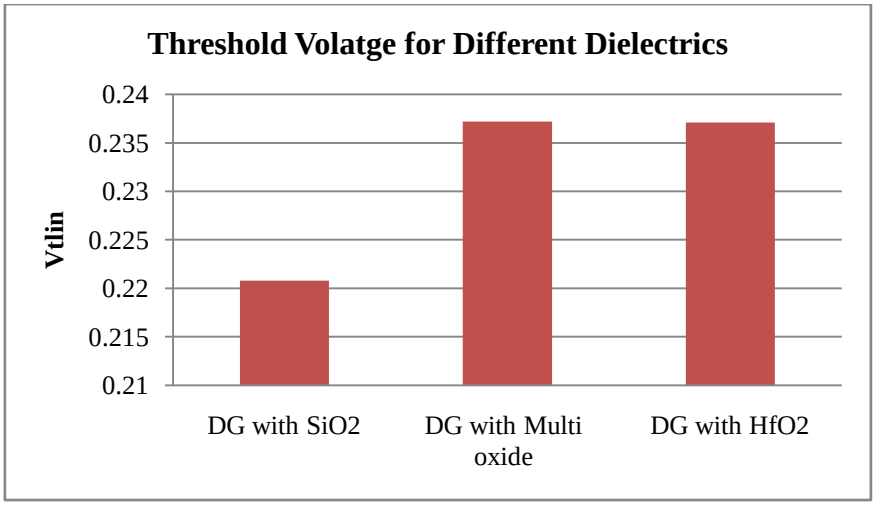

Figure 3.29: Threshold voltage variation with different dielectrics.

3.14.5.3 Effect of high-k material on the sub-threshold slope in N-type DG-SOI MOSFET

As already discussed the sub-threshold slope (SS) is a significant design parameter related to MOSFET, it is usually described how fast a device can turn off from the on-state. The sub-threshold slope is given by the equation (3.6)

$$SS = 2.3\ \frac{kT}{q}\left(\frac{\partial \Psi_{min}}{\partial V_{gs}}\right)^{-1}$$

Here Vgs is a voltage between gate to source, $\partial\Psi_{min}$ denote minimal surface potential. As represented earlier SS can be calculated as given by equation (3.7)

$$SS = \left(\frac{kT}{q}\right) ln_{10}\left(1 + \left(\frac{C_D}{C_{ox}}\right)\right)$$

As already discussed the SS depends on the first term only and has the ideal value of 60 mV/decade. The effect of high- k materials on the sub-threshold slope of the 32nm MOSFET is shown in figure 3.30.

3.14.5.4 Effect of high-k material on I_{ON}/I_{OFF} current ratio in N-type DG-SOI MOSFET

As discussed earlier I_{ON}/I_{OFF} ratio is the characteristics parameter for the MOSFET device. The variation of I_{ON}/I_{OFF} with different dielectric materials for 32nm N-type DG-SOI MOSFET is shown in figure 3.31. It can be seen from figure 3.31 that MOSFET with SiO_2 dielectric has a smaller value of I_{ON}/I_{OFF} ratio as compared to MOSFET with high-k dielectric materials which can be attributed to the fact that

strong depletion of a channel occurs with higher barrier potential in high-k devices [151].

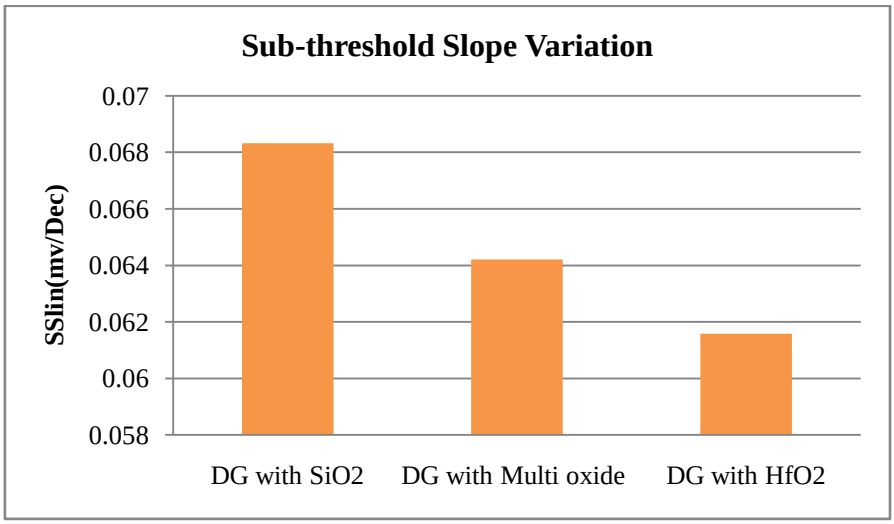

Figure 3.30: sub-threshold slope variation with different dielectrics.

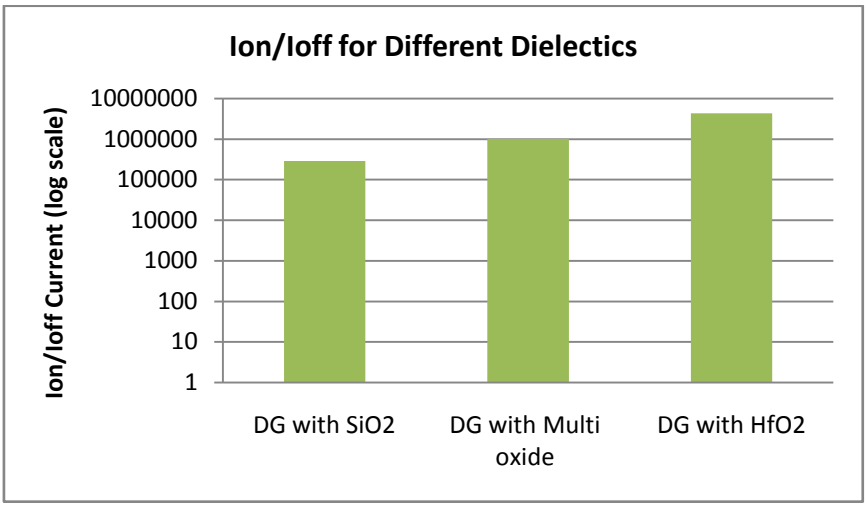

Figure 3.31: Variation of I_{ON}/I_{OFF} with different dielectric materials

3.15 THREE DIMENSIONAL (3D) VIEW OF 32 NM N-TYPE DG MOSFET

Figure 3.32 below depicts the three-dimensional view of 32 nm N-type DG MOSFET. Here purple colour represents conductor, yellow represents vacuum, blue represents SiO_2 and orange represents Silicon.

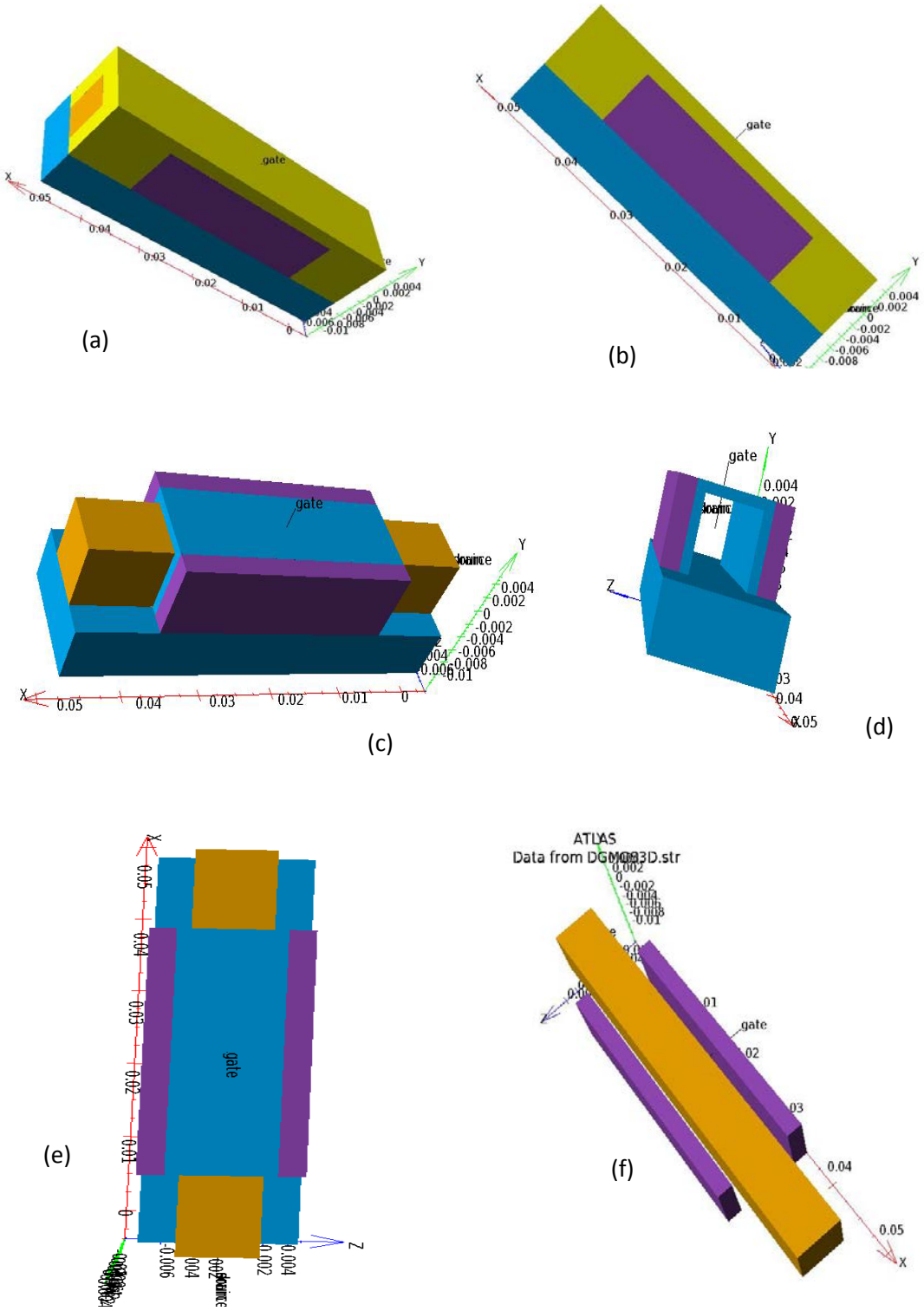

Figure 3.32: The 3D architecture of DG-SOI MOSFET with various abstract layers (a) 3D view (b) 3D view from gate side (c) 3D view with vacuum removed (d) 3D view with vacuum and silicon removed (e) 3D top view with vacuum removed with double gate (f) 3D view with gate and silicon material (oxide layer removed)

CHAPTER-IV

ANALYTICAL MODELLING AND SIMULATION OF JUNCTIONLESS TRANSISTOR

4.1 INTRODUCTION

At present semiconductor devices like MOSFET have two junctions, one present between the drain and channel and another present between source and channel. The separation between the source and drain is reduced by scaling. For new-age devices, this separation (channel length) has reached under 10 nm range. The advantage of the scaling process can be taken by keeping the high doping (in the range of 10^{20} cm^{-3}) in the source and drain region and it should change abruptly in terms of material and doping concentration (low) to create the channel region (in the range of 10^{15} cm^{-3}) [152]. This process should occur within a very limited length in the range of a few nanometers. The practical fabrication of this ultra-steep doping profile is very complicated even at present-day Foundry Technology. The modern-day ion-impanation instrument may not create such a profile easily in the limited length [153]. After ion-implantation high-temperature annealing is carried out to have high dopant activation in the drain and source region. This high-temperature processing creates thermal lateral diffusion of the dopant from the highly doped source and drain to the channel. The high-temperature annealing constraints the realization of the ultra-steep doping profile. It was realized that the device having no junction if works as a transistor will ease out the above complex process for scaled devices. Hence the device without junction or junctionless device does not require any ultra-steep doping profile and therefore the device will be fabricated with ease and in a cost-efficient manner.

4.2 JUNCTIONLESS FIELD EFFECT TRANSISTORS (JLFET)

The concept and principle of the junctionless device were patented in 1930 by Julius Edgar Lilienfield, a Physicist of Austrian-Hungarian origin [154], even before the realization of the first transistor. These junctionless devices are again into the recently proposed structures for realizing the scaled version of conventional MOSFET. The

junctionless FETs use a very thin semiconductor film with a stacked gate to modulate the current conduction by controlling the resistance of the film. The device structures use a different mechanism for the conduction of current and have different device properties due to the absence of the gate. Due to the latest advancement in the fabrication process, the researchers were able to realize the JLFET experimentally in the last few years only. The junctionless device structures have a low thermal budget and also require less complex fabrication. It also provides a cost-efficient solution to scaling issues.

4.3 DEVICE STRUCTURE AND OPERATION

The JLFET has heavily doped silicon film and a gate to modulate the carrier concentration in the channel to control the resistivity of the channel. The source and drain are heavily doped to have better ohmic contacts [155]. As the doping type and concentration from source to drain through the channel is the same hence the presence of junction is eliminated. The structure of the JLFET device is shown in Figure 4.1.

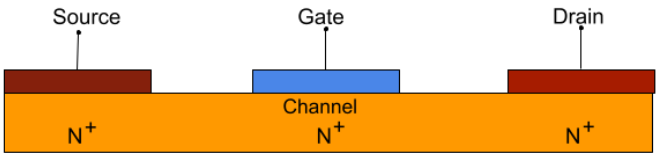

Figure 4.1: Structure of Junctionless Field-Effect Transistor

The JLFETs work on the principle of modulation of carrier concentration by applying the electric field using the gate [156]. In JLFET, the work function difference between the semiconductor and metal gate is such that the electrons would flow from the semiconductor interface to metal. The electric field will be created from semiconductor to metal when the work-function difference between metal to a semiconductor is positive. This field will create depletion in the semiconductor interface region as the electrons from the interface have flown into the metal. When the semiconductor is very thin, it is possible to completely deplete it. It is called volume depletion in which the complete volume under the gate is depleted. So the gate electrode work function creates volume depletion of the channel region to switch off the device [157].

In junctionless FETs, when the applied gate voltage is 0 V on the gate electrode having a high work function, the volume depletion in the thin channel occurs which restrain the flow of the majority charge carrier between source and drain. As the silicon channel is heavily doped in JLT so to achieve complete volume depletion, a gate with high work-function is required for NMOS and a gate with low work-function is required for PMOS. When the silicon channel of the JLT device is depleted it offers very low conductivity and is in the off state. This mode of operation for JLTs is known as a full depletion mode.

When the voltage at the gate electrode is made positive, the depletion layer starts to reduce and expose the undepleted region in the middle of the channel. It allows the majority of charge carriers to flow from source to drain. This is called partial depletion as still some part of the channel remains depleted and this undepleted part of the channel exists in the center of the channel. The gate voltage at which the undepleted region in the middle of the channel develops in the merged depleted region is called threshold voltage.

When the voltage at the gate terminal is further increased, the width of the depletion region reduces and hence exposing more undepleted regions for the charge carrier to move on. This operating mode of the device is known as flat band mode. The gate voltage at which the whole depletion width is reduced is called flat band voltage for JLFETs. In this case, the complete volume of the channel is available for the majority charge carrier to flow from source to drain.

When the voltage at the gate terminal is enhanced further, the electrons (in NMOS) would be attracted towards the surface of the channel. The device is said to work in the accumulation mode of the region. The accumulation mode is a condition in which voltage equal to supply voltage is applied at the gate and between drain to source.

The flat band voltage in which the charge conduction takes place throughout the device reduces the possibility of trapping the charge carrier near the surface. It makes the device less affected by many SCEs like the surface scattering and mobility reduction of charge carriers near the surface. The JLFETs have many advantages associated due to their working principle and simple fabrication process as compared to conventional MOSFETs.

4.4 MODELING OF FETS

The appropriate models for FETs are developed to assist the application of FETs. The theoretical models are essential to give a good understanding of the basics and operation of FETs. The generated model can be used in circuit simulators to characterize the circuits. The developments of robust, precise and computationally capable models for FETs are required to understand the circuit designs using new devices and to predict the performance of the circuits containing these FETs.

4.5 VARIOUS FET MODELING

In FET modeling the analytical relationship is derived that explains the electrical characteristics of FETs according to fundamental physics. The analytical model helps in realizing the device optimization and analysis at the circuit level. The general theoretical modeling of FETs can be classified as (a) Analytical modeling and (b) Compact modeling.

The familiar physical equations are solved with relevant approximations to produce a relationship between the input voltages and the output current in analytical modeling. The device's physical properties are more understandable by using the analytical models because it provides physical insight into the device. It seems that analytical models are more exact. However, they are computationally incapable and time-inefficient [158]. Therefore, these are not used for circuit or system-level simulations.

Compact models are developed by methods of Curve Fitting to suitably replicate the experimental characteristics and are usually empirical in nature. In this modeling, the experimental characteristics of terminal voltages and other empirical parameters are altered to replicate the data obtained experimentally. The compact models in comparison to analytical models are robust, computationally capable and fast [158]. Hence, these models are beneficial for circuit designers. However, these models do not give any fundamental information about the device's physical properties.

In terms of physical modeling, another category of modeling exist which includes aspects of both i.e. analytical modeling and compact modeling called compact analytical modeling. These models are based on fundamental physics and are also

fast. These models use suitable approximation and empirical relations to model the device.

Other than these some researchers have developed a quantum mechanics-based Atomistic Modeling Approach [159]. These models are very accurate and relevant at a very short length of the channel. It is expected that with the advancement in fabrication technology when the thickness/length of the silicon layer will reach under 7nm, these models have to be used to correctly access the electrical behavior of the device. However, these models are computationally inefficient and take too much time at present.

The very common technique to find out the analytical model for surface potential (Ψ_S) and its relation with gate voltage (V_G) is determined by solving Poisson's Equation using suitable assumptions and boundary conditions [160]. The surface potential model further can be used to find the threshold voltage. The gate voltage at which the inversion layer carrier density is equal to the bulk carrier concentration is known as threshold voltage [161].

4.6 ANALYTICAL MODEL FOR THRESHOLD VOLTAGE AND SURFACE POTENTIAL OF JLFETs

The minimum voltage required to turn the MOSFET is known as the threshold voltage. The threshold for single gate JLFET can be modeled by considering that the gate voltage (V_G) is applied to alter the potential drop across the gate oxide (Ψ_{ox}) and the surface potential (Ψ_S), which can be represented as 4.1[162]

$$V_G = V_F + \Psi_{OXIDE} + \Psi_S \qquad (4.1)$$

Where V_F is the flat-band voltage. It represents the charges present in oxide under the gate and the difference of work-function between Si substrate and gate. The surface potential can be calculated by approximating the charges of the depletion region to be present at the silicon-silicon dioxide interface as shown in Figure 4.2 (b).

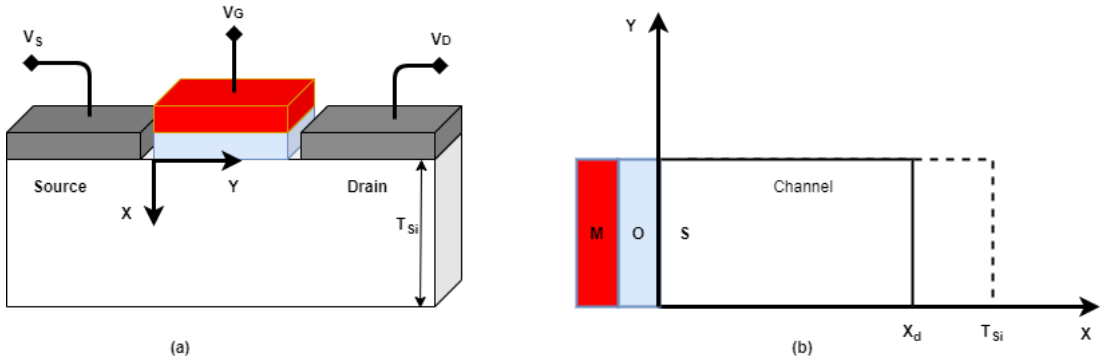

Figure 4.2**:** (a) Single-Gate JLFET (b) Silicon Depletion Charge Profile

The Poisson's Equation is used to find the relation between charge and potential as equation (4.2)

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=-\frac{\rho}{\epsilon_{Si}} \qquad (4.2)$$

For long-channel JLFET, the electric field component variation in the *y*-direction is insignificant compared to the *x*-direction [163]. Hence the electric field in the *y*-direction can be neglected by using gradual channel approximation. The 2D Poisson's Equation can be modified as

$$\frac{\partial^2\Psi(x)}{\partial x^2}=-\frac{\rho}{\epsilon_{Si}} \qquad (4.3)$$

Where the charge density in silicon channel is represented as $\rho= N_D*q$ (N_D doping concentration of donor and q is electron charge), the potential distribution in the channel is represented by $\Psi(x)$ and silicon permittivity is represented as ϵ_{Si}. By integrating Poisson's Equation is integrated w.r.t. x, we get

$$E(x)=\frac{qN_D x}{\epsilon_{Si}}+c \qquad (4.4)$$

Where E(x) is the electric field distribution in the Si channel and c is the integration constant. Assuming the electric field starting from the gate is reduced to 0 at the end of the depletion region i.e. $x = x_d$ (depletion region width), the c is can be determined as

$$c=-\frac{qN_D x_d}{\epsilon_{Si}} \qquad (4.5)$$

The surface potential can be found by integrating equation (4.4) with respect to x taking x equal to 0 to x_d, we get

$$\Psi(x_d) - \Psi(0) = \frac{qN_D x_d^2}{2\epsilon_{Si}} \quad (4.6)$$

Considering υ as electron quasi-Fermi potential ($x=x_d$), at silicon-silicon oxide the surface potential is

$$\Psi_s = \upsilon - \frac{qN_D x_d^2}{2\epsilon_{Si}} \quad (4.7)$$

In the case of volume depletion in JLFET υ=0, hence this surface potential modifies to

$$\Psi_{S} = - \frac{qN_D x_d^2}{2\epsilon_{Si}} \quad (4.8)$$

The electric field at the surface can be obtained by putting $x = 0$ in equation (4.4) as

$$E_s = - \frac{qN_D x_d}{\epsilon_{Si}} \quad (4.9)$$

The electric field inside the oxide can be found and represented as E_{oxide}. It can be found that $E_{oxide}*\epsilon_{oxide} = E_s*\epsilon_{Si}$ (assuming the electric field is constant inside the oxide layer). Hence potential drop across the oxide layer is

$$\Psi_{OXIDE} = E_{OXIDE}\, t_{OXIDE} = - \frac{q\, N_D x_d t_{OXIDE}}{\epsilon_{OXIDE}} \quad (4.10)$$

Here gate oxide thickness is represented as t_{oxide}. Now equation (4.1) can be represented as

$$V_G = V_F - \frac{qN_D x_d^2}{2\epsilon_{SI}} - \frac{qN_D x_d\, t_{OXIDE}}{\epsilon_{OXIDE}} \quad (4.11)$$

At the threshold voltage, the complete film will get depleted and x_d will be equal to t_{Si} (full width of silicon). The expression for the threshold voltage for single gate JLFET can be represented as

$$V_{Th} = V_F - \frac{qN_D t_{Si}^2}{2\epsilon_{Si}} - \frac{qN_D t_{Si}\ t_{OXIDE}}{\epsilon_{OXIDE}} \quad (4.12)$$

The threshold voltage for DG-JLFET can be found by modifying t_{Si} to $t_{Si}/2$ (as one gate depletes half of the depletion region). Hence, we get threshold voltage for DG-JLFET

$$V_{Th} = V_F - \frac{qN_D t_{Si}^2}{8\epsilon_{Si}} - \frac{qN_D t_{Si}\ t_{OXIDE}}{2\epsilon_{OXIDE}} \quad (4.13)$$

It can be observed that the threshold voltage is a function of the thickness of silicon film as observed in equation (4.13).

To find the relationship between gate voltage and surface potential the Gauss's law is applied at the Si-SiO_2 interface, the semiconductor channel charge density (Q_{SC}) can be related to the electric field (E_S) as

$$Q_{SC} = \epsilon_{Si} E_S \quad (4.14)$$

As the electrical displacement vector is continuous at the interface, hence we have

$$\epsilon_{Si} E_S = \epsilon_{oxide} E_{oxide} = \epsilon_{oxide} \frac{(V_G - V_F - \Psi_S)}{t_{oxide}} = C_{OXIDE} (V_G - V_F - \Psi_S) = Q_{SC} \quad (4.15)$$

From the above equation, we get the relationship between surface potential and semiconductor channel charge density. This charge density can be written as

$$Q_{SC} = qN_D x_d \quad (4.16)$$

Solving the equation (4.16) and (4.7) we get

$$\Psi_s = \upsilon - \frac{(V_G - V_F - \Psi_S)^2}{\eta} \quad (4.17)$$

Where

$$\eta = \frac{2qN_D \epsilon_{Si}}{c_{OXIDE}^2} \quad (4.18)$$

The equation (4.17) gives an analytical relationship between the surface potential and gate voltage. It is the surface potential model for single gate JLFETs. As the single

gate JLFETs have inefficient volume depletion. Hence, single JLFETs are not used. The modeling of JLFETs which is also used for carrying out the numerical simulations is carried out as follows.

4.6.1 Parabolic Approximation Technique for Modeling DG-JLFETs

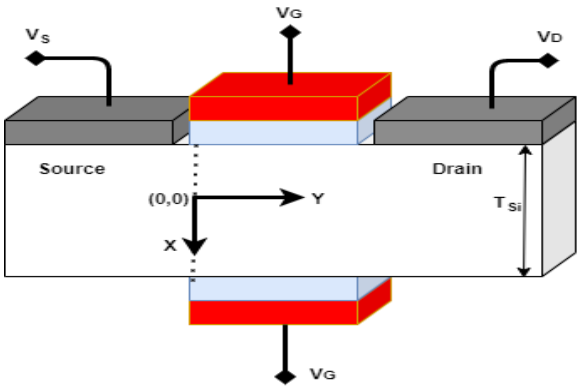

Figure 4.3**:** Double Gate JLFET.

The boundary conditions of a DGJLFET as shown in Figure 4.3 are as under

i) The surface potential is the potential at the Silicon-silicon oxide interface, as

$$\Psi(\pm\frac{t_{Si}}{2}) = \Psi_S \qquad (4.19)$$

ii) The electric field at the center of the JLFET should be zero due to its symmetric nature, hence

$$\frac{d\Psi}{dx} = 0 \text{ at } x=0 \qquad (4.20)$$

iii) The electrical displacement vector is continuous near to top gate at the silicon-silicon oxide interface, hence

$$\epsilon_{Si} E_{S,t} = C_{OXIDE} (V_G - V_F - \Psi_S) \qquad (4.21)$$

iv) Similarly, the electric displacement vector is continuous near the bottom gate at the Silicon-silicon oxide interface, hence

$$\epsilon_{Si} E_{S,b} = -C_{OXIDE} (V_G - V_F - \Psi_S) \qquad (4.22)$$

The pseudo-2D or the Parabolic Approximation Technique is used to model surface potential in JLFETs in various literatures [164-172]. This method is used as the potential distribution profile in the direction along the channel length (y-direction) differs but along the thickness the potential distribution profile remains constant [171]. Hence, the potential distribution profile can be represented as a quadratic polynomial [172]

$$\Psi(x,y) = \alpha_0(y) + \alpha_1(y)x + \alpha_2(y)x^2 \qquad (4.23)$$

The equation (4.23) is limited to second-order as the four boundary conditions of DG-JLFETs can be utilized to solve the only up to second-order quadratic equation. Hence other higher-order terms are neglected [172-174]. These approximations can be used to reduce 2D Poisson's Equation to an easy single dimension equation. Now the boundary conditions are used to find the valid and continuous relation between gate voltage and surface potential.

Equation (4.20) represents that in JLFETs, the electric field at the center is zero or E (0, y) =0, by substituting this value in equation (4.23), we get $\alpha_1(y)$ =0. Hence, equation (4.23) modified to

$$\Psi(x,y) = \alpha_0(y) + \alpha_2(y)x^2 \qquad (4.24)$$

Considering the center potential as $\Psi_{0,}$ using equation (4.19) we get $\alpha_0(y) = \Psi_0$.

Considering $\Psi_{S,\,b}$ as surface potential. Using equations (4.19) and (4.21) the equation (4.23) can be written as

$$\Psi(x,y) = \Psi_0 + (\Psi_{S,b} - \Psi_0)\frac{4x^2}{t_{Si}^2} \qquad (4.25)$$

The equation (4.22) can be utilized to represent ϵ_{oxide}*E_{oxide}=ϵ_{Si}*E_{Si} as

$$-C_{OXIDE}\left(V_G - V_F - \Psi_{S,b}\right) = -\epsilon_{Si}\frac{d\Psi\left(\frac{t_{Si}}{2},y\right)}{dx} = \frac{4\epsilon_{Si}\Delta\Psi}{t_{Si}} \qquad (4.26)$$

The silicon channel charge density which includes depletion charge and mobile electrons is given by [173]

$$\rho = \mathrm{q}N_D\left[e^{\frac{(\Psi_0-\upsilon)}{V_t}} - 1\right] \qquad (4.27)$$

The total charge density inside the silicon channel can be found by integrating equation (4.29) w.r.t. x using the value of the equation 4.25 and further solving we get

$$Q_{Sc} = \mathrm{q}N_D t_{Si} - \mathrm{q}N_D e^{\frac{(\Psi_0-\upsilon)}{V_t}} \int_{\frac{-t_{Si}}{2}}^{\frac{t_{Si}}{2}} e^{-\left(\frac{4\Delta\Psi}{t_{Si}^2 V_t}\right)x^2}\, dx \qquad (4.28)$$

Where $\Delta\Psi_0 = \Psi_0 + \Psi_{sb}$

Utilizing error function [174] and further solving, the total charge density is given by

$$Q_{Sc} = \mathrm{q}N_D t_{Si}\left[1 - \frac{e^{\frac{(\Psi_0-\upsilon)}{V_t}}}{2}\sqrt{\frac{\pi V_t}{\Delta\Psi}}\left\{\mathrm{erf}\left(\sqrt{\frac{\Delta\Psi}{V_t}}\right)\right\}\right] \qquad (4.29)$$

Equation (4.29) can be further solved by assuming the error function as unity [174]. This relationship was derived by assuming the parabolic potential profile, which exists in partially as well as fully depletion mode. In the flat band and weak inversion mode, the potential profile is not parabolic. The parabolic approach for modeling holds good for JLFETs as flat band condition occurs only when the device is on [175-178].

4.6.2 Short-Channel JLFETs Modeling

The modeling of the surface potential for DG-JLFETs is carried out in sections 4.6.1. In the above modeling, the impact of drain voltage on surface potential is neglected. The above modeling holds accuracy only for the long-channel JLFETs. However, the separation between source/channel interfaces to drain is very small in short channel JLFET. Hence, the electrical field interacts with the surface potential. This interaction disturbs the surface potential at the source/channel interface and causes DIBL [179]. Hence, the modeling for short channel JLFETs must take SCEs into consideration. A simple method for modeling the short channel JLFETs is described below.

4.6.2.1 Quasi-2D scaling equation

The quasi-2D scaling equation is used to obtain the simple second-order differential equation from the 2D Poisson's Equation. The 2D Poisson's Equation for MOSFETs in the sub-threshold regime may be written as by ignoring the mobile carriers in total charge density [180].

$$\frac{\partial^2\Psi(x,y)}{\partial x^2} + \frac{\partial^2\Psi(x,y)}{\partial y^2} = \frac{qN_A}{\epsilon_{Si}} \qquad (4.30)$$

As discussed in the last section the parabolic potential approximation is taken in *x*-direction as equation (4.23).

$$\Psi(x,y) = \alpha_0(y) + \alpha_1(y)x + \alpha_2(y)x^2$$

Similarly using boundary condition we have equation (4.24) as

$$\Psi(x,y) = \alpha_0(y) + \alpha_2(y)x^2$$

The value of α_2 can be found assuming continuity of electric displacement vector we have from equation (4.27)

$$-C_{OXIDE}\left(V_G - V_F - \Psi_{S,b}\right) = -\epsilon_{Si}\frac{d\Psi\left(\frac{t_{Si}}{2},y\right)}{dx} = -\epsilon_{si}t_{Si}\alpha_2(y) \quad (4.31)$$

The surface potential can be obtained by simplifying the equation (4.24) by putting the value of α_2 and considering the relationship between center and surface potential

$$\Psi_S(y) = \frac{\Psi_0(y) + \frac{C_{OXIDE}\ t_{Si}}{4\epsilon_{Si}}(V_G - V_F)}{1 + \frac{C_{OXIDE}\ t_{Si}}{4\ \epsilon_{Si}}} \qquad (4.32)$$

Utilizing equations (4.37) and (4.39) to solve equation (4.30), the central potential is given as

$$\frac{\partial^2\Psi_S(y)}{\partial y^2} - \frac{4C_{OXIDE}}{\epsilon_{Si}\,t_{Si}}\left(\Psi_S(y) - V_G - V_F + \frac{qN_A t_{Si}}{4C_{OXIDE}}\right) = 0 \qquad (4.33)$$

The equation (4.33) can be simplified by considering $1/L_1^2=4C_{oxide}/\epsilon_{Si}*t_{Si}$, $\xi_S=V_G-\gamma_1$ and $\gamma_1=V_F-(qN_At_{Si})/4C_{oxide}$. Here L_1 is the natural length and ξ_S is the long channel surface potential. Hence after solving equation (4.33) we get

$$\Psi_S(y) = \xi_S + a_1 e^{\frac{y}{L_1}} + a_2 e^{-\frac{y}{L_1}} \qquad (4.34)$$

As observed from equation (4.34), L_1 represents the extension of the potential profile and is proportional to the thickness of gate oxide and the channel thickness. The natural length also describes the impact of the drain electric field on the channel. For the better suppression of SCEs, the gate length should be more than its natural length [181].

The short channel DG-JLFET is shown in Figure 4.4.

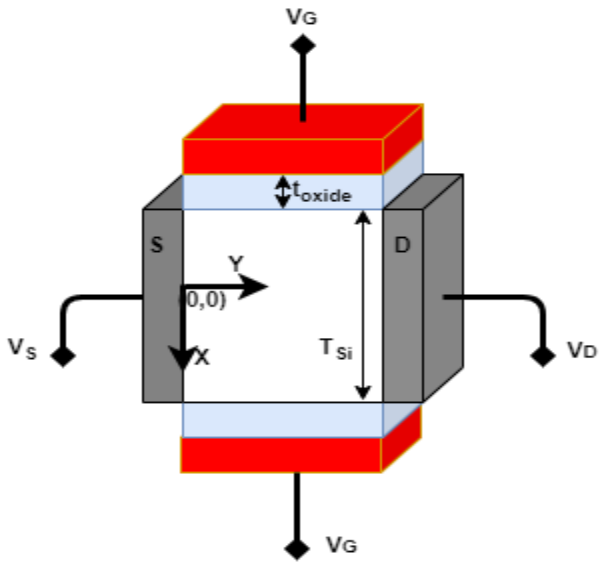

Figure 4.4: Short-channel DG-JLFET.

The Poisson's Equation is modified for the short-channel DGJLFETs as equation (4.1).

$$\frac{\partial^2\Psi(x,y)}{\partial x^2} + \frac{\partial^2\Psi(x,y)}{\partial y^2} = -\frac{\rho}{\epsilon_{Si}}$$

Considering boundary conditions and taking parabolic potential approximation we get

$$\Psi(x,y) = \Psi_0(y) + \frac{C_{OXIDE}}{\epsilon_{Si}\, t_{Si}}\left(V_G - V_F - \Psi_s(y)\right)x^2 \qquad (4.35)$$

By putting the value of Ψ_S from equation (4.32) to equation (4.35) and further solving we get

$$\frac{\partial^2\Psi_0(y)}{\partial y^2} - \frac{8C_{OXIDE}}{C_{OXIDE}\ t_{Si}^2 + 4\epsilon_{Si}\, t_{Si}}\left(\Psi_0(y) - V_G - V_F + \frac{qN_D\, t_{Si}}{2C_{OXIDE}} + \frac{qN_D\, t_{Si}^2}{8\epsilon_{Si}}\right) = 0 \qquad (4.36)$$

The equation (4.45) can be simplified by considering $1/L_2^2$=$8C_{oxide}/(4\epsilon_{Si}*t_{Si}+C_{oxide}t_{Si}^2)$, ξ_0=V_G-γ_2 and γ_2=V_F-$[(qN_At_{Si})/2C_{oxide}]$-$(qN_Dt_{Si}^2)/8\epsilon_{Si}$ [181]. Here L_2 is the natural length of DG-JLFET, ξ_0 is long channel central potential. The above equation can be simplified as

$$\frac{\partial^2\Psi_0(y)}{\partial x^2} - \frac{1}{L_2^2}(\Psi_0(y) - \xi_0) = 0 \qquad (4.37)$$

The solution of this differential equation is as

$$\Psi_0(y) = \xi_0 + a_1 e^{\frac{y}{L_2}} + a_2 e^{-\frac{y}{L_2}} \qquad (4.38)$$

The value of a_1 and a_2 can be obtained by using boundary conditions

$$a_1 = \beta_1 V_G + \beta_2 \qquad (4.39)$$

$$a_2 = \beta_3 V_G + \beta_4 \qquad (4.40)$$

Solving the above equation (4.46) we get the value of β_1, β_4, β_3 and β_4 as

$$\beta_1 = \frac{e^{-\frac{L_g}{L_2}} - 1}{2\sinh\left(\frac{L_g}{L_2}\right)} \qquad (4.41)$$

$$\beta_2 = \frac{V_{DS} - \gamma_2\left(e^{-\frac{L_g}{L_2}} - 1\right)}{2\sinh\left(\frac{L_g}{L_2}\right)} \qquad (4.42)$$

$$\beta_3 = \frac{1 - e^{\frac{L_g}{L_2}}}{2\sinh\left(\frac{L_g}{L_2}\right)} \qquad (4.43)$$

$$\beta_4 = \frac{-V_{DS} + \gamma_2\left(e^{-\frac{L_g}{L_2}} - 1\right)}{2\sinh\left(\frac{L_g}{L_2}\right)} \quad (4.44)$$

After calculating the value of a_1 and a_2, the expression for analytical relation can be solved. The minimum central potential location can be found by differentiating equation (4.38) [182]. The y_{min} is the location of the minimum central potential can be found as [182]

$$y_{min} = \frac{L_2}{2}\ln\left(\frac{a_2}{a_1}\right) \quad (4.45)$$

By putting the value of y_{min} in equation (4.38), the minimum central potential is

$$\Psi_0(y_{min}) = \sqrt{a_1 a_2} + \xi_0 \quad (4.46)$$

As in JLFET, when a gate voltage is equal to threshold voltage the channel starts to open [183]. Hence at threshold voltage the $\Psi_0(y_{min})=0$. For short-channel DG-JLFETs threshold voltage is given as

$$V_{Th} = \frac{2(\beta_2\beta_3 + \beta_1\beta_4) + \gamma_2 + \sqrt{(2(\beta_2\beta_3 + \beta_1\beta_4) + \gamma_2)^2 - (1 - 4\beta_1\beta_3)(\gamma_2 - 4\beta_2\beta_4)}}{(1 - 4\beta_1\beta_3)} \quad (4.47)$$

The analytical modeling solution for the threshold voltage for short channel DG-JLFETs is given by Equation (4.47). In the case of long channel DG-JLFETs, the value of β and γ =0. Hence, the threshold voltage for short channel DG-JLFET tends to ω_2, which is equal to the threshold voltage obtained for long channel DG-JLFET.

For DGJLTFET mobile electron concentration is given by [181]

$$n = N_D e^{\frac{\emptyset - v}{v_t}} \quad (4.59)$$

Ignoring the contribution of hole the Poisson's equation can be modified as

$$\frac{d^2\varphi}{dx^2} = \frac{qN_D[e^{\frac{\emptyset - v}{v_t}} - 1]}{\varepsilon_{Si}} \quad (4.60)$$

Solving equation we get

$$E(x)^2 = \frac{2qN_D V_t}{\varepsilon_{Si}}\left[e^{\frac{\emptyset - v}{v_t}} - \frac{\emptyset}{V_t}\right] \quad (4.61)$$

Using the boundary conditions for DGJLTFET equation electric field is given as

$$E_s^2 = \frac{2qN_D V_t}{\varepsilon_{Si}}\left[e^{\frac{\emptyset_s - v}{v_t}} - e^{\frac{\emptyset_0 - v}{v_t}} - \frac{\emptyset_s - \emptyset_0}{V_t}\right] \quad (4.62)$$

By applying a suitable approximation the value of the electric field given by equation (4.62) in DGJLTFET can be calculated.

In the previous section analytical modeling of surface potential and threshold voltage for the long channel JL-FET using parabolic approximation and short channel JL-FET using quasi-2D scaling technique was carried out. The dual-gate architecture is considered for modeling as this architecture gives one extra boundary condition to solve the differential equation easily. The general approach discussed here may be extended to other complex architectures.

4.7 NUMERICAL SIMULATION OF DOUBLE GATE JUNCTIONLESS FIELD EFFECT TRANSISTOR (DG-JLFET)

The numerical simulation of DG-JLFET at 32nm technology node is carried out using the Silvaco's TCAD tool. To improve the performance in DG-JLFET for the parameters such as off current, on current, trans-conductance, DIBL and threshold voltage, many gate and channel engineering approaches are adopted. The gate dielectric materials are required mainly for having good insulating properties and high capacitance value. The gate dielectric materials should be able to prevent the diffusion of dopant. These materials should have good thermal stability and very good interface adhesion with the substrate. However, the utilization of high-k materials improves the control of the gate and results in the reduction of SCEs along with all of the above qualities.

The performance of the DG-JLFET device can be further enhanced by introducing high-k dielectric gate materials. With the increasing value of dielectric, the value of DIBL is found to be decreasing exponentially which indicates suppression of SCE [184-187]. The transconductance of the devices also improves with high-k dielectric material utilization. An approach of using high-k dielectric is introduced in the 32nm

DG-JLFET to suppress the leakage current and the Short Channel Effects in this work. The structures considered for numerical simulations are having the gate oxide as SiO_2, HfO_2 and stack architecture of SiO_2 and HfO_2. These numerical simulations are done with the intention to analyse the characteristics of the device.

4.7.1 N-type DG-JLFET at 32 nanometres with SiO_2 as Dielectric Gate Material

The N-type DG-JLFETs at 32nm with (a) SiO_2 as dielectric material (b) Multi oxide (SiO_2+HfO_2) as dielectric material and (c) HfO_2 as dielectric material is shown in Figure 4.5. The physical thickness of oxide is taken as 2nm (in the case of multi oxide 1nm for SiO_2 and 1nm for HfO_2).

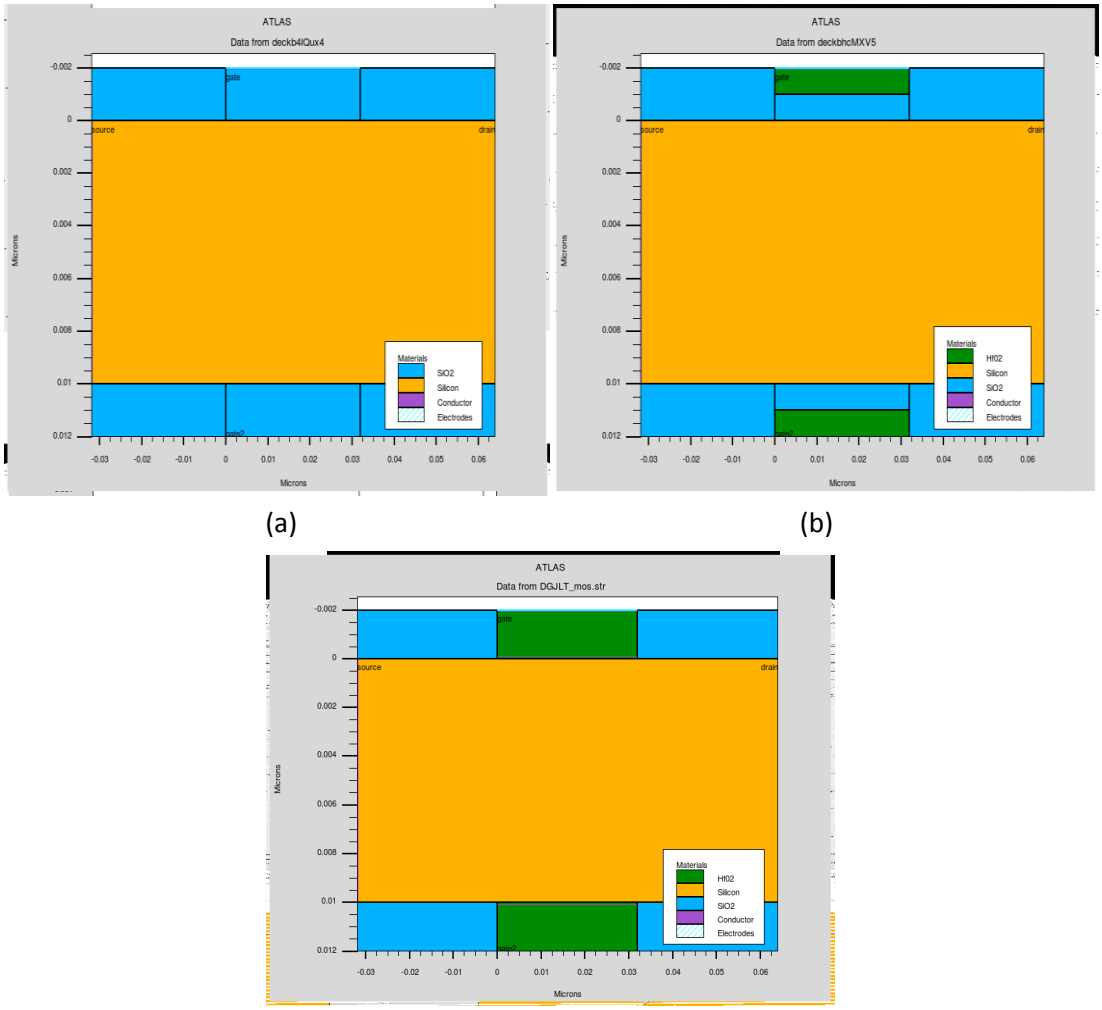

Figure 4.5: The N-type DG-JLFETs at 32nm with a dielectric material as (a) SiO_2 (b) Multi oxide (SiO_2+HfO_2) and (c) HfO_2

The work function of both gates material is taken as is 5.2ev. The silicon material is uniformly doped with n-type material with the doping density in the range of $1.5e^{-19}$ cm^{-3}. The permittivity of the HfO_2 is taken as 21 and the permittivity of the SiO_2 is taken as 3.9. The results were obtained using the Atlas device simulator and plotted on Tonyplot.

Figure 4.6 depicts the characteristics of drain current in saturation (high V_{DS}) on a logarithmic scale for different oxide materials. The characteristics of SiO_2 as the dielectric for gate oxide are shown with the red line, the green line shows the characteristics of multi-oxide as a dielectric material for the gate oxide and the blue line shows the characteristics of HfO_2 as a dielectric material for the gate oxide.

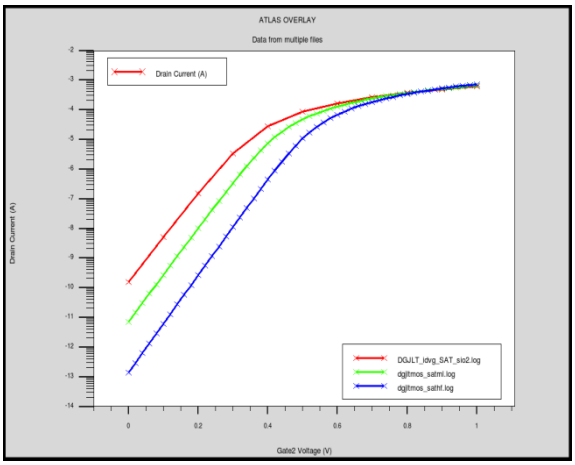

Figure 4.6: 32nm N-type DG-JLFETs transfer characteristics with SiO_2, Multi oxide and HfO_2 as gate dielectric materials.

It can be seen from Figure 4.6 that N-type DG-JLFETs architecture having HfO_2 (oxide permittivity=21) as dielectric material (blue line) has the lowest value of off current. The multi oxide has better off current properties than a device made only with SiO_2. It can also be observed that the on-current of all the devices is of the same order. The sub-threshold slope of the device can also be deduced from Figure 4.6 and it can be seen that the device having HfO_2 as a gate dielectric has the minimum sub-threshold slope among all compared here.

The detailed comparisons for the different dielectric materials obtained from numerical simulation are given in Table 4.1.

Table 4.1: 32nm N-type DG-JLFETs Characteristics with Different Oxide

Device	DG JLT with SiO2	DG JLT with Multi oxide	DG JLT with HfO2
V_{tsat}	0.293049	0.367348	0.456414
SS_{sat}	0.0661216	0.0628691	0.06094
I_{on}	0.000613	0.00066889	0.000737
I_{off}	1.587 e^{-10}	7.08627 e^{-12}	1.4025 e^{-13}
I_{on}/I_{off}	3.86 e^{+6}	9.4 e^{+7}	5.25 e^{+9}
V_{tlin}	0.324705	0.3987	0.474328
SS_{lin}	0.0664907	0.0632479	0.0611267
DIBL	0.033322	0.03302	0.0188568

4.7.2 Effect of High-k Material on Various Parameters for N-type DG-JLFETs

Table 4.1 shows the effects of high-k materials/ high-k materials in stack architecture for N-type DG-SOI MOSFET at 32nm. Some of the variations of characteristics parameters are analyzed as under.

4.7.2.1 Effect of high-k material on DIBL in N-type DG-JLFETs

The Drain Induced Barrier Lowering or DIBL is given by equation 3.3.

$$\text{DIBL} = \frac{V_{Th\,lin} - V_{Th\,sat}}{V_{sat} - V_{lin}}$$

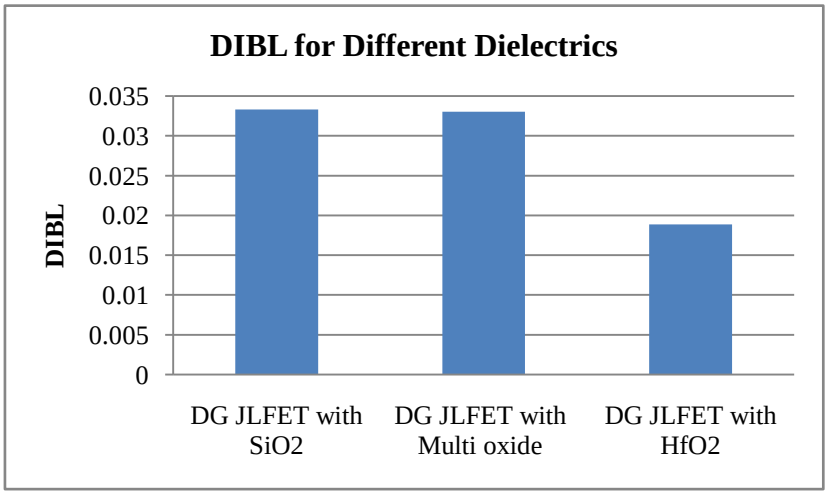

Figure 4.7: DIBL for 32nm N-type DG-JLFETs with different dielectric materials.

Here V_{sat} and V_{lin} are considered as 1.0V and 0.05V respectively. The $V_{th_{lin}}$ is the threshold voltage measured at V_{lin} and $V_{th_{sat}}$ is the threshold voltage measured at V_{sat}. Figure 4.7 shows the effect of high-k on DIBL for N-type DG-JLFETs.

4.7.2.2 Effect of high-k material on threshold voltage in N-type DG-JLFETs

In JLTFETs when the gate voltage is increased from zero, the channel starts to open. At a particular voltage, the depleted region in the middle of the channel vanishes due to the merged depleted region; this voltage is called threshold voltage for JLTFETs. At the threshold voltage, the inversion layer carrier density is equal to the bulk carrier concentration. The threshold voltage can be represented by equation (4.13).

$$V_{Th} = V_F - \frac{qN_D t_{Si}^2}{8\epsilon_{Si}} - \frac{qN_D t_{Si}\, t_{OXIDE}}{2\epsilon_{OXIDE}}$$

Here V_F is flat band voltage, q is the electron charge, N_D is donor doping concentration, ϵ_{Si} is the permittivity of silicon, t_{si} is the thickness of silicon channel in JLFET, t_{oxide} is oxide thickness and ϵ_{oxide} is the permittivity of gate oxide material. Figure 4.8 depicts the threshold voltage variation for the different dielectric.

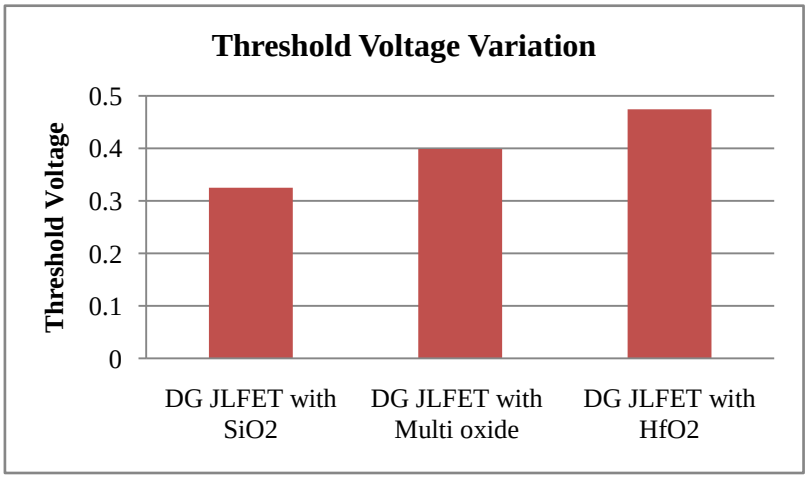

Figure 4.8: Threshold voltage variation with different dielectrics.

4.7.2.3 Effect of high-k material on the sub-threshold slope in N-type DG-JLFETs

As already discussed the sub-threshold slope (SS) is a significant design parameter related to MOSFET, it is usually described how fast a device can turn off from the on-state. The SS can be calculated as given by equation (3.7)

$$SS = \left(\frac{kT}{q}\right) ln_{10}\left(1 + \left(\frac{C_D}{C_{oxide}}\right)\right)$$

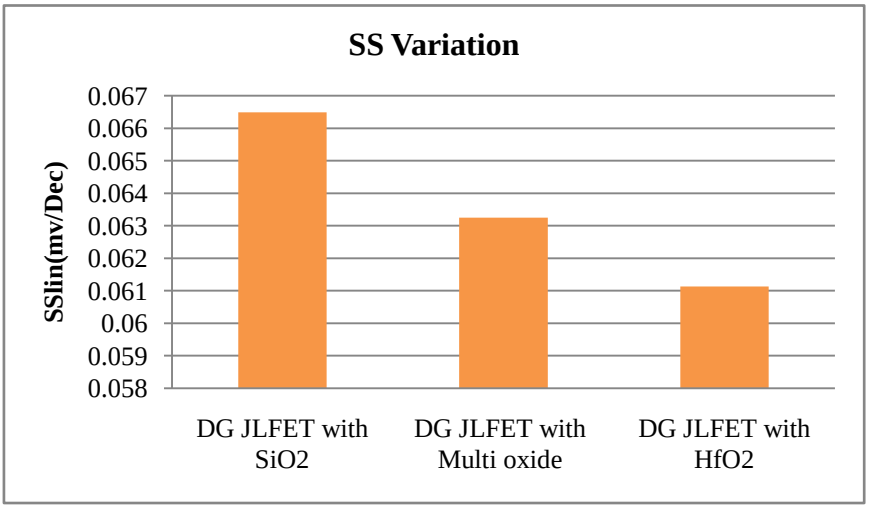

Figure 4.9: Sub-threshold slope variation with different dielectrics.

The SS depends on the first term only and has the ideal value of 60 mV/decade [188]. The effect of high- k materials on the sub-threshold slope of the 32nm DG-JLFETs is shown in Figure 4.9.

4.7.2.4 Effect of high-k material on I_{ON}/I_{OFF} current ratio in N-type DG-JLFETs

The variation of I_{ON}/I_{OFF} with different dielectric materials for 32nm N-type DG-JLFETs is shown in Figure 4.10. Figure 4.10 depicts DG-JLFETs with SiO_2 dielectric have a smaller value of I_{ON}/I_{OFF} ratio as compared to DG-JLFETs with high-k dielectric materials which can be attributed to the fact that strong depletion of a channel occurs with higher barrier potential in high-k devices [189].

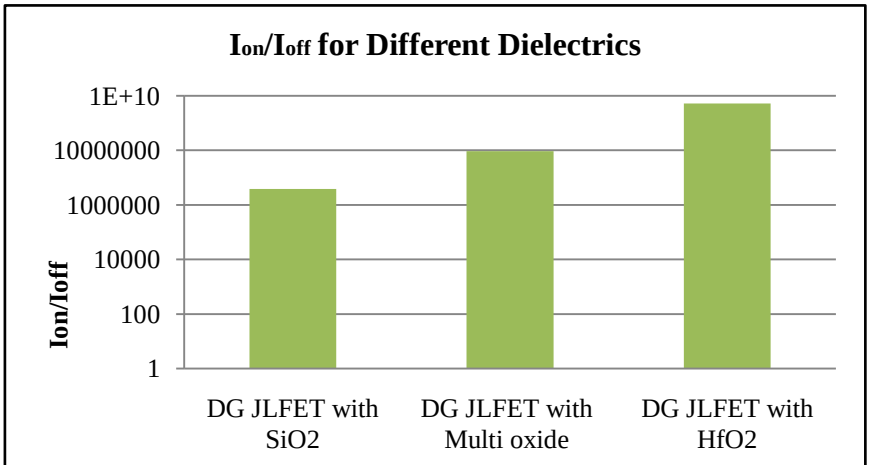

Figure 4.10: Variation of I_{ON}/I_{OFF} for DG-JLFETs with different dielectric materials

4.8 COMPARATIVE RESULTS ACROSS VARIOUS STRUCTURES FOR MULTIPLE OXIDES

The comparisons of transfer characteristics for all the structures of MOSFET viz. Bulk MOSFET, DG-SOI MOSFET and DG-JLTFET for various oxide viz. SiO_2, Multi oxide and HfO_2 are shown in Figure 4.11.

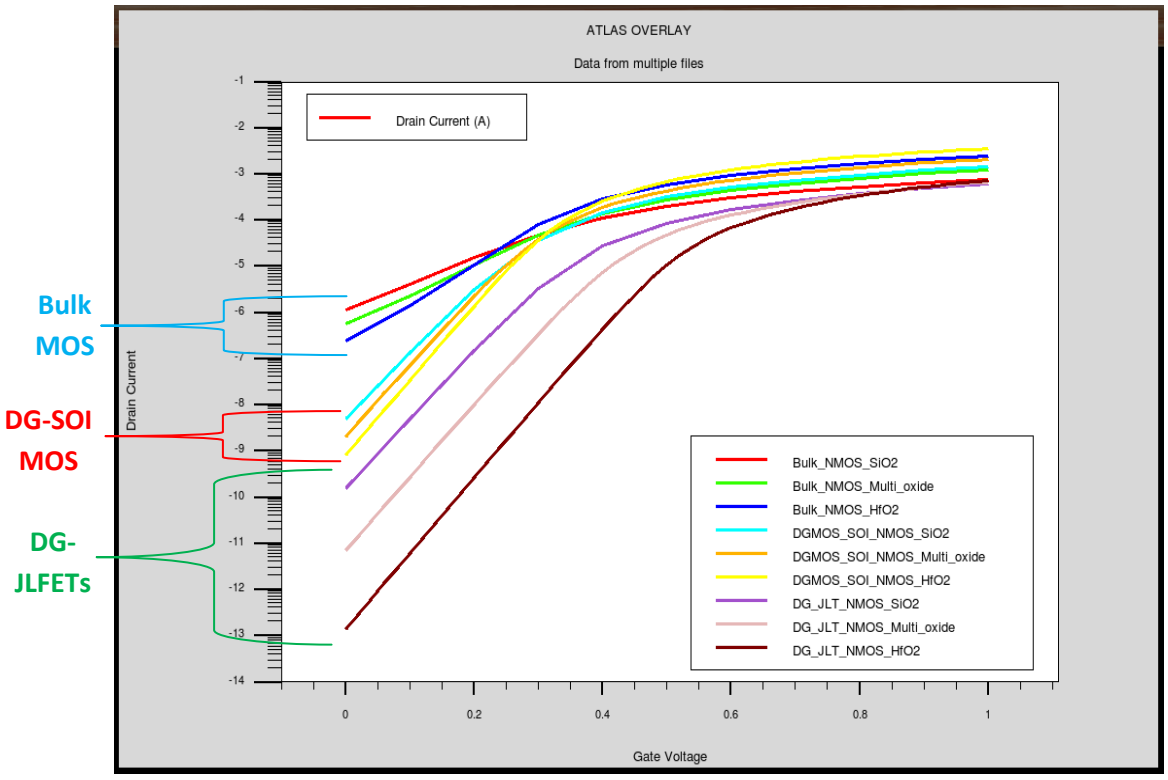

Figure 4.11: Transfer characteristics for all the structures for various oxides

Comparison of simulation results in Figure 4.11 was plotted on the Tonyplot tool of Silvaco's by overlaying Figure 3.17, Figure 3.27 and Figure 4.6. It can be seen from Figure 4.11 that the MOSFET made using DG-JLTs will give minimum off current and best slope among all compared for about the same order of on current. The DG-JLT MOSFET having gate dielectric is showing the best characteristics for the off current. Hence, the circuit made with DG-JLT MOSFET is expected to give minimum power dissipation. Figure 4.12 depicts the I_{on}/I_{off} ratio for various structures having different oxides as a gate dielectric.

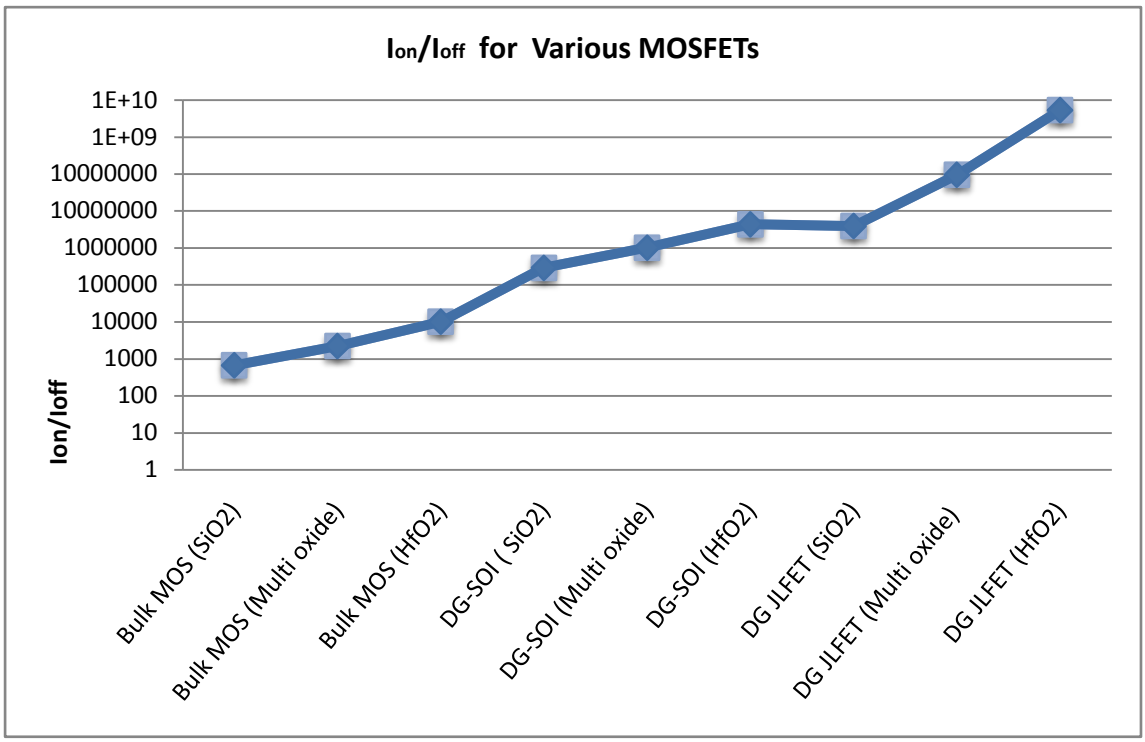

Figure 4.12: I_{ON}/I_{OFF} ratio for all the MOS structures

It can be seen from Figure 4.12 that the MOSFET made with DG-JLT has HfO_2 as dielectric giving a maximum on to off current ratio.

Figure 4.13 depicts the DIBL for various structures having different oxides as a gate dielectric. It can be seen that MOS structures made with DG-JLT and DG-SOI have almost the same minimum DIBL among the compared structures.

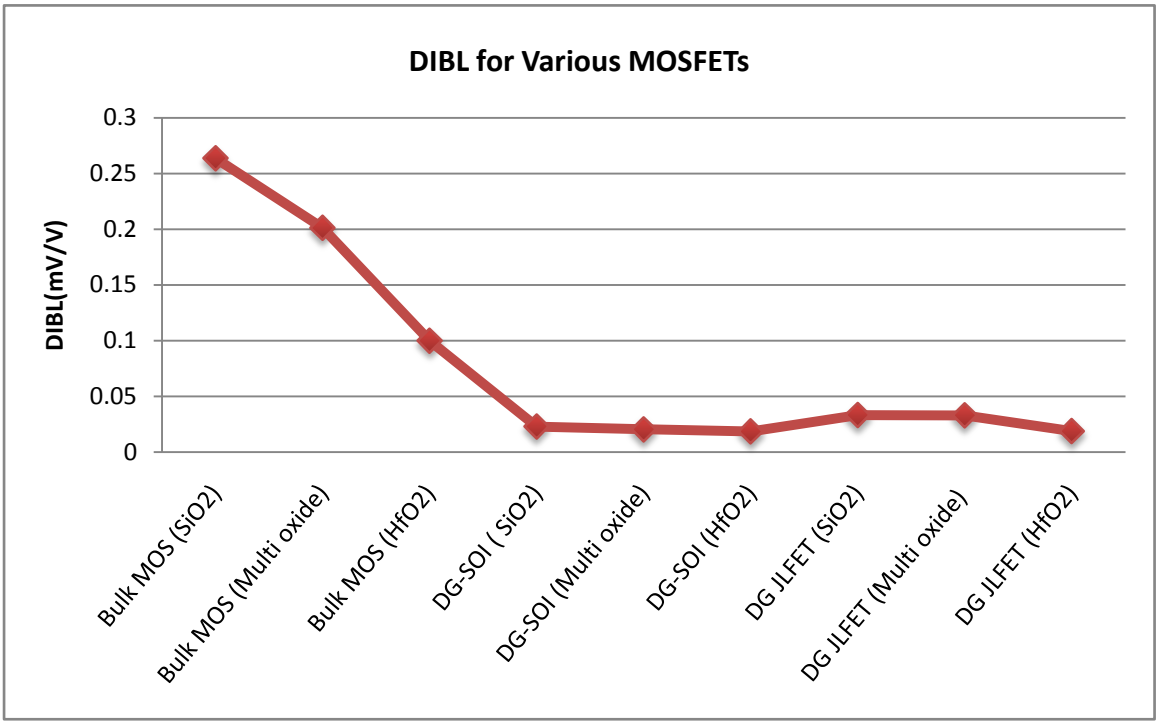

Figure 4.13: DIBL for various MOSFETs structures

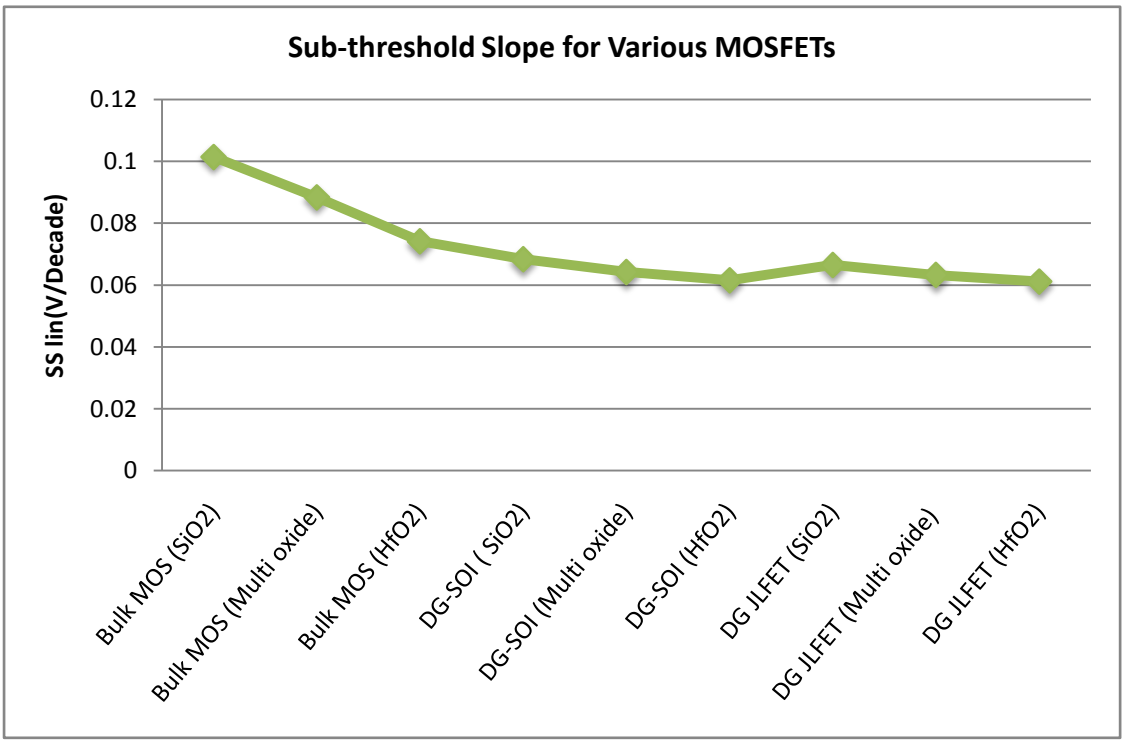

Figure 4.14: Sub-threshold slope for various MOSFETs structures

Figure 4.14 depicts the sub-threshold slope for various structures having different oxides as a gate dielectric. It can be seen that the MOS structure made with DG-JLT and DG-SOI has almost the same minimum sub-threshold slope close to perfect (60mv/Decade) among the compared structures.

4.9 RESULT AND DISCUSSION

The device features like surface potential and electric field have been analyzed by varying the device parameters like channel doping concentration, oxide thickness, drain bias, silicon thickness and work-function of the gate for the Junctionless Field Effect Transistor having HfO_2 as the gate dielectric.

4.9.1 Surface Potential

The electrostatic potential developed due to the presence of surface-confined charges is known as surface potential. The surface potential profile for JLT devices is numerically simulated using Atlas Device Simulator. These simulated surface potential profiles were compared with the surface potential profile developed from the analytical models. The following section discusses the variation in surface potential profile with various parameters.

4.9.1.1 Oxide thickness variation

The variation in surface potential along the channel length for various oxide thicknesses is shown in Figure 4.15. The various values of surface potential are simulated and plotted for the oxide thickness of 2 nm, 3 nm and 5 nm. The data is in close agreement with the analytical results.

As depicted in Figure 4.15, the surface potential reduces with the reduction in the thickness of gate oxide. This reduction in surface potential causes the reduction in DIBL due to the better electrostatic control of the gate for a thin gate dielectric. Hence, it results in suppression of Short Channel Effects (SCEs).

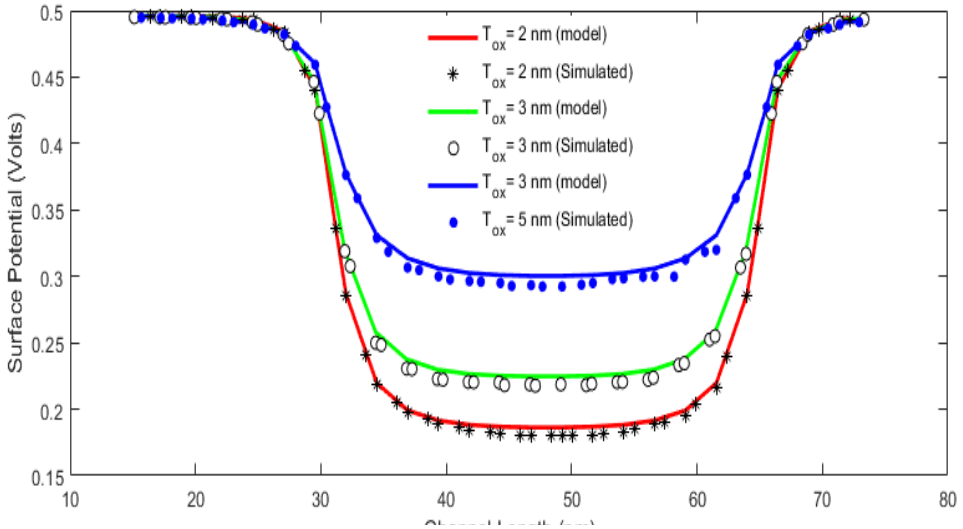

Figure 4.15: Variation in surface potential profile along with channel length for various oxide thicknesses

4.9.1.2 Silicon channel thickness variation

The deviation in surface potential along the channel length for various silicon channel thicknesses is shown in Figure 4.16.

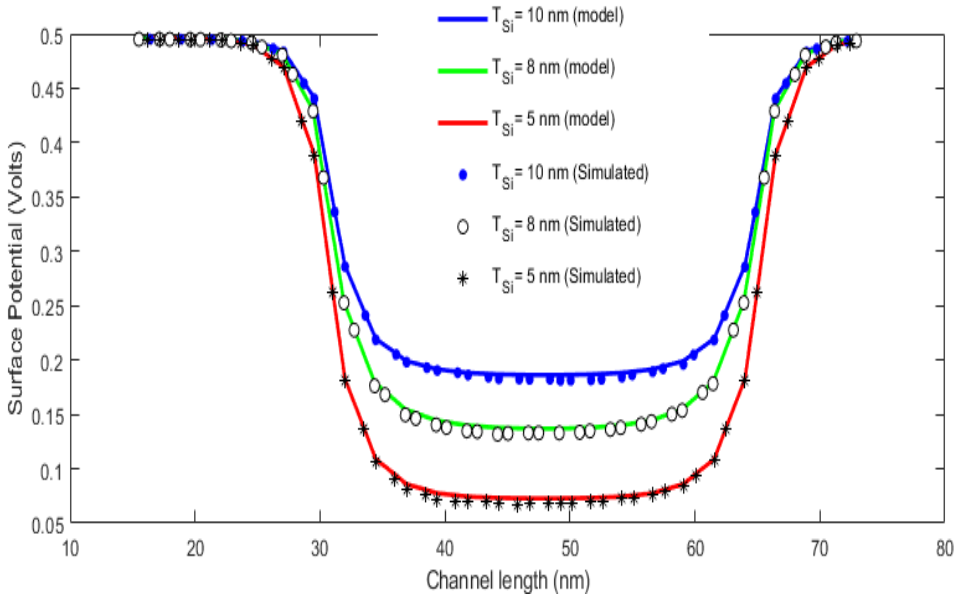

Figure 4.16: Variation in surface potential profile along with channel length for various silicon channel thicknesses

The various values of surface potential are simulated and plotted at the channel thickness of 5nm, 8nm and 10 nm. The simulated value is in good agreement with the analytical results. It can also be seen from the Figure as the thickness of the silicon channel increases the surface potential decrease. It is due to the better control of the thin channel by the gate.

4.9.1.3 Variation of drain to source bias

The deviation in surface potential along the channel length for the various drain to source bias is shown in Figure 4.17. The various values of surface potential are simulated and plotted at the drain to source bias values of 0.1V, 0.5V and 1.0V. The simulated value is in good agreement with the analytical results. The metal gate having high work-function minimizes the effects of drain to source bias variation. As can be seen from Figure 4.17 the effects of bias variation are prominent on the drain side and almost the same surface potential profile exists towards the source side.

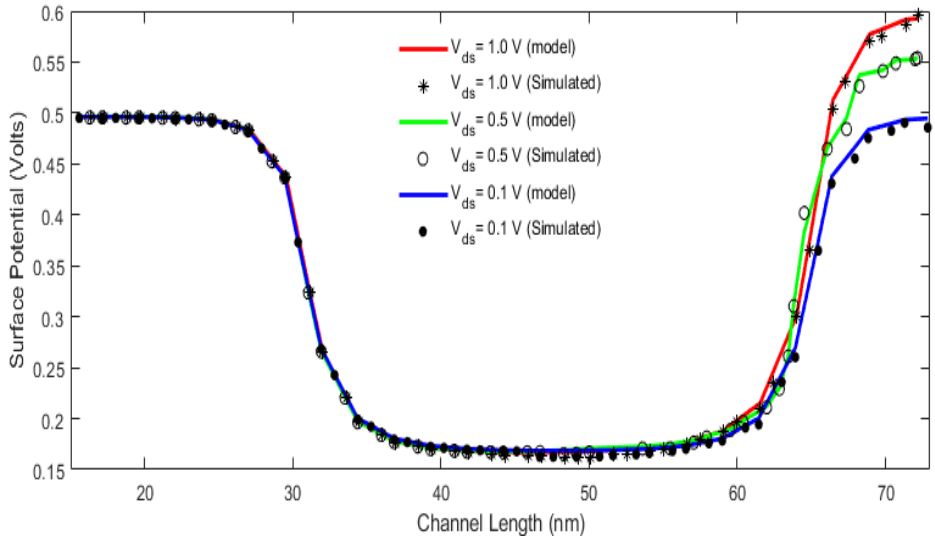

Figure 4.17: Variation in surface potential profile along with channel length for the various drain to source bias

4.9.1.4 Variation in Channel doping

The deviation in surface potential along the channel length for different values of channel doping is shown in Figure 4.18. The various values of surface potential is simulated and plotted for different channel doping value of $1e^{-19}$ cm^{-3}, $1.25e^{-19}$ cm^{-3}

and $1.5e^{-19}$ cm^{-3}. As can be seen from Figure 4.18, the simulated value is in good agreement with the analytical results. It can also be observed that with the decrease in doping concentration the value of surface potential decreases as the lower doping concentration results in the efficient depletion of the channel and effective suppression of the SCEs [190]

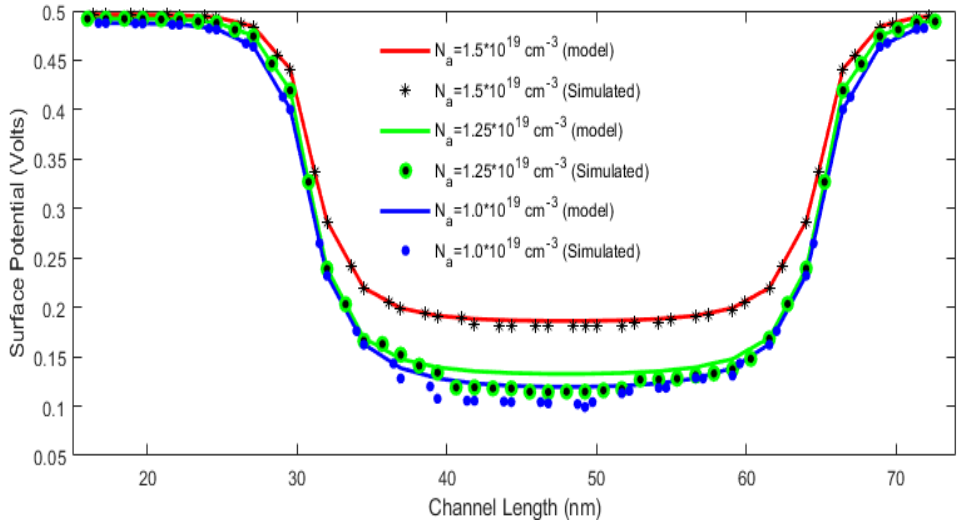

Figure 4.18: Variation in surface potential profile along with channel length for various channel doping

4.9.1.5 Variation in gate work-function

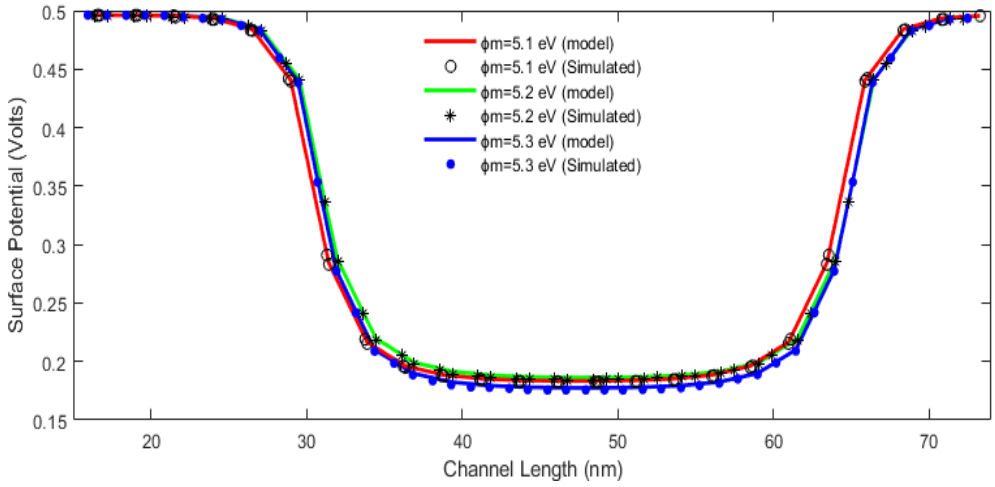

Figure 4.19: Variation in surface potential profile along with channel length for various gate work-function

The deviation in surface potential along the channel length for different values of gate work-function is shown in Figure 4.19. The various values of surface potential are simulated and plotted for different gate work-function values of 5.1eV, 5.2eV and 5.3eV. As can be seen from Figure 4.19, when the work-function of the gate increases the better control of the gate and efficient depletion of the channel is achieved.

4.9.2 Electric Field Distribution

The electric field for JLT having HfO_2 as a dielectric is determined and analyzed for various parameters. The electric field profiles are numerically simulated using Atlas Device Simulator. These simulated electric field profiles were compared with the electric field profile developed from the analytical models. The following section discusses the variation in electric field profiles with various parameters.

4.9.2.1 Oxide thickness variation

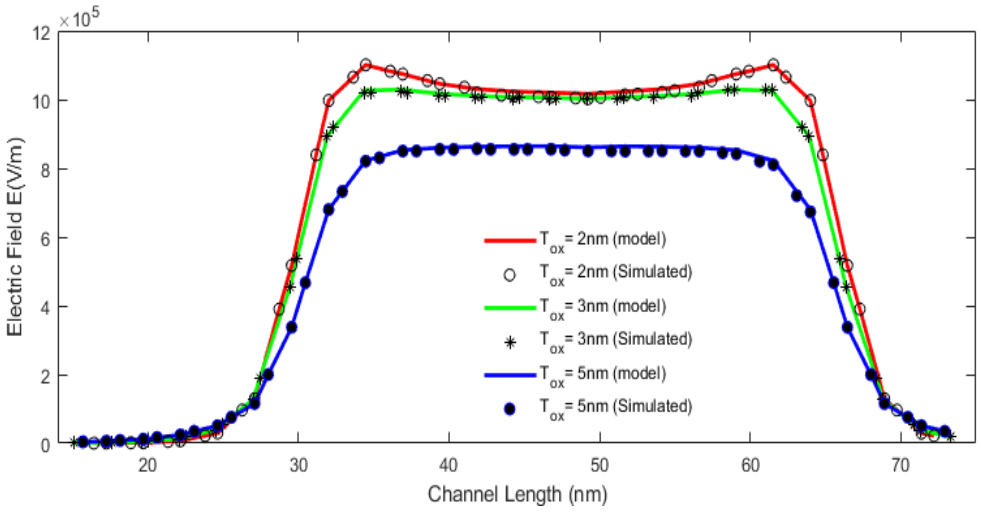

Figure 4.20: Variation in the electric field along with channel length for various silicon oxide thickness

The deviation in the electric field along the channel length for various oxide thicknesses is shown in Figure 4.20. The various values of the electric field are simulated and plotted at the oxide thickness of 2 nm, 3 nm and 5 nm. The data is in close agreement with the analytical results. It can be observed from Figure 4.20 that the lower values of oxide thickness produce the highest peak of the electric field. The

reduced oxide thickness also produces a large electric field which increases the average electric field.

4.9.2.2 Silicon channel thickness variation

The deviation in the electric field along the channel length for various silicon channel thicknesses is shown in Figure 4.21. The various values of the electric field are simulated and plotted at the oxide thickness of 5nm, 8nm and 10 nm. The simulated values are found in good agreement with the analytical results.

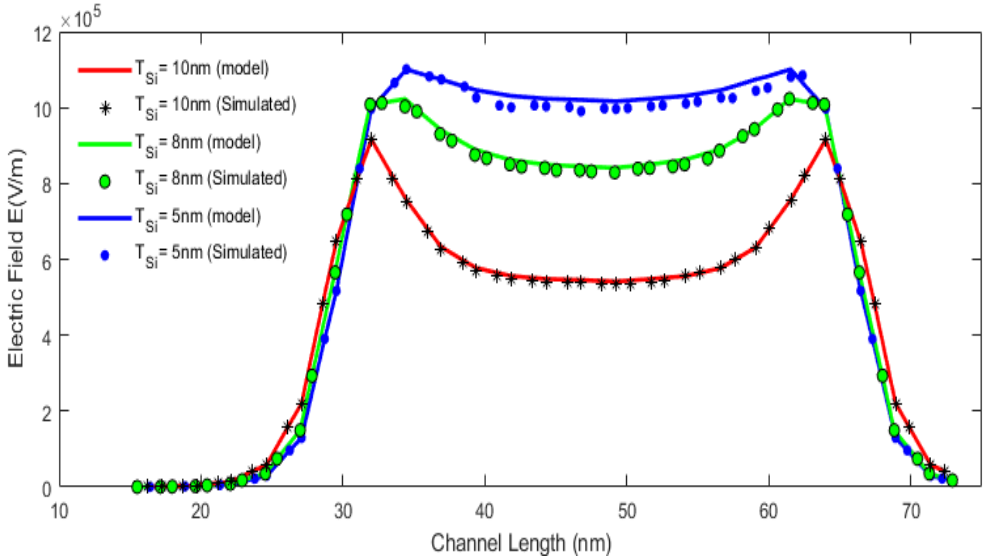

Figure 4.21: Variation in the electric field along with channel length for various silicon channel thickness variation

It can be seen from the Figure that the thickness of the silicon channel decreases with the increase in an electric field is observed. It indicates the reduction in the value of DIBL and SCEs.

4.9.2.3 Variation of drain to source bias

The deviation in the electric field along the channel length for the various drain to source bias is shown in Figure 4.22. The electric field is simulated and plotted at the drain to source bias values of 0.1V, 0.5V and 1.0V. The simulated value is in good agreement with the analytical results.

It can be seen from Figure 4.22 the peak of the electric field is located inside the drain, which minimizes the chances of electrons going into the oxide layer and acting as the hot electron. Hence overall reduction in the effect of the hot electron is observed in JLTs. It can also be seen that the value of the electric field is less for V=0.1 V and V=1V but the highest for V=0.5 V, this is due to the existence of drain voltage stress-induced degradation at lower voltage in JLTs and higher impact ionization rate at high drain bias [188].

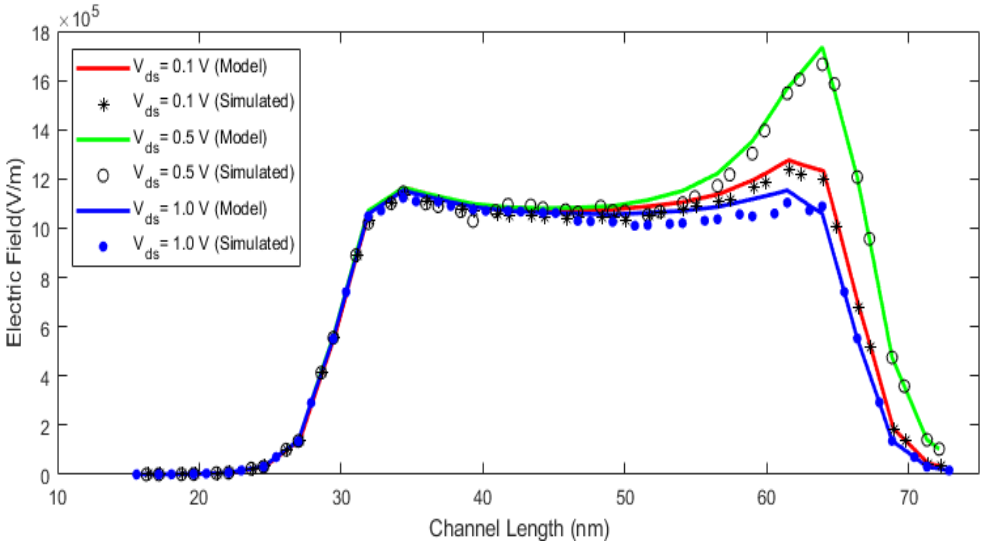

Figure 4.22: Variation in the electric field along with channel length for the various drain to source bias

4.9.2.4 Variation in Channel doping

The deviation in the electric field along the channel length for different values of channel doping is shown in Figure 4.23. The electric field is simulated and plotted for different channel doping value of $1e^{-19}$ cm^{-3}, $1.25e^{-19}$ cm^{-3} and $1.5e^{-19}$ cm^{-3}. As can be seen from Figure 4.23, the simulated value is in good agreement with the analytical results. The lower doping concentration in the channel suggests efficient depletion in the channel during off state. The reduction in the electric field due to reduction in channel doping can be interpreted as a reduction in SCEs.

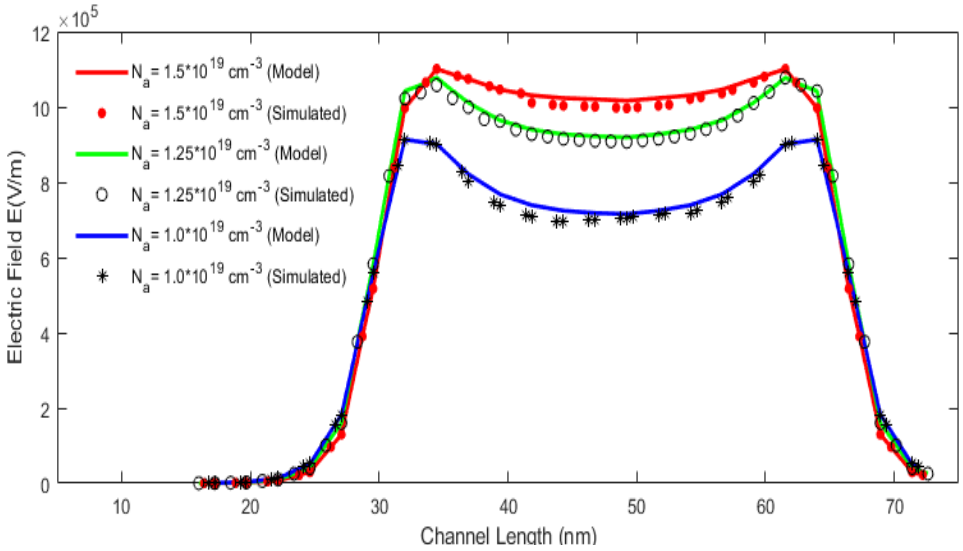

Figure 4.23: Variation in the electric field along with channel length for various channel doping

4.9.2.5 Variation in gate work-function

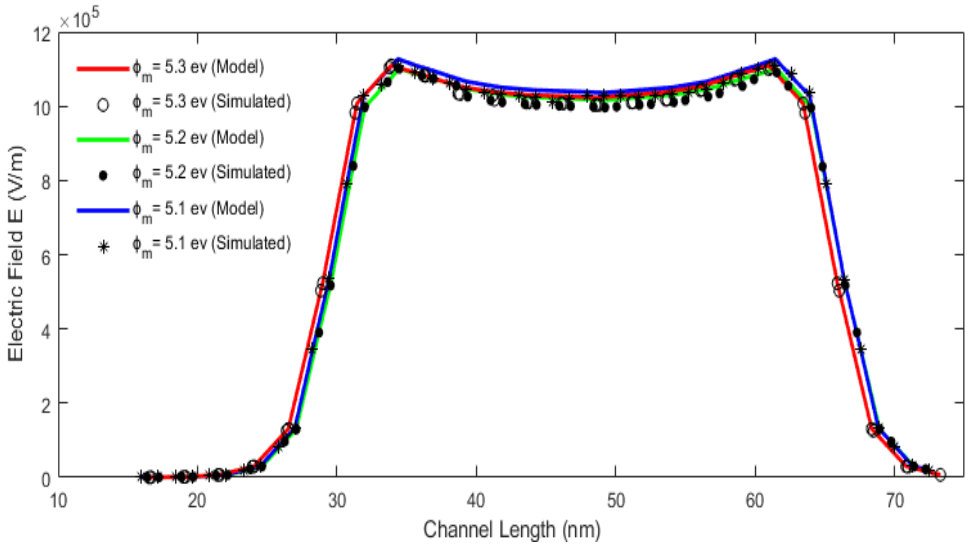

Figure 4.24: Variation in the electric field along with channel length for various gate work-function

The deviation in the electric field along the channel length for different values of gate work-function is shown in Figure 4.24. The electric field is simulated and plotted for different gate work-function values of 5.1eV, 5.2eV and 5.3eV. As can be seen from Figure 4.24, there is not much significant difference in electric field due to the

variation of the work function. It shows that the electric field is almost independent of the work function of the gate.

4.10 CONCLUSION

This chapter discusses the basics of the junctionless transistor and various parameters which affect its performance. The analytical modeling for surface potential and threshold voltage was developed in this chapter. The numerical simulation of JLFET is also carried out in this chapter. The simulation includes the application of HfO_2 and multi-oxide (SiO_2+HfO_2) as gate dielectric to analyse the characteristics of JLTs. Finally, the variation of surface potential profile and electric field with different parameters is carried out using Atlas and the results were also validated by analytical modeling.

CHAPTER-V

ANALYTICAL MODELING OF SUBTHRESHOLD CURRENT FOR SD-TM-CGAA-JLFETDEVICE FOR LOW POWER CMOS INVERTER

5.1 INTRODUCTION

The recent research in the field of semiconductor devices is biased toward alternate device structures that will provide the advantages of reduced power, reduced area and enhanced performance. There have been many devices structures that are architecturally modified to fulfill the objectives in recent years. The design approaches like Gate Engineering, Device Engineering and Channel Engineering have been explored extensively. The prime objective of all these design modifications is to decrease the Short Channel Effects which arises when the dimension of the MOSFET devices are reduced [88]. These SCEs hinder the further downscaling of the MOSFET devices. The multi-gate structure such as Double Gate (DG), Triple Gate and Surrounding/ Cylindrical Gate All Around (CGAA) MOSFETs device structures are being experimented with. The multi-gate device structures are found to have low leakage current, higher current drive capability and high packaging density in comparison to conventional MOSFET as reported in various literature [43, 50,109,121]. The advantages of multi-gate structures can be attributed to better electrostatic control over the channel region.

Other approaches to reduce the SCEs and enhance the performance of the MOSFET devices include the usage of the multi-metal gate in place of the conventionally used gate made up of single metal. Single metal gates (SMG) used over the year have constraints for further scaling [57]. Long et al. [191] initially introduced the concept of a multi-metal gate. Gate Metal Engineering also includes the device structures in which the gates are made from multiple materials having different work-function. Dual-Material Gate (DMG) composed of the gate is made using two different materials. The two gates are known as the control gate and screen gate. The control gate exists near the source and the screen gate exists near the drain side. The metal

near to source side has high work functions as compared to metal near to drain. The work-function of metal near-source is taken to be higher than the work-function of metal used near the drain to create a step in the potential profile. This potential profile step results in the enhancement of carrier transport efficiency and accordingly the gain of the semiconductor device also increases [52, 58]. The channel has a peak electric field due to the variation in the work function difference and it increases the electric field close to the source side and reduces the variation in potential near to drain side. In the source region, carrier velocity accelerates which further decreases the hot carrier effects [51]. To further reinforce the immunity against SCEs, Triple Metal MOSFET structures were proposed by various researchers. [192-195].

The other proposed methods to increase the gate control over the channel include the utilization of high-k materials as a gate dielectric [81, 84, 136]. The scaling requires that the oxide thickness should be decreased in the same proportion as the channel length. SiO_2 has been the primary gate insulator for a MOSFET. The thinner gate oxide provides large oxide capacitances, high drain current and reduced threshold voltage roll-off. However, if the thickness of gate oxide is reduced then gate leakage current will increase tremendously. This has led to the usage of high-k materials as gate dielectric. These high permittivity materials give more physical thickness along with a smaller effective oxide thickness (EOT) [196]. The stacked dielectric structure where a high-k dielectric material is deposited over SiO_2 reduces the gate leakage and improves the carrier transport efficiency in the channel.

The device structure of the Junctionless transistor as discussed in the previous chapter is simple to fabricate as the JLT devices do not have any junction and hence the ultra-sharp doping profile for short channel devices is not required. It also offers efficient characteristics in terms of the reduction of SCEs.

A design after considering the advantages offered by multi-gate approach (cylindrical gate all around MOSFET) with multi-metal gate approach (triple material) and high-k approach (stacked dielectric) as well as easy to fabricate junctionless device structure, a new device structure having stacked Dielectric Triple Material Cylindrical All-Around Gate Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET) is presented to further enhances the electrical characteristics performance. The

performance of the device is investigated for leakage current or the off current so as to implement the low power circuit.

5.2 DEVICE STRUCTURE

Figure 5.1 depicts a 3-D view of the SD-TM-CGAA-JLFET device. The cross-sectional view of the device is shown in Figure5.2. It can be noted that the gate terminal has three metal gates namely M_1, M_2 and M_3 having different work-function. The device has a work-function of M_1 (Gold) as 5.4 eV, a work-function of M_2 (Molybdenum) as 5.3eV and a work-function of M_3 (Titanium) as 5.2 eV. The SiO_2 thickness (t_{Sio2}) is kept as 1 nm and the thickness of high-k dielectric (t_{HfO2}) is kept as 4 nm as the inner and outer oxide layers respectively as stack dielectric architecture.

This triple metal Cylindrical gate-all-around structure with stack dielectric names as SD-TM-CGAA-JLFET is made on Silicon material having uniform doping from source to drain of the same material in the range of $1e^{19}$ cm^{-3}. The numerical simulations have been carried out on the ATLAS 3D device simulator. The channel length is 30nm for the device. The radius of the device is taken as 5nm. The value of various parameters used for the simulation of NMOS is enlisted in table 5.1.

Table 5.1: List of Constants and their Values for NMOS

Constants	Value
Work function of M_1 (Gold)	5.4 eV
Work function of M_2(Molybdenum)	5.3 eV
Work function of M_3(Titanium)	5.2 eV
Thickness of oxide t_{SiO2}	1nm
Thickness of oxide t_{HfO2}	4nm
Substrate doping	$1e^{19}cm^{-3}$
Channel Length	30nm
Radius of the Device	5nm
Length of each Material gate	10nm
Permittivity of HfO_2	21

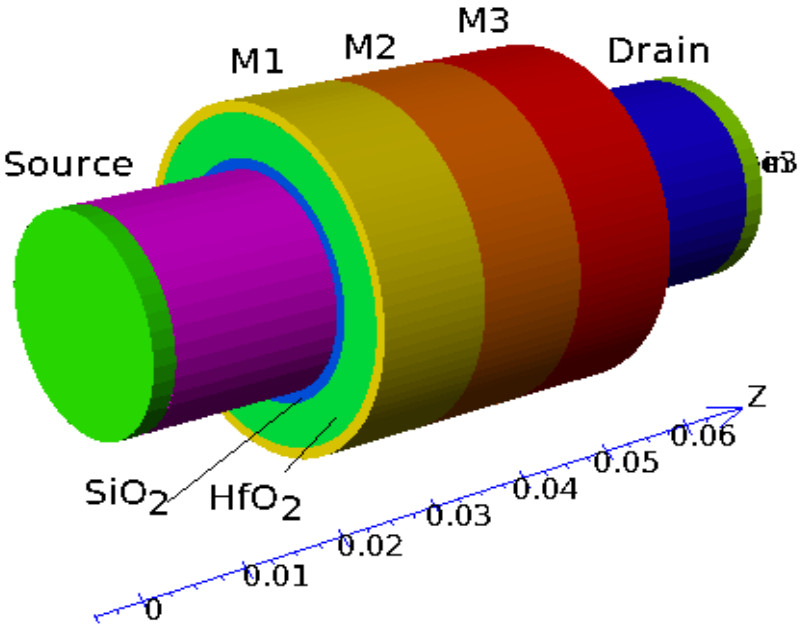

Figure 5.1: 3D View of SD-TM-CGAA-JLFET

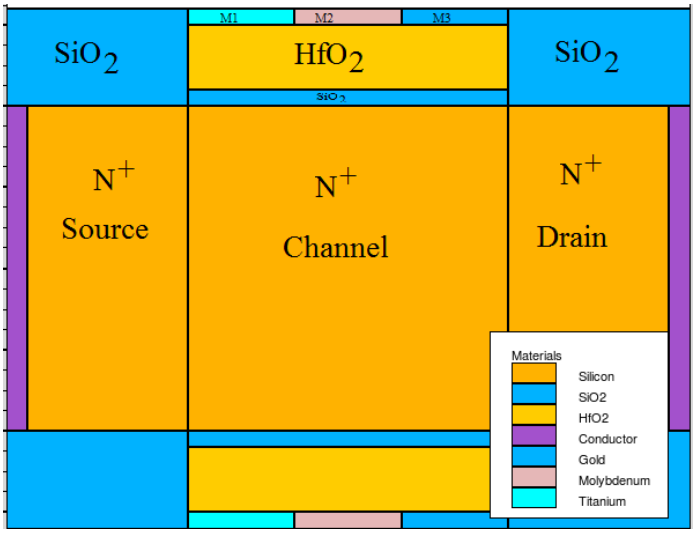

Figure5.2: Cross-sectional view of SD-TM-CGAA-JLFET

5.3 ANALYTICAL MODEL OF SD-TM-CGAA-JLFET

The length of the channel region and the diameter of the device is more than 30nm and 10 nm respectively hence, for the presented analytical model the quantum effects have been ignored [197]. SD-TM-CGAA-JLFET has been designed with the intention to take advantage of the low value of off current or sub-threshold current. Hence, the analytical model for sub-threshold current has been derived and reported in this chapter.

5.3.1Analytical Model for Sub-threshold Current

When the gate overdrive voltage is reduced below the threshold voltage a MOSFET device should not conduct and the drain current through it should be zero [113]. In practical devices, a small amount of current flows when the gate overdrive voltage is below threshold voltage and this current is known as the sub-threshold current. The low value of this sub-threshold current ensures that the circuit in which these semiconductor devices are employed will dissipate low power. Hence, it is very important to consider the sub-threshold behavior of a MOSFET.

The total current density is found by considering the drift and diffusion of current densities. Initially, the current flows from source to drain in the z-direction. Therefore, the total current density $J_C(r, z)$ is given by [198].

$$J_C(r,z) = -q\mu_n N_c(r,z)\frac{d\Psi_a(z)}{dz} \tag{5.1}$$

Where $N_C(r, z)$ is the charge carrier concentration and given by

$$N_c(r,z) = n_i e^{\frac{q\Psi_a(r,z)}{K_B T}} \tag{5.2}$$

Where $a = 1, 2, 3$for three-channel regions under the gate.

The subthreshold current can be obtained by integrating the total current density over the entire silicon thickness i.e. 0 to r. Here, the thickness of silicon (t_{si}) is the diameter of the cylindrical gate. Hence I_{sub} flowing along z-direction is

$$I_{sub}(z) = \pi t_{si}\int_0^{\frac{t_{si}}{2}} J_C(r,z)dr \tag{5.3}$$

Simplifying equation (5.3) we get

$$I_{sub}(z) = \frac{\pi\mu_n t_{si}\frac{K_B T}{q}\left[1-e^{\frac{-qV_{ds}}{K_B T}}\right]}{\int_0^L Q_a^{-1}(z).dz} \tag{5.4}$$

$$I_{sub}(z) = \left[\frac{\pi\mu_n t_{si}\frac{K_B T}{q}\left(1-e^{\frac{-qV_{ds}}{K_B T}}\right)}{\int_0^{L1} Q_1^{-1}(z)dz+\int_{L_1}^{L2} Q_2^{-1}(z)dz+\int_{L_2}^{L3} Q_3^{-1}(z)dz}\right] \tag{5.5}$$

L_1, L_2 and L_3 are the length of the channel under the metal M_1, M_2 and M_3 respectively and $Q_a(z)$ at $z=z_{a\,min}$is given by

$$Q_a(z) = 2\int_0^{\frac{t_{si}}{2}} \left(q\frac{n_i^2}{N_d} e^{\frac{q\Phi_a(r,z_{a\,min})}{K_B T}} \right) dr \qquad (5.6)$$

Solving the equation (5.6) by applying trapezoidal rule [199], which is used to state the integrals where piecewise linear curve method is utilized to approximate $Q_a(z)$ as for k = 1, 2, 3 and $1 \leq p \leq \infty$.

$$Q_a \approx \frac{t_{si}}{2p} q\frac{n_i^2}{N_d} \left(e^{\frac{q\Psi_a(r,z_{a\,min})}{K_B T}} + 2\sum_{m-1}^{p-1} e^{\frac{q\Phi_a\left(\frac{t_{si}}{2p},z_{a\,min}\right)}{K_B T}} + e^{\frac{q\Phi_a(0,z_{a\,min})}{K_B T}} \right) \qquad (5.7)$$

Simplifying the equation (5.5) using equation (5.7) as

$$I_{sub}(z) = \left[\frac{\pi\mu_n t_{si}^2 n_i^2 K_B T\left(1-e^{\frac{-qV_{ds}}{K_B T}}\right)}{\left[\frac{L_1}{M_1}+\frac{L_2}{M_2}+\frac{L_3}{M_3}\right]2pN_d} \right] \qquad (5.8)$$

$$M_1 = e^{\frac{q\Psi_a(r,z_{a\,min})}{K_B T}} + 2\sum_{m=1}^{p-1} e^{\frac{q\Psi_a\left(\frac{t_{si}}{2p}m,z_{a\,min}\right)}{K_B T}} + e^{\frac{q\Psi_a(0,z_{a\,min})}{K_B T}} \qquad (5.9)$$

As the SD-TM-CGAA-JLFET is having a symmetrical structure, the equation (5.9) can be simplified as [199]

$$M_a \approx e^{\frac{q\Psi_a(r,z_{a\,min})}{K_B T}} + e^{\frac{q\Psi_a(0,z_{a\,min})}{K_B T}} \qquad (5.10)$$

Or $M_a \approx 2e^{\,q\Psi a\,min/\,KBT}$ (5.11)

$$I_{sub}(z) = \left[\frac{\pi\mu_n t_{si}^2 n_i^2 K_B T\left(1-e^{\frac{-qV_{ds}}{K_B T}}\right)}{\left[\frac{L_1}{e^{\frac{q\Psi_{1\,min}}{K_B T}}}+\frac{L_2}{e^{\frac{q\Psi_{2\,min}}{K_B T}}}+\frac{L_3}{e^{\frac{q\Psi_{3\,min}}{K_B T}}}\right]N_d} \right] \qquad (5.12)$$

As from the structure, it can be observed that$\Psi_{3\,min} > \Psi_{2\,min} > \Psi_{1\,min}$. Hence equation (5.12) can be written as

$$I_{sub}(z) \approx \frac{\pi \mu_n t_{si}^2 n_i^2 K_B T\left(1-e^{\frac{-V_{ds}}{V_T}}\right) e^{\frac{\Psi_{1\,min}}{V_T}}}{L_1 N_d} \qquad (5.13)$$

Where $V_T = \frac{K_B T}{q}$ and the Boltzmann's constant K_B=1.38*10^{-23} J/K, intrinsic carrier density n_i=1.45*10^{10}cm^{-3}, electron mobility is μ_n=1076 cm^2/Vs and T=300K.

5.3.2 Sub-threshold Slope

The sub-threshold slope of the devices is defined as the gate to source voltage required to bring a one-decade decrease in current for a MOSFET. This factor also provides information about the speed of the device [200]. The sub-threshold slope is given by

$$SS = 2.303 \frac{K_B T}{q} \frac{1}{\frac{d\Psi_{1\,min}}{dv_{gs}}} \qquad (5.14)$$

$$\Psi_{1\,min} = 2\sqrt{\alpha_1 \alpha_2} - \frac{\chi_1}{\kappa^2} \qquad (5.15)$$

The values of α_1, α_2 are given as [201]

$$\alpha_1 = \alpha_5 + \frac{(M_4 - M_5)}{2\delta_4} + \frac{(M_3 - M_4)}{2\delta_3} + \frac{(M_2 - M_3)}{2\delta_2} + \frac{(M_1 - M_2)}{2\delta_1} \qquad (5.16)$$

$$\alpha_2 = \frac{(M_1 - M_2)\delta_1}{2} + \frac{(M_2 - M_3)\delta_2}{2} + \frac{(M_3 - M_4)\delta_3}{2} + \frac{(M_4 - M_4)\delta_4}{2} - \alpha_5 \delta^2 + (M_5 + V_{bi} + V_{ds})\delta \qquad (5.17)$$

The value of M_a, δ_a can be written as [199]

$M_a = \frac{\chi_a}{a^2}$ and $\delta_a = \exp(aL_a)$

$$\delta_a^{-1} = \exp(-aL_a) \qquad (5.18)$$

here a = 1,2,3 and $a^2 = \frac{2C_{ox}}{\varepsilon_{Si} R}$

$$\chi_1 = \frac{qN_{a1}}{\varepsilon_{si}} - a^2(V_{gs} - V_f) \qquad (5.19)$$

Where q is an electronic charge, ε_{Si} permittivity of silicon, V_{gs} is the gate to source voltage and V_f is the flat-band voltage for JLFET.

5.4 NUMERICAL SIMULATION OF SD-TM-CGAA-JLFET

SD-TM-CGAA-JLFET device is simulated using Silvaco's Device Simulator ATLAS at 30nm channel length. The transfer characteristics obtained from the simulation are shown in Figure 5.3. The dielectric is arranged in a stacked manner (one over the other), the SiO_2 layer of 1nm having good adhesive properties with Silicon is used inside and HfO_2, a high-k dielectric of 4nm is used outside of this SiO_2 layer. The permittivity of HfO_2 is taken as 21 and the permittivity of the SiO_2 is taken as 3.9. The three metals have varied work-function. The metal having the highest work function is arranged near to source so as to have greater charge carrier velocity [202]. The silicon material in the channel is uniformly doped. The simulation results were plotted on Silvaco's Tonyplot.

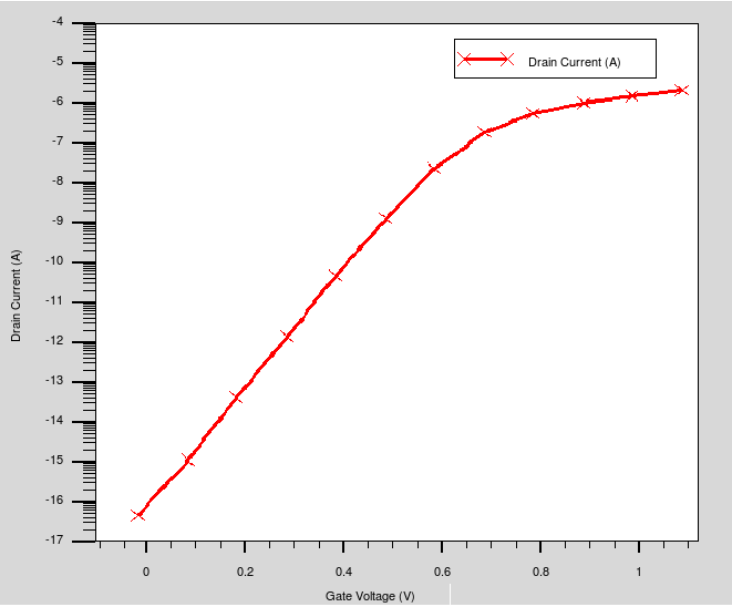

Figure 5.3: Transfer characteristics of SD-TM-CGAA-JLFET

The transfer characteristics of n-type SD-TM-CGAA-JLFET are shown in Figure 5.3 which is essentials for the prediction of on/off current and sub-threshold characteristics of MOSFET. The plotted transfer characteristics of the N-type SD-TM-CGAA-JLFET are shown for linear mode and it can be seen that the value of I_{sub} is in the range of $4.9e^{-16}$A.

5.5 RESULTS AND DISCUSSION

The sub-threshold current and sub-threshold slope of SD-TM-CGAA-JLFET are determined analytically and from the simulation is compared and analyzed with respect to various device parameters. The gate near to source is called the control gate to have the highest work function. The first screen gate has a moderate work function and finally the second screen gate near to drain has the lowest work function.

5.5.1 Sub-threshold Current

The sub-threshold current is simulated using ATLAS. The effects of various parameters on the sub-threshold current of the SD-TM-CGAA-JLFET structure are given below.

5.5.1.1 Silicon thickness variation

The variation in the value of off current with V_{gs} for various values of silicon channel (diameter of the cylindrical channel) thickness is shown in Figure 5.4. The thickness of the silicon channel varied from 5nm to 10nm. As observed from Figure 5.4, the off current increases when the thickness of the silicon channel increases. This increase in off current is due to the inefficient depletion of the channel in the center, better electrostatic control is applied when the thickness of the channel is small. A thicker device provides a good current drive but has a poor value of off current. Hence, the optimum value thickness of the channel is to be selected for appropriate on/off current in the practical application of the SD-TM-CGAA-JLFET device.

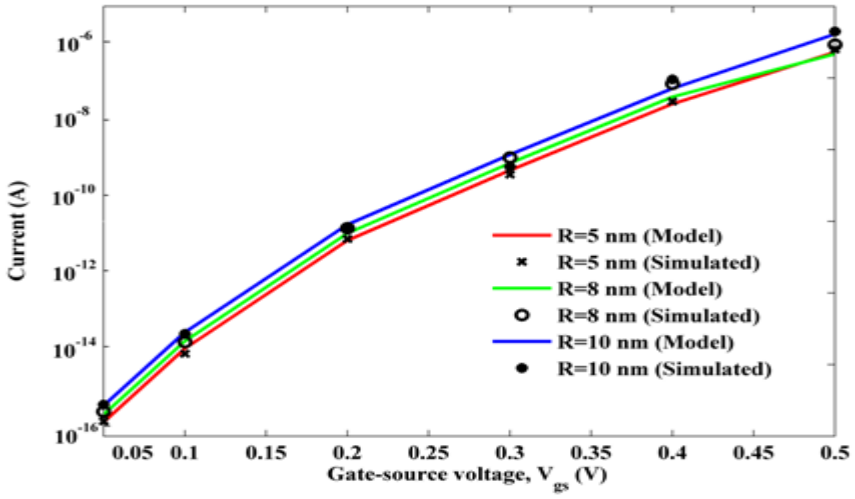

Figure 5.4: Variation in off current with V_{gs} for various silicon channel thickness

5.5.1.2 Channel doping variation

It can be seen from Figure 5.5 when the channel doping concentration increases the value of the off current reduces. The channel doping is varied from $0.5e^{-19}cm^{-3}$ to $1.5e^{-19}cm^{-3}$. This change in off current with the change in doping concentration is due to the velocity saturation of electrons at high doping conditions [203].

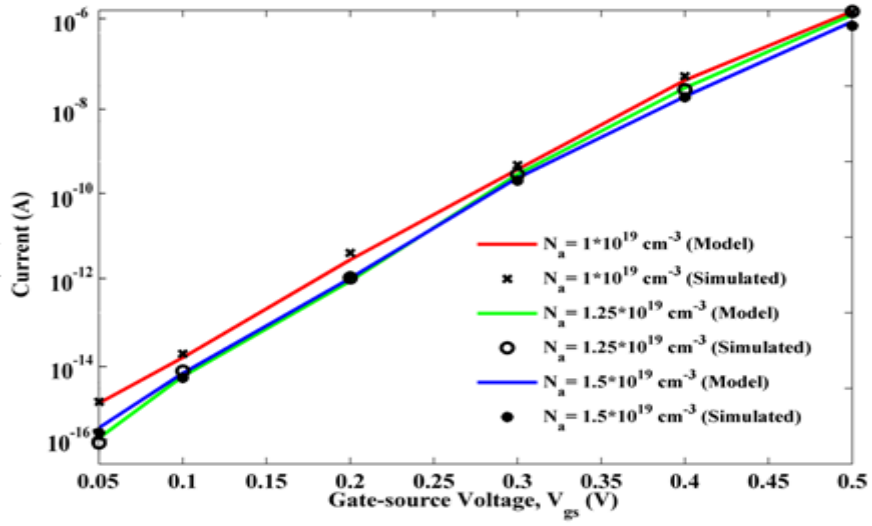

Figure 5.5: Variation in off current with V_{gs} for various channel doping concentrations

5.5.1.3 Oxide thickness variation

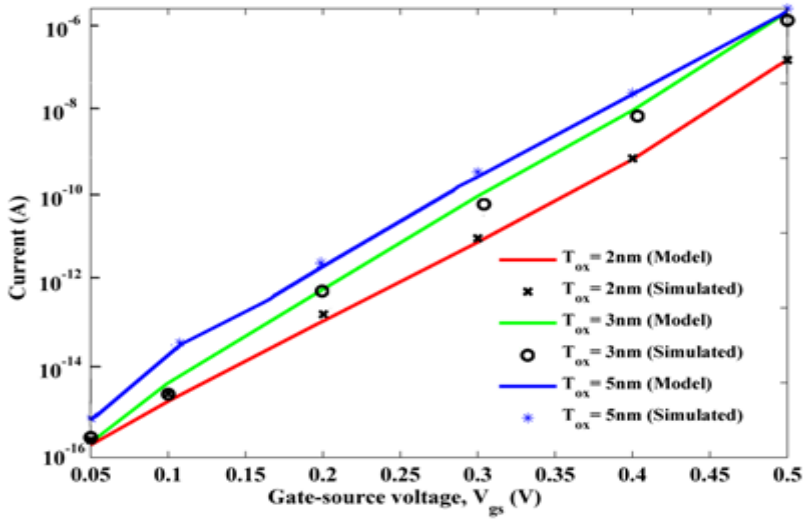

Figure 5.6: Variation in off current with V_{gs} for various oxide thicknesses.

The variation in the value of off current with V_{gs} for different oxide thickness variations in SD-TM-CGAA-JLFET is shown in Figure 5.6. The thickness of the

oxide is varied in the range of 2nm, 3nm and 5nm. It can be seen that with the increase in the thickness the value of the off current increases. It is due to the fact that a thicker oxide reduces the control of the gate on the channel. The value obtained from the analytical is also in close agreement with the simulated values.

5.5.1.4 Drain to source bias variation

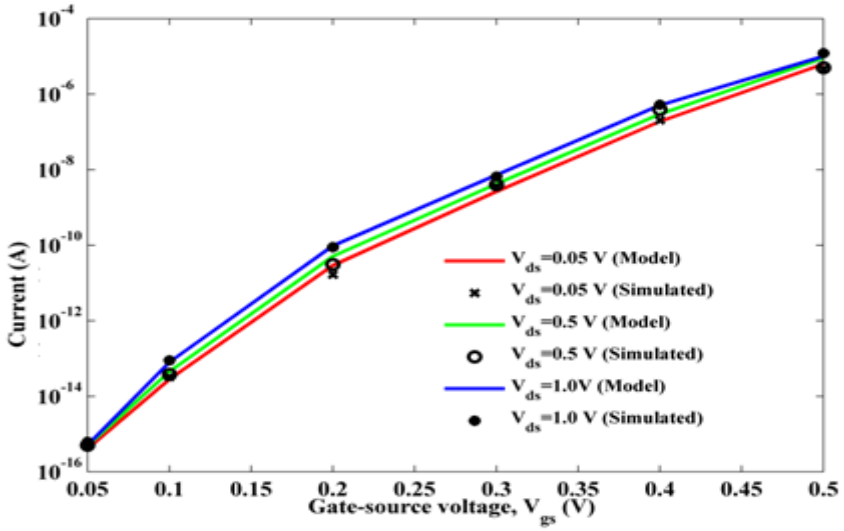

Figure 5.7: Variation in off current with V_{gs} for various drain biases.

The variation in off current with Vgs for various drain biases in the range of Vds=0.05 to 1V is shown in figure 5.7. The value of off current or sub-threshold current is neglected for long channel devices but its value cannot be neglected for short channel devices. As shown in Figure 5.7, the value of the off current was found to vary linearly with the V_{gs}. However, it can be seen that off current varies exponentially with V_{ds}. This variation in current is due to DIBL [204]. As the changes in V_{ds} moves the position of minimum surface potential [98]. The higher value of the off current will raise the power dissipation of the circuits in which this component is employed.

5.5.1.5 Channel length ratio variation

The variation in the value of off current with V_{gs} at various length ratios of triple gates used in SD-TM-CGAA-JLFET is shown in Figure 5.8. It can be seen that when the length of the control gate is increased the value of the off current reduces. Hence, the gate length ratio on 3:2:1 results in the lowest value of off current among the various reported length ratio. The analytical results are in close agreement with the simulated results.

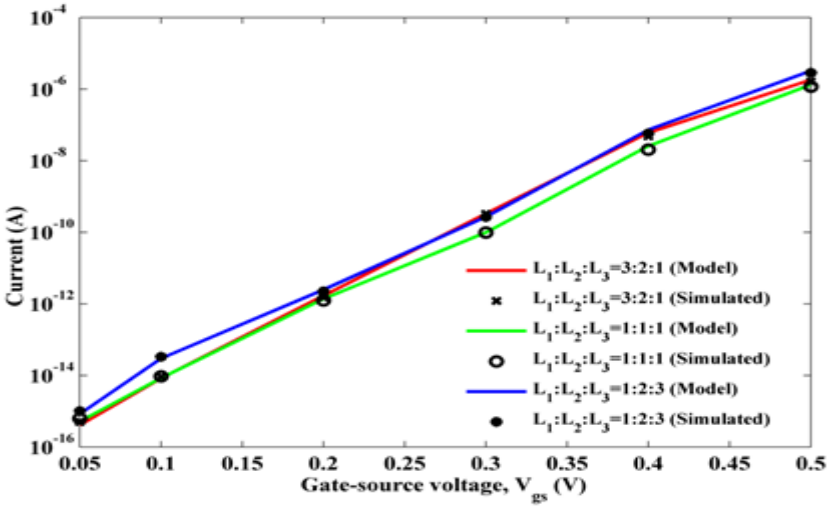

Figure 5.8: Variation in off current with V_{gs} for various device length ratios.

5.5.2 Sub-threshold Slope (SS)

The Sub-threshold slope of SD-TM-CGAA-JLFET MOSFETs is determined with respect to various device parameters and found by numerical simulation using ATLAS. The values computed from analytical expression are also closely matched to the simulated results. The value of the sub-threshold slope is considered for the linear region i.e. when the applied V_{ds} is low (0.1V). The value of SS is 62.34mV/decade for SD-TM-CGAA-JLFET. The sub-threshold slope of value 60 mV/decade is considered ideal and the simulated value and computed value of SS closely match with an ideal value of SS.

The analytical model of Stacked Dielectric Triple Material Cylindrical Gate-All-Around Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET) for sub-threshold current and the sub-threshold slope was developed and analyzed. The variation in device parameters like the thickness of silicon channel, channel length ratio, oxide thickness and doping concentration was carried out to analyze the behavior of off/sub-threshold current with gate to source voltage. It was observed that for all the variations in device parameters, a close agreement between simulation results and analytical results was found.

5.6 INVERTER CIRCUIT IMPLEMENTATION

A basic CMOS (Complementary symmetry Metal Oxide Semiconductor) inverter circuit is a circuit configuration composed of NMOS and PMOS transistor for the

implementation of NOT gate logic. CMOS inverter is having an important characteristic of low power dissipation. As one of the transistors is always in the off state so the inverter circuit draws power momentarily when it is switching between two states viz. on to off state or off to on state. The circuit diagram of the CMOS inverter circuit is shown in Figure 5.9.

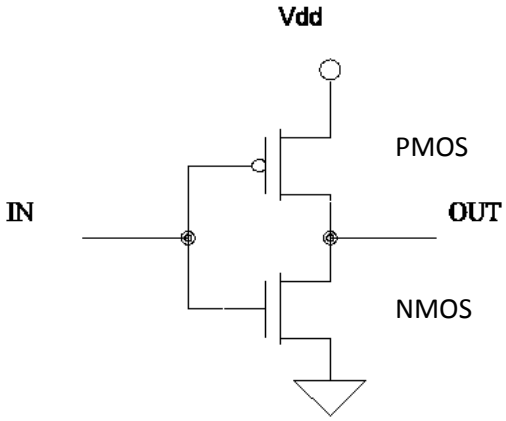

Figure 5.9: CMOS Inverter

A CMOS inverter is a basic building block of almost all the digital circuits hence applying any approach and analyzing its result will give us an idea about the whole family of digital circuits in general. It was found that the presented SD-TM-CGAA-JLFET device structure is offering a very low sub-threshold current hence; this device is utilized in the inverter circuit. The various characteristics of the CMOS inverter were analyzed using SD-TM-CGAA-JLFET type NMOS and PMOS structure. The estimation for static power dissipation for the inverter circuit was also carried out.CMOS inverter circuit also requires a compatible PMOS structure. Hence, a PMOS device based on the same SD-TM-CGAA-JLFET device approach was designed.

5.7 SD-TM-CGAA-JLFET BASED PMOS

PMOS device based on Stacked Dielectric Triple Material Cylindrical Gate All Around Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET) was designed and numerically simulated using device simulator ATLAS from Silvaco's TCAD. Since it was already established that SD-TM-CGAA-JLFET based NMOS device is using gate/channel/device engineering for efficient suppression of Short Channel Effects (SCEs) hence by using the comparative dimension, a PMOS device is

designed. The 3D structure of the device is the same as Figure 5.1 and the cross-section view is the same as Figure 5.2. The major differences which exist between PMOS and NMOS design include the nature of doping impurity and the work-function of the metal gate utilized in PMOS devices. The thickness of the Silicon channel has been modified to achieve the matching threshold voltage and current rating as an NMOS device.

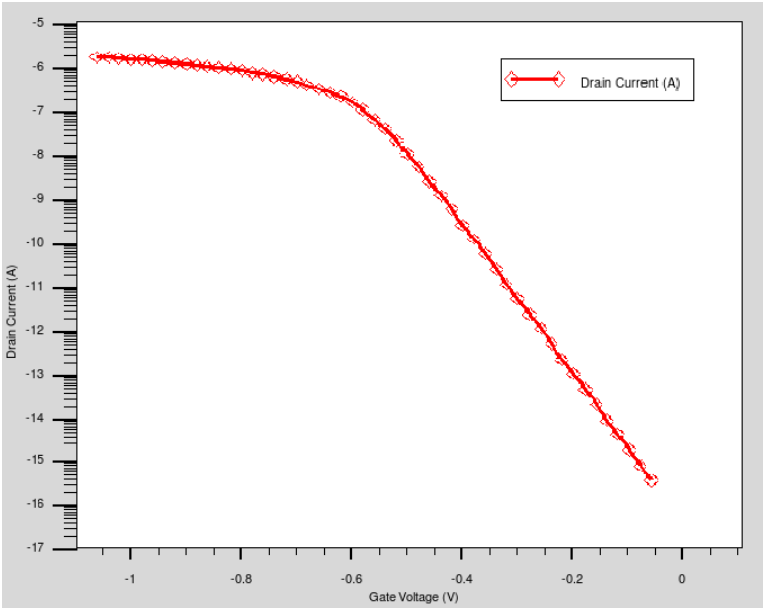

Figure 5.10: Transfer characteristics of the P-type SD-TM-CGAA-JLFET device

The transfer characteristics of p-type SD-TM-CGAA-JLFET are shown in Figure 5.10. These characteristics are essentials for the prediction of on/off current and sub-threshold characteristics of MOSFET. The plotted transfer characteristics of the P-type SD-TM-CGAA-JLFET are shown for linear mode and it can be seen that the value of I_{sub} is in the range of $3.98e^{-16}$A.

The above P-type device designed using the SD-TM-CGAA-JLFET approach is used in the CMOS inverter circuit along with the N-type SD-TM-CGAA-JLFET device.

5.8 CMOS INVERTER CHARACTERISTICS

The transient characteristics of the CMOS inverter are shown in Figure 5.11. These characteristics show a good response for the NMOS and PMOS devices during turning on and off. When the input is high, the NMOS is turned on and PMOS turned off which causes the low voltage at the output. In the other case, NMOS turned off

and PMOS turned on which caused the high voltage at the output. The switching speed is decided by the gate overdrive voltage.

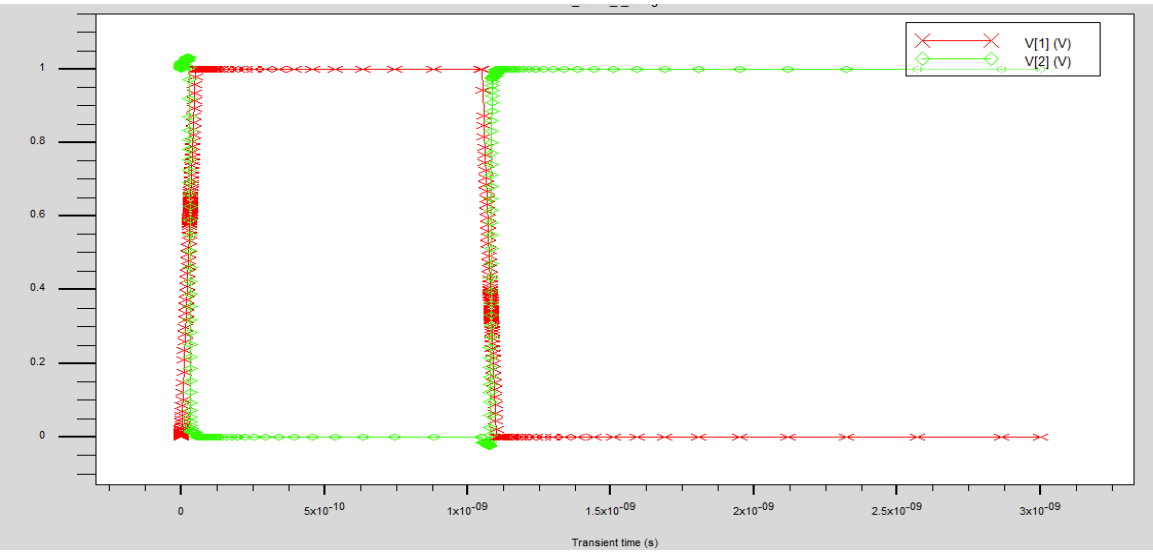

Figure 5.11: Transient characteristics of CMOS Inverter

The voltage transfer characteristic (VTC) of the CMOS inverter is the curve between output and input voltage of the circuit as shown in Figure 5.12. It is also known as DC characteristics of CMOS inverter. The static behavior of the inverter is represented by VTC and it is a key metric parameter of an inverter. It can be seen that the output response of the CMOS inverter is quite fast. Hence for a very small duration, both the transistors are on and consume power in the form of short circuit current.

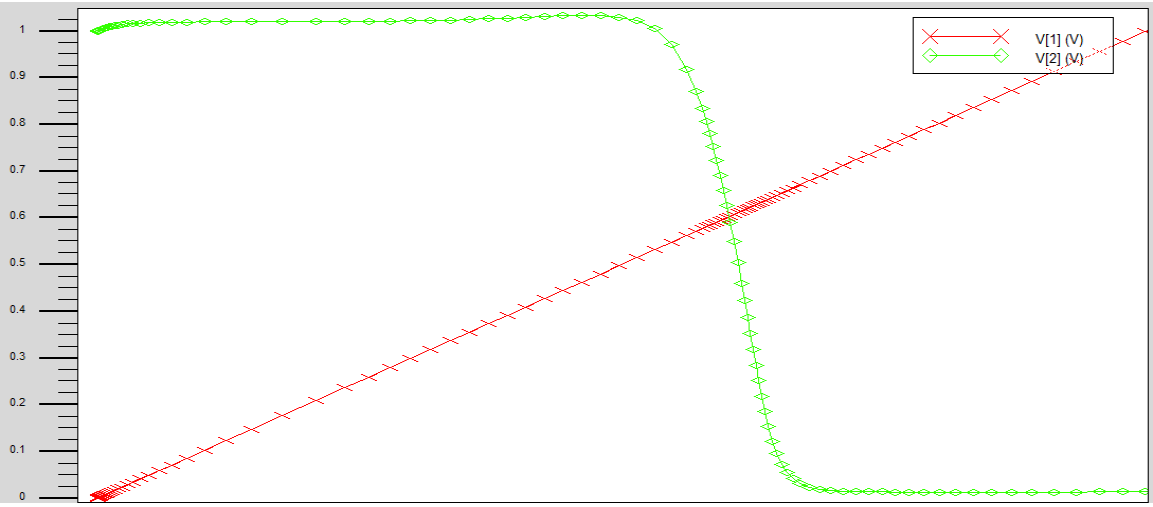

Figure 5.12: DC characteristics of CMOS Inverter

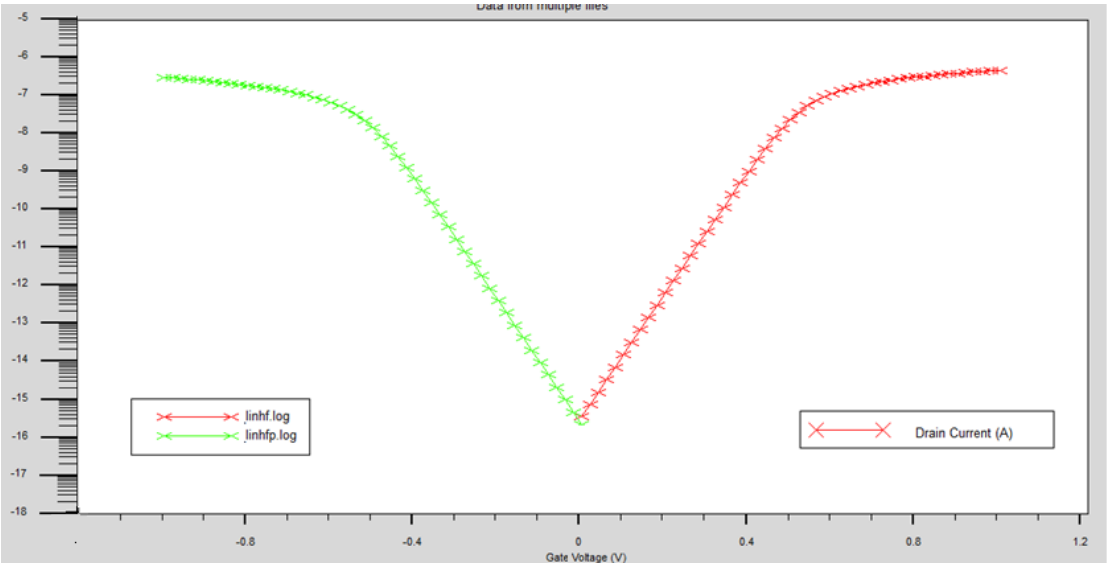

Figure 5.13: The V-curve of CMOS Inverter

Figure 5.13 shows the V curve which indicates the ideal matching of drive current for P and N devices in a CMOS inverter.

5.9 POWER DISSIPATION OF CMOS INVERTER

Power consumption in CMOS hugely relies upon load capacitance C_{load}. This capacitance is the combination of wiring capacitance and electrode capacitance. In operation of steady-state, the presented CMOS inverter dissipates an insignificant amount of power i.e. only a very little amount of power during the switching only. The on transistor delivers current to load when the full voltage swing takes place. This low leakage current performance of the CMOS device makes it suitable for low-power applications.

The power dissipation of the CMOS inverter is found to be $4.44*10^{-16}$ watts in comparison to $2*10^{-15}$ watts reported by Wagaj et al. in [205] for DMG SOI Junctionless MOSFET at 30nm technology node.

5.10 CONCLUSION

In this chapter, the Stacked Dielectric Triple Material Cylindrical Gate-All-Around Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET) was presented with the objective of obtaining very low sub-threshold current along with the suppression of short channel effects for the MOSFET device. Hence, the analytical model of sub-

threshold current and sub-threshold slope for Stacked Dielectric Triple Material Cylindrical Gate-All-Around Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET) was developed. The analytical results were compared for variation of different parameters and good agreement was obtained in the values. The value of the sub-threshold slope was found to be very close to the ideal value of SS for MOSFET. Since the sub-threshold current of the device was found to be very low the device was implemented in the basic CMOS inverter. A PMOS transistor for the purpose was also designed using the same SD-TM-CGAA-JLFET approach. The drive current of the PMOS transistor was tuned with the NMOS device so as to obtain the ideal matching in the drive current. Finally, the power dissipation of the CMOS inverter was computed and compared with [205]; it was found the power dissipation in the presented CMOS inverter is approx. 5 times less CMOS DMG-SOI JLT inverter than reported by Wagaj et al. in [205].

CHAPTER-VI

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In today's era, every electronic device is getting more efficient than its predecessor in terms of size, performance, speed and power dissipation. The reduction in power dissipation and area are considered prime goals for designing devices for portable/ handheld devices. The reduction in size or the higher packing density of Integrated Circuits (ICs) is obtained by decreasing the dimension of the semiconductor devices or in other words by the process of scaling. Recently, the process of scaling of conventional MOSFET devices is somewhat halted as the Short Channel Effects (SCEs) surfaces for these devices of channel length in the nano regime. In recent times the research has diverted from improving the characteristics of conventional MOSFET to alternate structures of MOSFET. In multiple works of literature, various device structures involving Gate Engineering, Channel Engineering and Device Engineering have been proposed as future devices. These devices provide good results for scaling and also reduce the effects of Short Channel Effects.

In the current reported work basic high-k Double Gate-Junctionless Field Effect Transistor (DG-JLFET) is presented which is found to be reducing the effects of Short Channel Effects very efficiently. Further improvement in the form of SD-TM-CGAA-JLFET device includes the approaches of Channel Engineering, Gate Engineering and Device Engineering for the further reduction of SCEs. The models of these devices were developed analytically and numerical simulations of the device were carried out on Silvaco’s TCAD Tool.

The analytical modelling of the JLFET device for surface potential and threshold voltage was carried out in the current work by the solution of 2D Poisson’s Equation using the Parabolic Approximation Method to validate the suppression of Short Channel Effects.

The SD-TM-CGAA-JLFET device has the gate designed using three dissimilar work-functions metals. This approach results in producing gradual steps function profile at the interface between metal gates. The lower work-function gate is used towards the drain side which causes the reduction of the electric field in the channel region near the drain end. Hence, it results in a reduction in Short Channel Effects and enhancement in the transport efficiency of charge carriers.

Surface potential and threshold voltage sensitivity to different parameters of the MOS device such as channel length, channel thickness and applied voltages have been investigated by comparing the analytical results with the simulated model from Silvaco's TCAD. The analytical results so obtained are in good agreement with the simulated results.

The research work in this thesis begins with the analysis of the scaling process. It was found out that at the smaller channel length, the short channel effects get prominent in the bulk MOSFET devices. The scaled devices also require a reduction in oxide thickness. When oxide thickness reduces to 2 nm due to scaling, the SiO_2 dielectric is not an appropriate choice as a gate insulator. The alternative dielectric materials such as high-k materials having equivalent oxide thickness as of SiO_2 are used. HfO_2 is one such material with a dielectric constant of about 21 and a band gap of 6 eV, which is found to be a capable substitute. This approach of applying high-k dielectric to reduce the Short Channel Effects was also applied to Silicon-On-Insulator (SOI), which is the reported low-leakage current device in multiple works of literature. The Junctionless transistor is recently introduced promising devices structures offering low leakage current and reduced Short Channel Effects. It offers the advantage of easier fabrication for low dimension devices due to the absence of junction between source/channel and channel/drain.

Gate Engineering approach in which multi-gates are applied for better control of the channel, is applied to all the investigated structures. Different MOSFET devices with multi-gates structures and different gate oxide dielectric materials are explored for low power applications in this research work.

The leakage current or the off current is a vital feature to assess the performance of the device and development of such device having very low off current been the

prime objective of the thesis. The presented SD-TM-CGAA-JLFET device was found to have a very low value of off current in the range of 4.9 e^{-16} A for NMOS. The PMOS using the same approach was developed and found to have off current in the range of 3.98 e^{-16} A. These two devices were implemented in the inverter circuit. Since the off currents of the devices were very low, the static power dissipation of the inverter circuit designed using this NMOS and PMOS was found to be in the range of 4.44 e^{-16} watts in comparison to 2 e^{-15} watts of Wagaj et al. [205] for the devices made at comparative technology. The n-type SD-TM-CGAA-JLFET device shows a sub-threshold slope close to 60 mV/decade. It is due to the presence of the dual dielectric material over the channel.

The obtained results conclude that the devices employed with the high-k material perform considerably better than the equivalent devices having SiO_2 as a dielectric material for all the devices considered in this thesis.

It can also be concluded that Stacked Dielectric-Triple Materials-Cylindrical Gate All Around- Junctionless Field Effect Transistor (SD-TM-CGAA-JLFET) is found to be appropriate MOSFET devices that can be used in low power circuits.

6.2 FUTURE SCOPE

The 2D analytical model for SD-TM-CGAA-JLFET and Junctionless Transistor structures has been developed in the current work. This research work can be further extended such as:

- The analytical model can be further improved to represent the performance of the device for lower dimensions by incorporating Quantum Mechanical (QM) effects in the device modelling.
- A further improvement in device structures can be made by incorporating the hetero-dielectric as a gate insulator and by applying other Channel Engineering methods.
- The structures having high-k dielectric material can be further investigated for various oxide interface traps charges. These high-k materials can also be analyzed for stress and strain characteristics.

- Investigation of the RF characteristics and radiation-induced soft errors of the device may be carried out for the analog RF application of the device.

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BRIEF PROFILE OF RESEARCH SCHOLAR

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LIST OF PUBLICATION IN JOURNAL

S.No.	Title of Published Paper	Name of Journal	ISBN No.	Volume and Issue	Year	Pages
1	High-k Dielectric Double Gate Junctionless (DG-JL) MOSFET for Ultra Low Power Applications- Analytical Model	Silicon 2021 (SPRINGER) **[SCIE Journal]**	1876-9918	DOI: 10.21203/rs.3.rs-989803/v1	2021	-
2	Subthreshold Current Modeling of Stacked Dielectric Triple Material Cylindrical Gate All Around (SD-TM-CGAA) Junctionless MOSFET for Low Power Applications	Silicon 2021 (SPRINGER) **[SCIE Journal]**	1876-9918	https://doi.org/10.1007/s12633-021-01399-4	2021	-
3	Performance Investigation of Dual-Halo Dual-Dielectric Triple Material Surrounding Gate MOSFET with High-dielectrics for Low Power Applications	JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE (JSTS) **[SCI-E Journal]**	1598-1657	Vol 20 No. 3	2020	297-304
4	Elicitation of Scattering Parameters of Dual-Halo Dual-Dielectric Triple-Material Surrounding Gate (DH-DD-TM-SG) MOSFET for Microwave Frequency Applications	Advances In Electrical and Electronic Engineering **[ESCI Journal]**	1804-3119	Vol 19 No. 1	2021	66-73
5	Performance Analysis of Noise in Dual Halo Dual Dielectric Triple Material Surrounding Gate MOSFET for RF Applications	International Journal of Nanoscience **[ESCI Journal]**	1793-5350	https://doi.org/10.1142/S0219581X20400025	2019	-
6	Analytical Modeling and Simulation of	International Journal of	2278-3075	Vol 8 Issue 10	2019	2946-2950

	Nanoscale Fully Depleted Dual Metal Gate SOI MOSFET	Innovative Technology and Exploring Engineering **[SCOPUS Journal]**				
7	Comparative Analysis of FD-DMDG SON MOSFET over FD DMDG SOI MOSFET	Journal of Electronic Design Technology **[UGC Approved Journal]**	2229-6980	Vol 9 No 1	2018	9-16
8	Study of Scaling of MOSFET on Various Electrical Characteristics using Silvaco TCAD Tool	Journal of Semiconductor Devices and Circuits **[UGC Approved Journal]**	2455-3379	Vol 5 No 1	2018	11-19
9	An Investigation into NMOS at 65nm using Silvaco TCAD	IJMTE **[UGC Approved Journal]**	2249-7455	Vol 8 Issue IX	2018	553-560
10	Comparative Analysis of Fully Depleted DMG SOI-MOSFET and SMG SOI-MOSFET	International Journal of Recent Research Aspects **[Peer Reviewed Journal]**	2349-7688	Vol 2 Issue 2	2015	125-128

PAPER PRESENTED AT WoS/SCOPUS CONFERENCE

S.No.	Title of Paper	Name of Conference	Type of Conference
1	A Systematic Study on Mitigating Parameter Variation in MOSFETS	Fifth International Conference on Soft Computing for Problem Solving (SocProS 2015)	International Conference at IITR (SPRINGER Conference)
2	Noise analysis of Dual Halo Dual Dielectric Triple Material Surrounding Gate MOSFET for RF applications	3rd International IEEE conference "2019 Devices for Integrated Circuit (DevIC)"	IEEE Conference
3	Performance Analysis of Fully Depleted SOI (FD-SOI) MOSFET Incorporating Dielectric Engineering	3rd International Conference on Future of Engineering Systems and Technologies, (FEST 2021)	International Conference (IOP Conference)
4	An Investigation of Different Gate Dielectric Material for FD-SOI MOSFET	Computing for Sustainable Global Development (INDIACom-2017)	IEEE Conference
5	Electric field modeling and critiques of Dual-Halo Dual-Dielectric Triple-Material Surrounding-Gate MOSFET	International Conference on Intelligent Computing and Smart Communication 2019	International Conference (SPRINGER Conference)
6	Analytical Modelling and Performance Analysis of Surface Potential for Junctionless MOSFET	International Conference on Computing, Communication, Electrical and Biomedical System (ICCCEBS -2021)	International Conference (IOP Conference)
7	Design of an Ultra-Low Power CMOS ADC using Threshold Inverter Quantization for Communication System	IEEE ICONAT 2021	IEEE Conference
8	Adder circuit design using advanced quantum dot cellular automata (AQCA)	Recent Advances in Electronics & Computer Engineering (RAECE)	IEEE Conference at IITR
9	Low Power Sub-threshold Domino AND Gate	FEST 2020, International Conference on Future of Engineering Systems and Technologies	International Conference (IOP Conference)
10	Power Efficient Combinational Circuits using Reversible Gate	Machine Learning and Smart system (MISS-2020)	International Conference (SPRINGER Conference)

PAPER PRESENTED AT INTERNATIONAL/NATIONAL CONFERENCE

11	Surface potential modeling and critiques of Dual-Halo Dual-Dielectric Triple-Material Surrounding-Gate MOSFET	International Conference on Materials and Energy (ICME 2019)	International Conference
12	2D Simulation Study of Novel Attributes of Dual Halo Dual Dielectric Triple Gate Surrounding MOSFET	Advancements in Engineering and Technology 2019	International Conference
13	Performance Investigation of Fully Depleted SOI MOSFET with Various Dielectric Materials	International Conference on Innovations in Smart Technology, Advanced Materials and Communication Engineering (ISTAMCE 2021)	International Conference
14	Simulation of NMOS Transistor using Silvaco TCAD at 65nm Technology	International Conference on Materials Research and Technology (ICMRT-2017)	International Conference
15	Performance Analysis of Junction Less Double Gate (JL DG) MOSFET for Low Power	International Conference on Innovations in Smart Technology, Advanced Materials and Communication Engineering (ISTAMCE 2021)	International Conference
16	Simulation and Analysis of Multiplexer using Various Design Methodology	International Conference on Innovations in Smart Technology, Advanced Materials and Communication Engineering (ISTAMCE 2021)	International Conference
17	A Simulation Perspective for Novel Characteristics of DH-DD-TM-SG MOSFETs	8th International Symposium on Fusion of Science and Technology (ISFT-2020)	International Conference
18	Design and Analysis of 90nm nMOSFET for Lower Leakage	International Conference on Recent research and Innovation in Social Science & Education (RISE 2018)	International Conference
19	FinFET structural analysis and process Mechanism	Medical Instrumentation, Biomaterials and Signal Processing 2020	National Conference
20	A review of Conventional and junction less MOSFET using TCAD simulation	Medical Instrumentation, Biomaterials and Signal Processing 2020	National Conference

21	An Investigation of Different Gate Dielectric Material for FD-SOI MOSFET	National Conference on Role of Science and Technology Towards 'Make in India' (RSTTMI-2016)	National Conference
22	A Comparative Study and Analysis of MOSFET at 200nm, 90nm and 65nm Technology Using Silvaco TCAD Tool	National Conference on Role of Science and Technology Towards 'Make in India' (RSTTMI-2016)	National Conference
23	Parameters Extraction of 200nm NMOS Transistor using Silvaco TCAD Tools	Second National Conference on Machine Intelligence and Research Advancement (NCMIRA-2015)	National Conference
24	A Study of Power Dissipation for Various1-bit Comparators	National Conference on Role of Science and Technology Towards 'Make in India' (RSTTMI-2016)	National Conference
25	Analytical Comparison of different 1-Bit full adder's scheme for 250nm CMOS technology	National Conference on Science in Media (SIM-2012)	National Conference